ALP LAB

Over-the-Air Firmware Updates

AN-006 · E1M and E1M-X SoMs

Document Number: AN-006 **Revision:** 0.6 **Date:** November 2026 **Status:** Preliminary

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1 Scope

Set up signed Over-the-Air (OTA) firmware updates for fielded SoMs. Two flows are supported by the Alp SDK™:

- **Yocto / Linux** targets (Cortex-A55 on V2N family) use **Mender** for full-image updates with A/B partition rollback. This is the shipping in-field path.
- **Zephyr** targets (Cortex-M on AEN, and the M33 on V2N) use **MCUboot** with ECDSA-P256 signing. On E1M-AEN, MCUboot is built single-slot (`SB_CONFIG_MCUBOOT_MODE_SINGLE_APP=y`; slot1 and scratch were removed to fit the per-core slot0 budget), so there is **no** A/B swap and **no** automatic rollback: a bad image is refused at boot and must be replaced by reflashing slot0. There is **no in-field OTA client** for Zephyr yet (deferred to v1.1); deliver signed images by physical reflash or via a Linux companion until then.

Audience	Engineers and DevOps teams managing fielded SoM fleets.
Prerequisites	Functional Wi-Fi or Ethernet network (see **AN-002**), secure-boot keys generated (see **AN-010**), Mender server or local CDN reachable.
Outcome	End-to-end OTA: build artefact, sign, upload to update server, device pulls and installs, automatic rollback on failed health-check.
Time	60 minutes (server setup is the long pole).
Source	`docs/tutorials/12-mender-ota.md`, `docs/ota.md`, `docs/ota-device-contract.md` in alp-sdk.

Table 1 Scope summary

2 Hardware Setup

No carrier-side wiring beyond the standard network connection. The on-module memory layout (eMMC + LPDDR4X on V2N; MRAM + optional OSPI on AEN; single slot0 per core on AEN, no A/B) provides the partition layout the OTA flows expect.

> **Note:** For the V2N family, the bootloader (U-Boot) owns A/B partition selection and automatic rollback. The GD32 bridge MCU is updated through its own independent firmware-update path (see `docs/ota-device-contract.md`) and is decoupled from the main-system OTA, so a failed bridge update cannot brick the application core, and vice versa.

3 Software Walkthrough

3.1 Yocto / Linux (V2N A55)

Enable Mender declaratively via the top-level `ota:` block in your project's `board.yaml` (the orchestrator emits the matching `MENDER_*` weak-assignments plus `INHERIT += "mender-full"` into the slice's `local.conf`), then build the Mender-aware image:

```
# Build the Mender-aware Alp image (produces the signed .mender artefact):
MACHINE=e1m-v2n101-a55 bitbake alp-image-edge
# Output: tmp/deploy/images/e1m-v2n101-a55/alp-image-edge-e1m-v2n101-a55.mender
# Upload the .mender artefact via the Mender UI's Releases tab,
# then create a Deployment targeting your device group.
```

3.2 Zephyr (AEN / V2N M-class)

Drive MCUboot from the `boot:` block in `board.yaml` (the orchestrator emits the `SB_CONFIG_BOOTLOADER_MCUBOOT`, `SB_CONFIG_MCUBOOT_SIGNATURE_TYPE_ECDSA_P256`, and `SB_CONFIG_BOOT_SIGNATURE_KEY_FILE` sysbuild options). The underlying build is a sysbuild MCUboot child image that signs the slot0 app at build time – there is no separate `west sign` step:

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```
# Build a signed image via sysbuild (MCUboot child image + signed slot0 app):
west build -p always --sysbuild \
    -b alp_e1m_aen801_m55_he/ae822fa0e5597ls0/rtss_he \
    examples/aen/aen-mcuboot-smoke -d build/mcuboot-smoke -- \
    "-DEXTRA_ZEPHYR_MODULES=<alp-sdk>;<hal_alif>" \
    '-DSB_CONFIG_BOOT_SIGNATURE_KEY_FILE="<abs>/keys/mcuboot_shared_dev_ecdsa_p256.pem"'
# Signs with the public shared dev key trusted by the factory MCUboot (no security).
# A key from keys/generate_dev_key.sh is accepted only by an MCUboot rebuilt with it and re-
provisioned.
# Signed slot0 app: build/mcuboot-smoke/aen-mcuboot-smoke/zephyr/zephyr.signed.bin
```

There is no in-field OTA client header (`<alp/ota.h>`) for Zephyr yet. Until v1.1, deliver the signed image by physical reflash (J-Link / OpenOCD) or via a Linux companion coordinating through the bridge. The declarative `boot:` + `ota:` blocks are exercised by `examples/connectivity/iot-fleet-ota` (the v0.6 reference, `native_sim`-verified; HiL gates on a staged Mender server).

3.3 Helper-MCU firmware: CC3501E radio co-processor (AEN)

The CC3501E is updated over the Alif→ CC3501E SPI bridge, independently of the application core. **The full OTA cold-swap cycle is proven on silicon:** the image streams over the bridge (`OTA_BEGIN` → RAM-staged `OTA_WRITE` → `OTA_FINISH`), which only **stages** it; `OTA_PROMOTE` then commits the swap, the bridge link drops for a few seconds while the CC3501E reboots, and BL2/MCUboot swaps the pending slot to primary. The swapped image self-accepts and persists across a true cold power-on with no rollback. `cc3501e_ota_update()` runs the whole sequence, including `OTA_PROMOTE`, for you.

> **Warning:** **The OTA payload's signed version must exceed the running primary.** The CC3501E enforces monotonic anti-rollback: a downgrade is refused at `psa_fwu` install and the session ends in the error state. This is the single most common cause of a "streams cleanly but nothing changes" result.

The CC3501E firmware and its signed artefacts (detached ECDSA-P256 `.sig` and `.sha256` manifest) are published in the `prebuilt/` directory of the `alplabai/cc3501e-bridge-firmware` repository (moved out of alp-sdk by ADR 0031). Verify both files before use. The AEN SoM presets list it as `helper_firmware cc3501e_otp` with no `firmware_path` and `flash_policy: recovery_only`: Alp Lab programs the CC3501E in production, a customer flash is permitted only to recover a bricked device with Alp Lab-supplied binaries, and `tan flash` declines this entry.

> **Warning:** **`OTA_FINISH` stages; `OTA_PROMOTE` commits — and `PROMOTE` must run in the same CC3501E boot as `FINISH`.** `cc3501e_ota_promote()` (`OTA_PROMOTE`, opcode `0x46`) requests the swap-reboot for the image the last `FINISH` staged. The swap request is held in CC3501E RAM, so after any reset of the CC3501E between `FINISH` and `PROMOTE` the image still reads STAGED but **cannot be promoted** (`OTA_STATUS` reports `reserved[0] = 119`, and no swap happens). A staged image cannot be promoted after a reset: call `cc3501e_ota_abort()` (or start a new `cc3501e_ota_begin()`, which clears the slot), re-send the whole image, then run `FINISH` and `PROMOTE` back to back in one boot. `cc3501e_ota_promote()` only issues the promote when the image store reports a STAGED image, and returns `ALP_ERR_NOT_READY` otherwise.

> **Note:** **Confirm the result with `GET_VERSION`, not `OTA_STATUS`.** After a good update, `OTA_STATUS` `pending` reads 4 (`FAILED`). That value describes the **old**, now non-primary slot, not the new image, so a successful update can look like a failed one. Re-establish the bridge link after the reboot and check the new firmware version with `GET_VERSION`.

Wire protocol MAJOR 4. The bridge protocol is now MAJOR 4: every frame except the opening `GET_VERSION` exchange carries a CRC-16/CCITT-FALSE trailer, and the success reply code `RESP_OK` is `0x5A` (it was `0x00`). The SDK host speaks both MAJOR 3 and MAJOR 4 (it decodes each firmware by the major it reports), so **update the host first**, then the CC3501E firmware: a host that only speaks 4 cannot talk to a fleet still on 3.

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3.4 Helper-MCU firmware: GD32 bridge (V2N)

The GD32 bridge firmware is published in the `alplabai/gd32-bridge-firmware` repository (moved out of alp-sdk). It is updated through Path A — an application bootloader plus A/B slots, over the opcode range `0xF0–0xF6` (`OTA_BEGIN`, `WRITE_CHUNK`, `VERIFY`, `COMMIT`, `ROLLBACK`, `GET_STATE`, `ABORT`). It is **safe by default**: the flash path is armed only in a `-DBRIDGE_OTA_PARTITIONED` build. A stock build answers `STATUS_NOSUPPORT` across the whole range and touches no flash, so the unpartitioned image cannot brick itself.

Current hardening a customer should design around:

Behaviour	What it means for you
Slot and image validation	A slot id that is not A or B is rejected outright rather than silently resolving to slot A. A CRC-valid but truncated or vector-less image is rejected at `COMMIT` **and** again before the bootloader jumps — CRC integrity alone is treated as necessary but not sufficient.
Newest-first boot records, with fallback	The bootloader orders both A/B metadata records newest-first and tries each in turn. A newer record that fails validation does **not** suppress an older bootable one, so a bad update cannot strand the part in recovery while a good slot sits unused.
Host gates OTA on protocol minor >= 6	The chunk wire format changed incompatibly in v0.6 (an explicit length byte after the offset) in a way a major-only handshake cannot detect. Call `gd32g553_ota_supported()` first: it is true only if the bridge advertised minor >= 6 at init. `gd32g553_ota_begin()` and `_write_chunk()` refuse an older peer with `ALP_ERR_NOSUPPORT` **before** touching flash, so a current host cannot corrupt a pre-v0.6 bridge.
`OTA_BEGIN` is non-blocking	`BEGIN` no longer erases the slot synchronously — that stalled the SPI reply long enough to hang the host. It arms a background erase pumped from `bridge_hw_tick` (one page-region per main-loop tick) and acks immediately, leaving the state machine BUSY. **Poll `gd32g553_ota_get_state()` until it reports READY before streaming the first chunk**; a chunk sent while BUSY is rejected.

Table 2 GD32 bridge OTA Path-A behaviour

> **Note: Scope of the GD32 silicon claim.** Boot-select, dual-bank erase, and the background-erase path are silicon-validated on the GD32, as is the full stream → verify → commit → boot-new-slot → rollback cycle over the 25 MHz link. That validation covers the **bridge firmware and its host driver on the V2N bench** (`hil_silicon: verified` in the SDK's chip manifest); the driver's `driver_status` is still `partial`. First flash of a partitioned part additionally needs a factory metadata record written at `0x08008000`. A bricked part is recovered with a bench SWD probe. A host-driven SWD reflash also exists (`<alp/chips/gd32_swd.h>`, driven over the GD32 SWD lines from the host) but is **untested on silicon**: do not rely on it for field recovery. Its `GD32_SWD_GENERIC_CM33_R0P1_IDCODE` constant (`0x6BA02477u`) is a generic Cortex-M33 value that has not been measured on a GD32, so never treat an IDCODE mismatch as fatal or as proof of wrong silicon or wiring; if you want to refuse on a mismatch, compare against a value measured on your own board.

4 The Update Audit Log and Its Assurance Tiers

`<alp/update_log.h>` gives one portable, append-only, hash-chained record of what firmware was installed and whether it was accepted. `alp_update_log_verify()` walks the chain and reports mutation, truncation, rollback, or reorder. The log never wraps: when the backing store fills, `alp_update_log_append()` returns `ALP_ERR_NOMEM` and the existing chain stays intact and verifiable, because wrapping would erase audit history.

The strength of that record is **not the same on every SoM**. Query it — never assume it:

```
#include <alp/update_log.h>

alp_update_log_t *log = alp_update_log_open();
if (alp_update_log_assurance(log) == ALP_UPDATE_LOG_HW_ENFORCED) {
```

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```
    /* Log writer lives behind a hardware boundary. */
} else {
    /* ALP_UPDATE_LOG_SW_TAMPER_EVIDENT -- app-cooperative. */
}
```

Tier	What it actually guarantees
`ALP_UPDATE_LOG_SW_TAMPER_EVIDENT`	Every target. Hash chain anchored to a monotonic counter; `alp_update_log_verify()` **detects** out-of-band mutation, truncation, rollback, and reorder. It is tamper-**evident**, not tamper-proof: code that can write the backing partition can rebuild the store and its counter consistently and **forge a coherent history**. With `CONFIG_ALP_SDK_UPDATE_LOG_PERSIST` plus an `alp_ulog_partition` fixed partition the log survives reboot and update; without it, entries live in RAM and vanish on reboot. **Persistence does not raise the assurance level.**
`ALP_UPDATE_LOG_HW_ENFORCED`	Only where a trusted owner exists. The application core is a **client**; the log writer and its store sit behind a hardware boundary the app cannot rewrite. Routes: TF-M (`CONFIG_ALP_SDK_UPDATE_LOG_TFM`, PSA Protected Storage) and Alif E4/E8 AEN (a trusted M55 owner plus an SE/firewall-locked MRAM partition). If the trusted owner or the isolation proof is absent, `alp_update_log_open()` **silently falls through to the software tier** — unless `CONFIG_ALP_SDK_UPDATE_LOG_REQUIRE_HW_ENFORCED` is set, which makes it fail closed instead.

Table 3 Update-log assurance tiers

Warning: **Scope the `HW_ENFORCED` guarantee precisely: it is app-immutable, not reflash-immutable.** The application cannot rewind or rewrite the log — the owner holds it and its sequence counter inside the protected region. It does **not** survive an attacker who can reflash the part. A reflash-proof guarantee needs a monotonic anchor stored outside the rewindable MRAM, and current E8 SE firmware exposes no runtime-writable one (no SE NV-counter mailbox, no runtime OTP-write path, no per-log MCUboot security counter). If your threat model includes an adversary with physical reflash access, this log is **not** your control.

Note: Prefer `alp_update_log_append_boot()` over `alp_update_log_append()` for update-result entries. It sources the version, image hash, and verification status from the platform's authenticated boot-metadata provider instead of accepting them from app code, so firmware cannot log a forged-but-well-formed entry. Platforms with no provider return `ALP_ERR_NOSUPPORT` — which is the signal to fix provisioning, not to fall back to the app-supplied path. Both boot-metadata entry points are marked `[ABI-EXPERIMENTAL]`: the surface may change until the hardware backend is silicon-proven.

5 Expected Output

On the Yocto / Mender path, watch the device pick up a deployment:

```
$ journalctl -u mender-client -f
... Update available
... Downloading update
... Installing update to the inactive A/B rootfs slot
... Rebooting to apply update
... (after reboot) Running version: alp-image-edge-...
... Update committed
```

If the new image boots cleanly and the post-reboot health check passes, the swap is committed. If the device does not confirm within the inventory interval, the bootloader reverts to the previous partition automatically on the next reset. On the Zephyr / MCUboot path the equivalent confirm is the image calling MCUboot's `boot_set_confirmed()` within its health-check window;

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an image that never confirms is rolled back by MCUboot on the next reboot on targets built with a secondary slot. Not on E1M-AEN: its single-slot MCUboot does not roll back.

6 Troubleshooting

- **Signature verification fails**: the artefact was signed with a different key than the ECDSA-P256 verify key provisioned into the device. On Mender this anchor is the verify key written into the rootfs (`/etc/mender/`); on MCUboot it is the public key compiled into the bootloader. Use the same key pair from your **AN-010** secure-boot provisioning.
- **Health-check times out**: the device never confirmed the new image. On Zephyr, the firmware must call MCUboot's `boot_set_confirmed()` within its health-check window (typically 30 s after boot). On Yocto, the device must check in within `MENDER_INVENTORY_INTERVAL` (default 60 s) or the bootloader rolls back after `MENDER_RETRY_POLL` (default 5 min).
- **Download stuck at 0 %**: server URL unreachable, or TLS pinning mismatch. Test with `curl` from the device or host first.
- **Rollback loop**: the new image keeps failing health-check, so the bootloader keeps reverting (targets with a secondary slot only; E1M-AEN single-slot MCUboot does not revert). Pin the version on the server until the bug is fixed.

7 References

- **Tutorial**: `docs/tutorials/12-mender-ota.md` in alp-sdk.
- **OTA architecture**: `docs/ota.md`, `docs/ota-device-contract.md`.
- **Examples**: `examples/connectivity/iot-fleet-ota/` (declarative `boot: + ota:` reference, `native_sim`-verified), `examples/connectivity/firmware-update-log/` (update audit log; its README carries the assurance-tier scoping), `examples/aen/aen-mcuboot-smoke/` (SES → MCUboot → slot0 secure-boot bench test).
- **SDK API**: `<alp/update_log.h>` (firmware-update audit log + `alp_update_log_assurance()`), `<alp/iot.h>` (transport), `<alp/security.h>` (signature verification). There is no `<alp/ota.h>` Zephyr OTA client header yet.
- **Helper-MCU OTA**: `<alp/chips/cc3501e/ota.h>` and `<alp/protocol/cc3501e.h>` (CC3501E bridge OTA, incl. `OTA_PROMOTE 0x46`); `<alp/chips/gd32g553.h>` (GD32 bridge Path-A OTA opcodes); the GD32 bootloader design lives in the `alplabai/gd32-bridge-firmware` repository.
- **Companion AN**: **AN-010** (secure boot and code signing — the key pair that signs every artefact here).

8 Revision History

Revision	Changes	Date
0.1	• Initial draft.	May 2026
0.2	• Corrected to current SDK: ▸ removed non-existent `<alp/ota.h>/alp_ota_confirm()/ CONFIG_ALP_OTA_GRACE_SECONDS` ▸ clarified that Zephyr in-field OTA is deferred to v1.1 (MCUboot signed boot + `boot_set_confirmed()` rollback only) ▸ aligned Yocto build to `bitbake alp-image-edge` (MACHINE `e1m-v2n101-a55`) and Zephyr build to the sysbuild MCUboot flow ▸ fixed example path to `examples/connectivity/iot-fleet-ota` and added `firmware-update-log/aen-mcuboot-smoke` ▸ pointed API references at `<alp/update_log.h>`, `<alp/iot.h>`, `<alp/security.h>`.	June 2026
0.3	• Added the update-log assurance tiers with the load-bearing scoping that `HW_ENFORCED` is app-immutable, not reflash-immutable, and that the SW tier detects but cannot prevent forgery. • Added the CC3501E OTA state (full cold-swap proven on E8, forward-version-only, `OTA_PROMOTE` 0x46, signed v0.2.0 prebuilt) and the GD32 bridge Path-A hardening, with the silicon claim scoped to boot-select, dual-bank erase and background erase — bridge firmware, not the `gd32g553` chip driver.	July 2026

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Revision	Changes	Date
	• Corrected cross-references: secure boot is AN-010, not AN-008. • Fixed the Alp SDK repository links (`alpDevs` → `alplabai`).	
0.4	• Re-verified against Alp SDK™ v0.17.0. • CC3501E: ‣ firmware and signed artefacts now come from `alplabai/cc3501e-bridge-firmware` (the `cc3501e_otp` entry has no `firmware_path` and is recovery-only) ‣ documented wire-protocol MAJOR 4 (CRC-16/CCITT-FALSE trailer except on the opening `GET_VERSION`, `RESP_OK` `0x5A`, host speaks 3 and 4 so update the host first) ‣ `OTA_FINISH` now only stages and `OTA_PROMOTE` commits, in the same CC3501E boot, so a staged image cannot be promoted after a reset ‣ after a good update `OTA_STATUS` `pending` reads 4 for the old slot, so confirm with `GET_VERSION`. • Removed the obsolete “unjamming a stuck slot” advice. • GD32: ‣ firmware now in `alplabai/gd32-bridge-firmware` ‣ the `gd32g553` chip is `hil_silicon: verified` ‣ a host-driven SWD reflash exists but is untested on silicon, and its IDCODE constant must never be made a fatal check.	October 2026
0.5	• Release history: every entry formatted as a bullet list.	October 2026
0.6	• Product name on page 1 links to the product page on alplab.ai.	November 2026

Table 4 Revision History

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