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E1M-AEN — ALIF SEMICONDUCTOR ENSEMBLE

Edge-1 AI Module (E1M™) — built on the open E1M standard

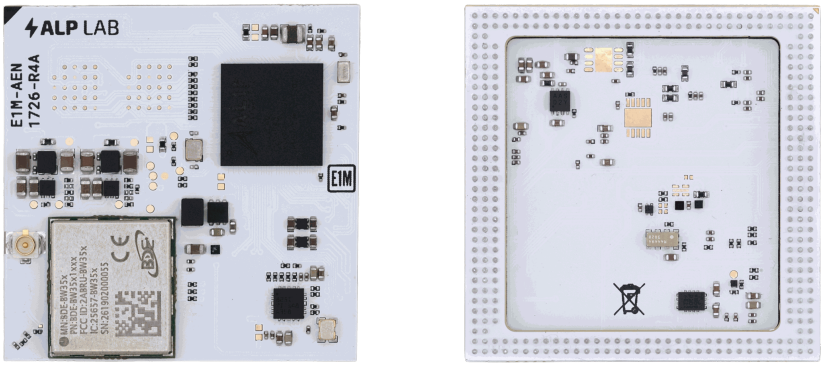


Figure 1 E1M-AEN module — front (left) and back (right)

The E1M-AEN Ensemble series modules use the Edge-1 AI Module (E1M™) form factor, an open standard (E1M-STD-1.0) for the footprint and pinout, with a unified pin layout and hardware functionality. This footprint allows users to interchange MCU/MPU modules seamlessly while keeping hardware compatible. E1M™ is designed for flexibility, functionality, and longevity in high- and medium-range MCU/MPUs.

Features

- Various core options with the same footprint, based on the Alif Semi Ensemble MCU/MPU series:
  - E8 — 2 × 800 MHz ARM A32, 2 × ARM M55, 2 × ARM Ethos U55 + 1 × ARM Ethos U85
  - E7 — 2 × 800 MHz ARM A32, 2 × ARM M55, 2 × ARM Ethos U55
  - E6 — 1 × 800 MHz ARM A32, 2 × ARM M55, 2 × ARM Ethos U55 + 1 × ARM Ethos U85
  - E5 — 1 × 800 MHz ARM A32, 2 × ARM M55, 2 × ARM Ethos U55
  - E4 — 2 × ARM M55, 2 × ARM Ethos U55 + 1 × ARM Ethos U85
  - E3 — 2 × ARM M55, 2 × ARM Ethos U55
- Internal memory: 13.5 MB (E3 / E5 / E7) or 9.75 MB (E4 / E6 / E8) SRAM on-die, 5.5 MB MRAM
- External memory: HyperRAM and NOR flash on one OSPI bus, fitted on E1M-AEN803 only; a build option on E1M-AEN301 / 401 / 501 / 601 / 701; not available on E1M-AEN801
- MIPI DSI display output, 2 lanes, up to 1.25 Gbps/lane
- MIPI CSI-2 camera input, 2 lanes
- 2.4 GHz Wi-Fi 6 with up to 20 Mbps throughput
- Bluetooth LE 5.4
- 100 Mbps Ethernet PHY
- CAN-BUS PHY (assembly option)
- Ultra-low-power standby: STOP ≈ 3.84 µA, self-off with RTC self-wake ≈ 1.14 µA (typical, calculated)
- On-module real-time clock with a backup input for a carrier-side coin cell or supercapacitor, and a carrier wake output
- Assembly variants available for cost reduction
- Small size: 35 × 35 mm

Applications

IoT, industrial, robotics, motor drive, drones, mobile PoS, smart speakers, object detection, medical devices, vending machines, smart home, process control, smart appliances, scanners.

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Table of Contents

Features . . . 1
Applications . . . 1
1 General Description . . . 4
1.1 Highlights . . . 4
1.2 Block Diagram . . . 5
1.3 Module Variants . . . 6
1.4 Hardware Revisions . . . 6
1.5 Alif Semi Ensemble MCUs/MPUs . . . 7
2 Pin Diagram and List . . . 8
2.1 Power & Control Pins . . . 12
2.2 Analog Pins . . . 14
2.3 Digital Pins . . . 15
2.4 Not Connected Pins . . . 18
2.5 Reserved Pins . . . 20
3 Specifications . . . 20
3.1 Absolute Maximum Ratings . . . 20
3.2 Recommended Operating Conditions . . . 21
3.3 Electrical Characteristics . . . 21
3.4 ESD & Latch-up Ratings . . . 22
3.5 Thermal Characteristics . . . 23
4 Power . . . 24
4.1 Power Architecture . . . 24
4.2 RTC Backup . . . 26
4.3 Power-Up & Reset Sequence . . . 27
4.4 Power Consumption . . . 28
5 Boot Modes . . . 29
6 Reset, Module Enable & Power Control . . . 29
6.1 Module States . . . 30
6.2 Control Timing . . . 30
6.3 Carrier Sequences . . . 31
7 JTAG / SWD Debug . . . 32
8 Interfaces . . . 33
8.1 Ethernet . . . 33
8.2 USB . . . 34
8.3 Serial Interfaces . . . 35
8.3.1 I^2C . . . 35
8.3.2 I^3C . . . 35
8.3.3 UART . . . 35
8.3.4 SPI . . . 36
8.3.5 I^2S . . . 36
8.3.6 CAN Bus . . . 36
8.4 Wireless Module & Antenna . . . 37
8.4.1 RF Characteristics . . . 38
8.4.2 Antenna Options . . . 38
8.4.3 Regulatory Information . . . 39
8.5 SD Card . . . 39
8.6 MIPI DSI Display & Backlight Controller . . . 40
8.7 MIPI CSI Camera . . . 41
8.7.1 On-die ISP & JPEG Encoder (E4 / E6 / E8) . . . 41
8.8 Parallel Camera . . . 42
8.9 Microphone – PDM . . . 43
8.10 Analog Inputs . . . 43
8.11 Analog Outputs . . . 43
8.12 Memories . . . 44
8.12.1 Identity EEPROM and I^2C0 . . . 44
8.12.2 Application MRAM Partition Map . . . 44
9 Environmental & Reliability . . . 45
9.1 Operating & Storage Conditions . . . 45
9.2 Reflow Profile . . . 45
9.3 Reliability Data . . . 46
10 Software & Operating System Support . . . 46
11 Reference Schematic . . . 47
12 Compliance & Certifications . . . 49
12.1 Environmental Compliance . . . 49
12.2 Wireless Certifications . . . 49
12.3 Functional Safety & Industry-specific Compliance . . . 49
13 Mechanical & Footprint Dimensions . . . 49
13.1 Recommended PCB Land Pattern . . . 49
13.2 Mounting and Keep-Out Zones . . . 50
13.3 Module Marking . . . 51
14 Packaging . . . 51
14.1 Trays . . . 51
14.2 MSL & Handling . . . 51
15 Ordering Information . . . 51
15.1 MPN Decoder . . . 51
15.2 Ordering Matrix . . . 52
16 References & Related Documents . . . 53
17 Revision History . . . 53
18 Legal Notices . . . 59
18.1 Disclaimer . . . 59
18.2 Trademarks . . . 59
18.3 Export Control . . . 59
18.4 Contact . . . 59

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List of Figures

Figure 1 E1M-AEN module — front (left) and back (right) . . . 1
Figure 2 E1M-AEN Block Diagram . . . 5
Figure 3 Alif Semi Ensemble MCU/MPU Series . . . 7
Figure 4 E1M-AEN Pin-out (top view, 312-pad LGA), top left: rows A–Q, columns 1–17 . . . 9
Figure 5 E1M-AEN Pin-out (top view, 312-pad LGA), top right: rows A–Q, columns 18–34 . . . 10
Figure 6 E1M-AEN Pin-out (top view, 312-pad LGA), bottom left: rows R–AH, columns 1–17 . . . 11
Figure 7 E1M-AEN Pin-out (top view, 312-pad LGA), bottom right: rows R–AH, columns 18–34 . . . 12
Figure 8 E1M-AEN Power-dissipation Derating (estimated) . . . 24
Figure 9 E1M-AEN Power Architecture . . . 26
Figure 10 E1M-AEN Power-Up Timing (module level) . . . 28
Figure 11 E1M-AEN Reset Timing (PORn warm reset) . . . 32
Figure 12 Reference JTAG / SWD Header Pinout . . . 33
Figure 13 E1M-AEN Ethernet Connection . . . 33
Figure 14 E1M-AEN USB 2.0 Carrier Connection . . . 34
Figure 15 E1M-AEN I^2C / I^3C Carrier Pull-ups . . . 35
Figure 16 E1M-AEN UART and SPI Pads . . . 36
Figure 17 E1M-AEN CAN Connection: Standard Build and CAN PHY Assembly Option . . . 37
Figure 18 E1M-AEN Antenna Connection . . . 38
Figure 19 E1M-AEN SD Card Connection . . . 39
Figure 20 E1M-AEN MIPI DSI and Backlight Connection (carrier side) . . . 40
Figure 21 E1M-AEN MIPI CSI-2 Camera Connection and Camera Rails (carrier side) . . . 41
Figure 22 E1M-AEN Parallel Camera Pads . . . 43
Figure 23 E1M-AEN PDM Microphone Connection (two microphones per data line) . . . 43
Figure 24 E1M-AEN Memory Options . . . 45
Figure 25 Recommended reflow profile: measured E1M-AEN profile, smoothed (JTR1000 oven, ALPHA OM338) . . . 46
Figure 26 E1M-AEN Minimum Reference Circuit (power and control) . . . 48
Figure 27 E1M-AEN Recommended Land Pattern (top view) . . . 50

List of Tables

Table 1 E1M-AEN Variant Summary . . . 6
Table 2 Carrier-visible Changes, R2 ⟶ R3 . . . 6
Table 3 Ensemble MPU Options . . . 8
Table 4 E1M-AEN Power & Control Pins . . . 12
Table 5 E1M-AEN Analog Pins . . . 14
Table 6 E1M-AEN Digital Pins . . . 15
Table 7 E1M-AEN Not-connected Pins . . . 18
Table 8 E1M-AEN Reserved Pins . . . 20
Table 9 E1M-AEN Absolute Maximum Ratings . . . 20
Table 10 E1M-AEN Recommended Operating Conditions . . . 21
Table 11 E1M-AEN Electrical Characteristics . . . 21
Table 12 E1M-AEN ESD & Latch-up Ratings . . . 23
Table 13 E1M-AEN Thermal Characteristics . . . 23
Table 14 Module Output Rails . . . 25
Table 15 RTC Backup Options . . . 26
Table 16 E1M-AEN Power Consumption (typical, calculated) . . . 28
Table 17 Reset, Enable & Power-control Signals . . . 29
Table 18 Module States Seen from the Carrier . . . 30
Table 19 Carrier Control Timing . . . 30
Table 20 Reference Carrier Configurations . . . 31
Table 21 JTAG / SWD Pinout . . . 32
Table 22 Ethernet PHY Configuration . . . 33
Table 23 E1M-AEN USB Interface . . . 34
Table 24 E1M-AEN Wi-Fi 6 / BLE RF Characteristics . . . 38
Table 25 Wireless Regulatory Approvals . . . 39
Table 26 E1M-AEN MIPI Interface Summary . . . 40
Table 27 External Memory per Variant . . . 44
Table 28 Application MRAM Partition Map (Alp SDK v0.17.0) . . . 44
Table 29 Environmental Conditions . . . 45
Table 30 Reflow Profile Parameters (Pb-free): recommended window and measured values . . . 46
Table 31 Reliability Targets . . . 46
Table 32 Software Support Matrix . . . 47
Table 33 Environmental Compliance . . . 49
Table 34 E1M-AEN Mechanical Dimensions . . . 49
Table 35 Land Pattern Parameters . . . 50
Table 36 Tray Specifications . . . 51
Table 37 E1M-AEN MPN Convention . . . 51
Table 38 Ordering Information . . . 52
Table 39 Related Documents . . . 53
Table 40 Revision History . . . 53

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1 General Description

1.1 Highlights

The Alp Lab E1M-AEN System-on-Module (SoM) is a low-power, cost-effective solution for edge-AI applications. Powered by the Alif Semiconductor Ensemble series processor, it features an Arm Cortex-A32 application CPU (up to 2 × 800 MHz), Arm Cortex-M55 real-time cores, integrated Arm Ethos U55 / U85 NPUs, and an optional JPEG encoder and ISP, making it suitable for low-power edge-AI tasks.

The E1M-AEN supports one camera over a 2-lane MIPI CSI-2 interface and provides customizable options including on-board Wi-Fi / Bluetooth, multiple memory and storage configurations, and PHY variants.

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1.2 Block Diagram

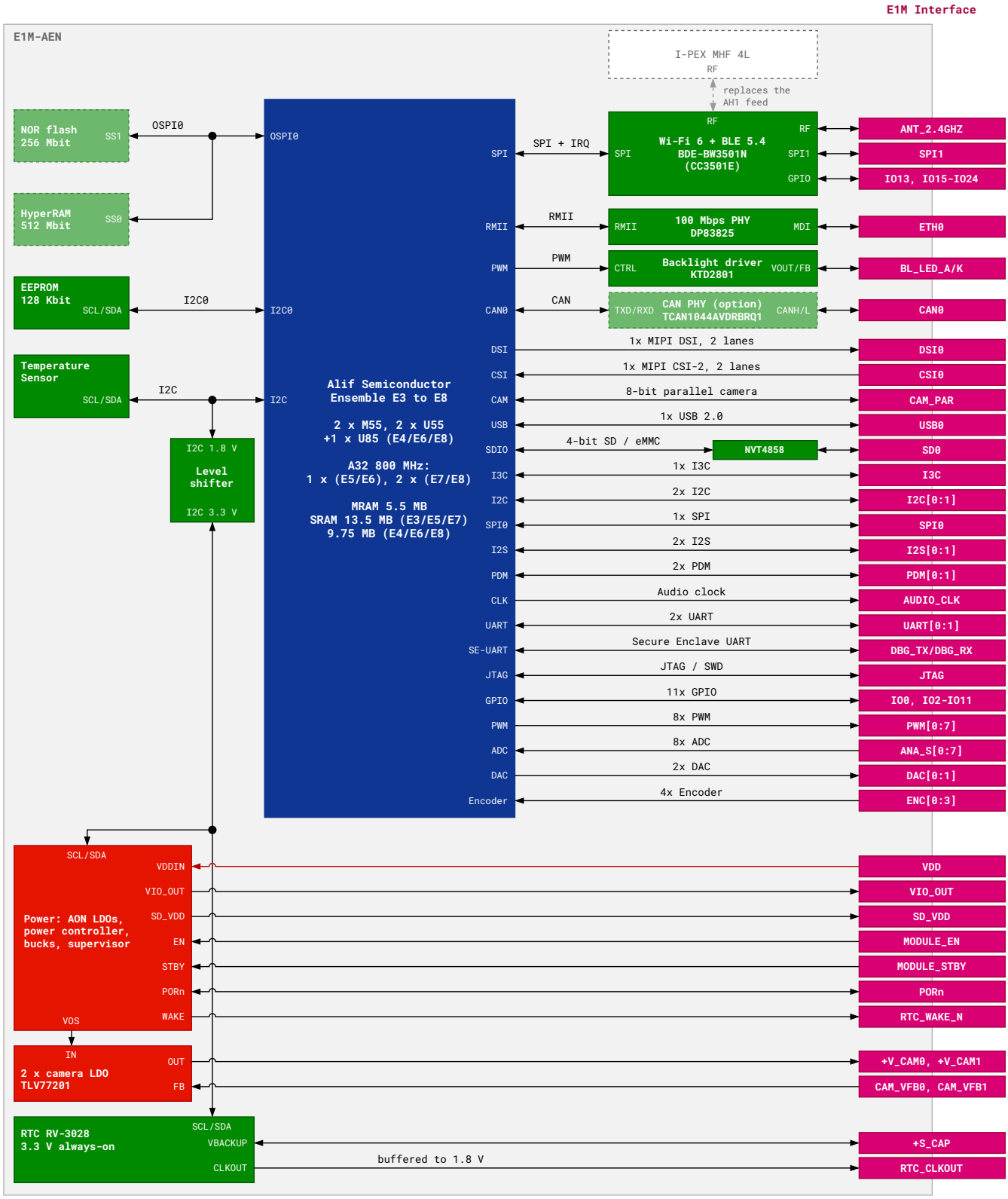


Figure 2 E1M-AEN Block Diagram

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1.3 Module Variants

The E1M-AEN family ships in seven MPN variants that share a common E1M™ footprint. Variants differ in the Ensemble SoC used, the application-CPU (A32) count, and the on-die NPU/ISP configuration. See Section 15 for the full ordering matrix and MPN decoder; the table below summarises the differences.

MPN	Ensemble	A32 cores	NPUs	ISP / JPEG
E1M-AEN301	E3	–	2 × U55	–
E1M-AEN501	E5	1 × 800 MHz	2 × U55	–
E1M-AEN701	E7	2 × 800 MHz	2 × U55	–
E1M-AEN401	E4	–	2 × U55 + 1 × U85	Yes
E1M-AEN601	E6	1 × 800 MHz	2 × U55 + 1 × U85	Yes
E1M-AEN801	E8	2 × 800 MHz	2 × U55 + 1 × U85	Yes
E1M-AEN803	E8	2 × 800 MHz	2 × U55 + 1 × U85	Yes

Table 1 E1M-AEN Variant Summary

External memory differs per variant. E1M-AEN803 is the E8 variant with both external OSPI memories fitted: 512 Mbit HyperRAM and 256 Mbit NOR flash. E1M-AEN801 fits neither. On E1M-AEN301, 401, 501, 601 and 701 both memories are a build option (assembly variant); the standard build has on-die memory only. Contact Alp Lab for an assembly variant with external memory.

1.4 Hardware Revisions

This revision of the datasheet describes E1M-AEN hardware revision **R3**. R3 keeps the E1M™ footprint and the SoC options of R2 and changes the power architecture and a small number of pad assignments. Carrier boards designed for R2 must be checked against the table below before they carry an R3 module.

Item	R2	R3
USB 2.0 pads	I1 / J1 / I2 / J2	B1 / C1 / C2 / D2 (I1, J1, I2, J2 not connected)
IO8, IO9, IO10, IO11 (AG33, AH34, AH33, A18)	Wi-Fi module GPIOs	SoC GPIOs P15_1, P15_7, P15_5, P7_5; IO8, IO9 and IO10 can wake the SoC from STOP
IO21–IO24 (L3, M3, N3, O3)	Not connected	Wi-Fi module GPIOs (valid only while Wi-Fi is powered)
IO25 (P3)	Not connected	RTC_WAKE_N open-drain wake output to the carrier
MODULE_STBY (O2)	RTC event input only, 1.8 V (100 kΩ pull-up to 1.8 V on the module)	Sleep / wake / self-off control, 5 V tolerant; open drain, or push-pull from 1.8 V, 3.3 V or 5 V logic with $V_{OH} \geq 1.45$ V (Section 6)
MODULE_EN (O1)	Module enable	Module enable with a 1.0 ms glitch filter, 5 V tolerant; same levels as MODULE_STBY (Section 6)
Reset and brownout supervisor	None on the module (module erratum E-02, see the note below)	On-module supervisor orders the SoC reset when the supply falls
+S_CAP (AG15)	–	RTC backup input. The carrier provides the backup store (coin cell or supercapacitor) or ties the pad to GND (Section 4.2). Never enable the RTC trickle charger with a coin cell fitted.
VIO_OUT (P1, P2)	200 mA	100 mA, ≤ 2.5 µF carrier load
+V_CAM0 / +V_CAM1	0.6–3.3 V, 300 mA each	0.6–3.1 V, 170 mA combined

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Item	R2	R3
VDDIN operating range	4.5–5.5 V	4.75–5.25 V
Wi-Fi, Ethernet PHY, OSPI memory supply	Wi-Fi switched by a SoC GPIO; Ethernet PHY and OSPI memory always powered	All switched off by default; enabled by the Alp SDK™ on demand
SD_VDD (AH10)	Supply input: the carrier powers the SD card	3.4 V output from the module, switched by firmware, off by default. Remove any carrier supply from AH10.
Self-off with RTC self-wake	–	Yes

Table 2 Carrier-visible Changes, R2 → R3

Note: R2 modules: no on-module reset or brownout supervisor. This is a module erratum (E-02 in the E1M-AEN Errata), caused by the Ensemble SoC requirement in Alif errata ER004 (E4, E6 and E8, all silicon revisions): the SoC must be held in reset while its supply is below 1.65 V, or it can be permanently damaged. R3 fixes it with a supervisor on the module, so an R3 carrier needs no brownout circuit; it only has to meet the VDDIN limits and the hold-up capacitance in Recommended Operating Conditions. The impact on R2 modules and the R2 workaround are in the errata.

Note: The MIPI CSI-2 pad polarity (P33/P34, Q33/Q34, R33/R34) listed in this datasheet applies to R3. On R2 the P and N pads of each CSI-2 lane are swapped on the module.

1.5 Alif Semi Ensemble MCUs/MPUs

This document should be read together with the corresponding Alif Semiconductor Ensemble MCU/MPU datasheet.

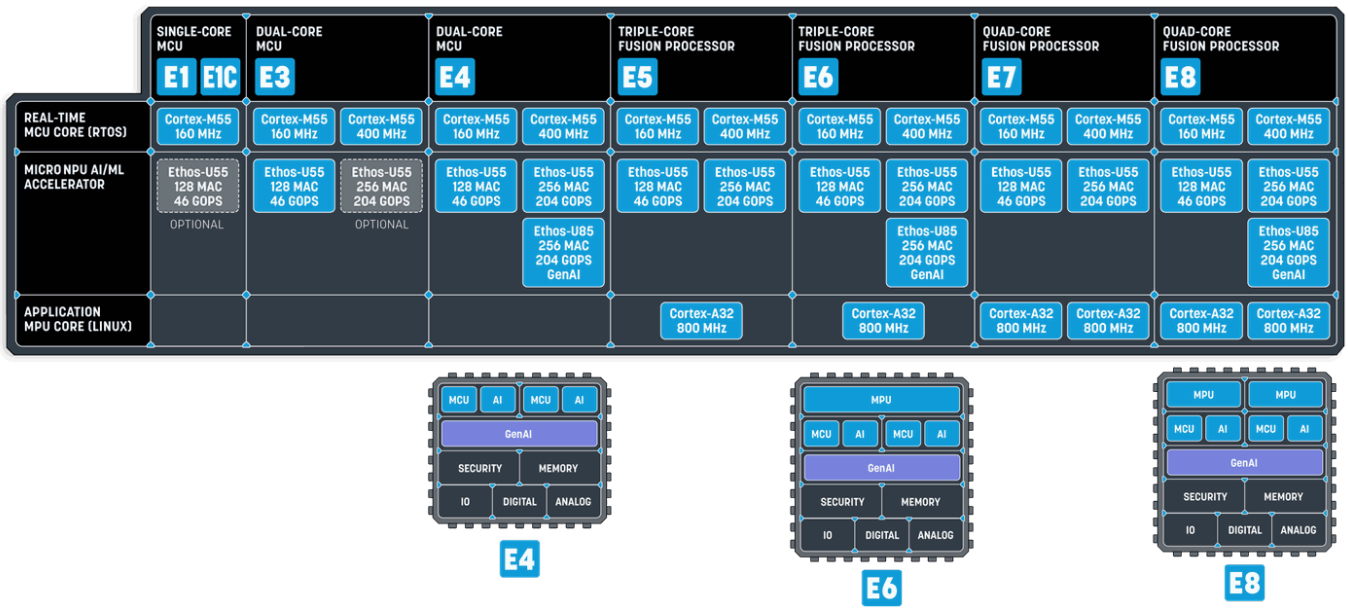


Figure 3 Alif Semi Ensemble MCU/MPU Series

Ensemble	MCU	MPU	NPU	Internal Memory	External Memory	ISP / JPEG
E3	2 × M55	–	2 × U55	5.5 MB – 13.5 MB	2 × OSPI	–
E5	2 × M55	1 × A32 800 MHz	2 × U55	5.5 MB – 13.5 MB	2 × OSPI	–
E7	2 × M55	2 × A32 800 MHz	2 × U55	5.5 MB – 13.5 MB	2 × OSPI	–
E4	2 × M55	–	2 × U55 + 1 × U85	5.5 MB – 9.75 MB	2 × OSPI	Yes
E6	2 × M55	1 × A32 800 MHz	2 × U55 + 1 × U85	5.5 MB – 9.75 MB	2 × OSPI	Yes
E8	2 × M55	2 × A32 800 MHz	2 × U55 + 1 × U85	5.5 MB – 9.75 MB	2 × OSPI	Yes

Table 3 Ensemble MPU Options

2 Pin Diagram and List

The E1M™ standard defines the primary pin functions; the pin-out below follows that standard. Pins can be reassigned to alternate functions in software, but hardware compatibility with other E1M variants will no longer hold because each MCU/MPU has a different pin structure and peripheral mapping.

Pad names follow the pad frame of the E1M™ standard (top view, component side up): the pad letter is the row, A to AH from top to bottom, and the pad number is the column, 1 to 34 from left to right. A1 is the top-left pad, next to the 0.5 mm triangular pin-1 fiducial; the module outline is a plain rectangle. A2 is directly to its right and B1 directly below it; A34 is the top-right pad, AH1 the bottom-left pad and AH34 the bottom-right pad.

The pin-out is drawn in the top view across the 35 mm × 35 mm module. The pad band is two pads deep along the top and bottom edges (rows A, B and AG, AH) and three pads deep along the left and right edges (columns 1–3 and 32–34); pads C3, AF3, C32 and AF32 are not fitted. The map is split into four quarters (rows A–Q / R–AH, columns 1–17 / 18–34), drawn at one scale, so that every pad name stays legible; each column is drawn at the same horizontal position in every row.

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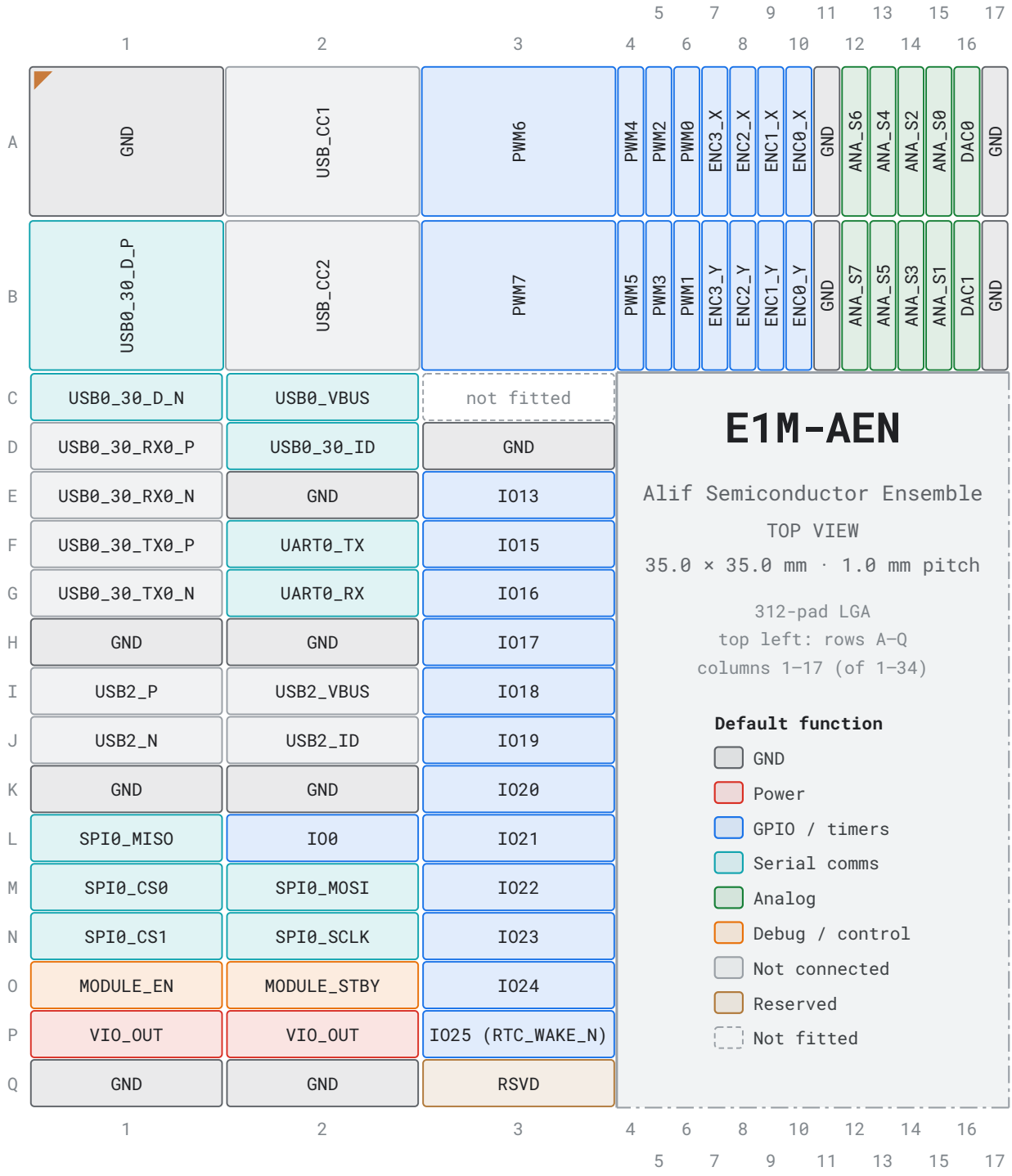


Figure 4 E1M-AEN Pin-out (top view, 312-pad LGA), top left: rows A–Q, columns 1–17

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Figure 5 E1M-AEN Pin-out (top view, 312-pad LGA), top right: rows A–Q, columns 18–34

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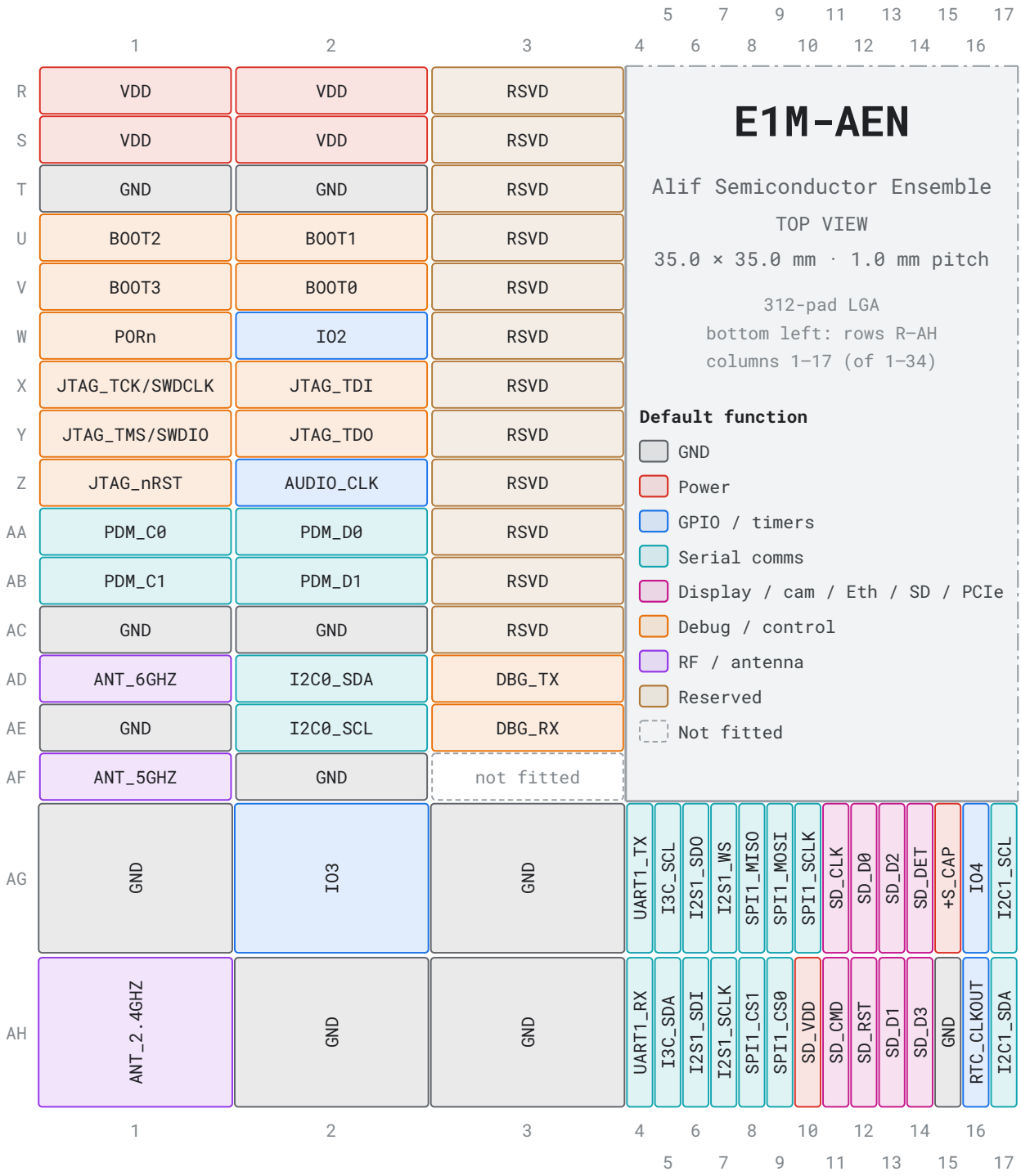


Figure 6 E1M-AEN Pin-out (top view, 312-pad LGA), bottom left: rows R–AH, columns 1–17

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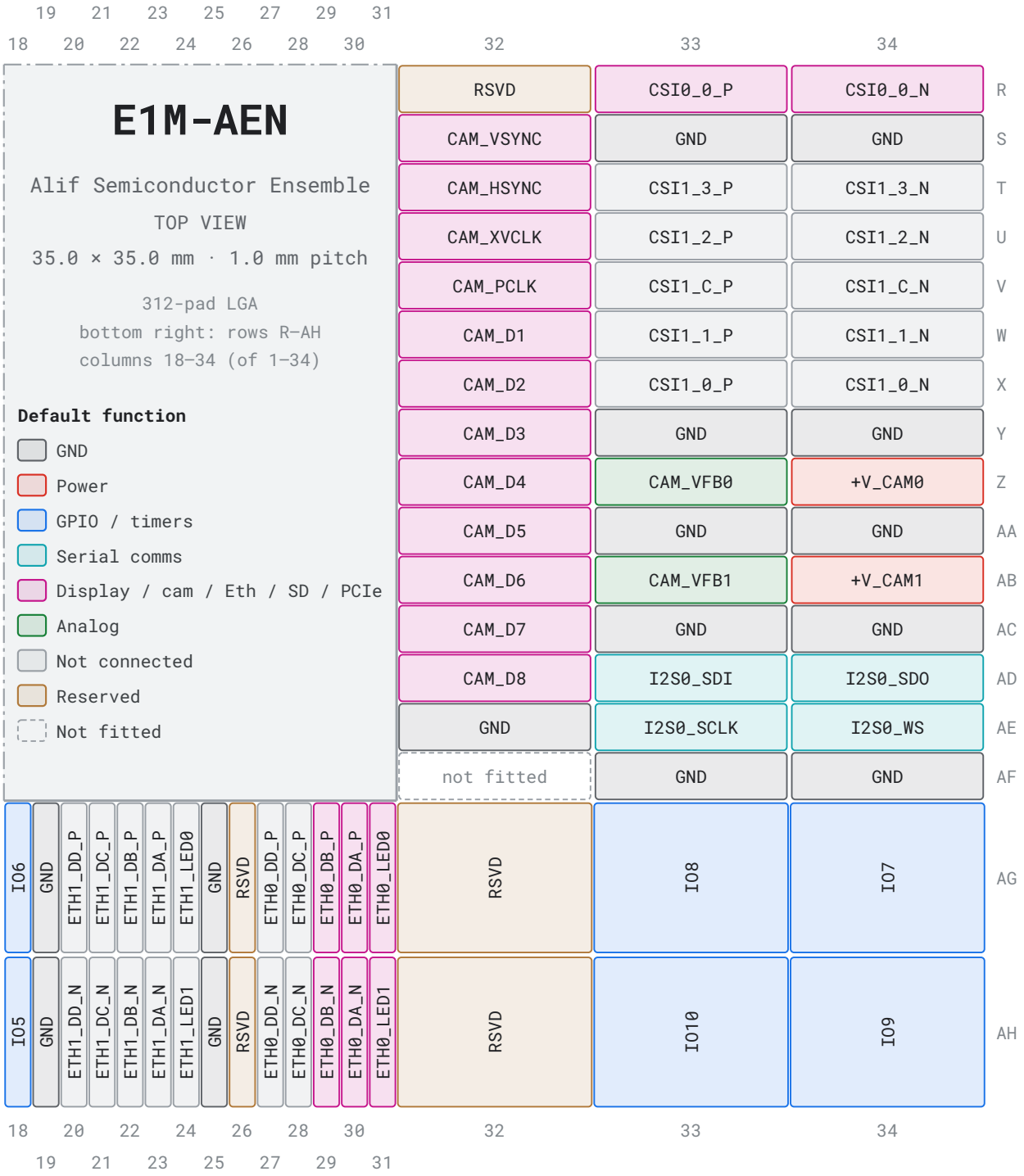


Figure 7 E1M-AEN Pin-out (top view, 312-pad LGA), bottom right: rows R–AH, columns 18–34

2.1 Power & Control Pins

Pin Number	Pin Name	Description
A1, A11, A17, A20, A30, A32, AA33, AA34, AC1, AC2, AC33, AC34, AE1, AE32, AF2, AF33, AF34, AG1, AG3, AG19, AG25, AH2, AH3, AH15, AH19, AH25, B11, B17, B20, B30, B32, D3, E2, G33, G34, H1, H2,	GND	Ground.

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Pin Number	Pin Name	Description
K1, K2, M33, M34, Q1, Q2, S33, S34, T1, T2, Y33, Y34		
R1, S1, R2, S2	VDD	+5V main supply input to the module. No input protection on the module; see Section 3.1.
P1, P2	VIO_OUT	+1V8 output, output only. High = module rails up. Up to 100 mA, ≤ 2.5 µF carrier load. Use as the I/O reference for carrier-side level shifters.
Z34	+V_CAM0	Adjustable LDO output (TLV77201). 0.6 V to 3.1 V; 170 mA combined with +V_CAM1. Switched by firmware.
AB34	+V_CAM1	Adjustable LDO output (TLV77201). 0.6 V to 3.1 V; 170 mA combined with +V_CAM0. Switched by firmware.
Z33	CAM_VFB0	Feedback node (FB pin) of the +V_CAM0 LDO. The module has no divider: fit the divider from +V_CAM0 to this pad to GND on the carrier, close to the module pin. Leave Z33 and Z34 floating only if +V_CAM0 is never enabled.
AB33	CAM_VFB1	Feedback node (FB pin) of the +V_CAM1 LDO. The module has no divider: fit the divider from +V_CAM1 to this pad to GND on the carrier, close to the module pin. Leave AB33 and AB34 floating only if +V_CAM1 is never enabled.
AH10	SD_VDD	SD/eMMC card power output, 3.4 V, up to 212 mA. Switched by firmware, off by default. No current limit on the module: protect the card socket on the carrier. Never connect a carrier supply to this pad.
AG15	+S_CAP	RTC backup input. Connects a backup store on the carrier to the on-module real-time clock: a coin cell (BR-type primary lithium), a supercapacitor, or nothing. If no store is fitted, tie the pad to GND; do not leave it floating. Keep the total leakage on this pad (ESD diode, holder) ≤ 10 nA. See Section 4.2 before connecting anything: never enable the RTC trickle charger with a coin cell fitted (the cell can leak, vent or burst).
O1	MODULE_EN	Module enable, active high, 5 V tolerant. Drive open drain, open collector or a switch to GND (preferred), or push-pull from 1.8 V, 3.3 V or 5 V logic (V_{OH} ≥ 1.45 V). Low for ≥ 2 ms forces the module off; release to power on. No carrier pull-up is needed; left open the pad sits at about 1.2–1.5 V. Leave open if not used. See Section 6.
O2	MODULE_STBY	Module stand-by request and wake, active low, 5 V tolerant. Same circuit and levels as MODULE_EN: open drain, open collector or a switch to GND (preferred), or push-pull from 1.8 V, 3.3 V or 5 V logic (V_{OH} ≥ 1.45 V). No carrier pull-up is needed. Leave open if not used. See Section 6.
W1	PORn	SoC reset, open-drain, wired-AND on the module: 100 kΩ pull-up to the module 1.8 V rail and 1 nF to GND on the module; do not add a carrier pull-up or capacitor. High = SoC out of reset. Pull low for ≥ 2 ms to reset the SoC; leave floating if not used. Never drive it high. R3 modules hold it low through the on-module supervisor when the supply falls; R2 modules have no supervisor and the carrier must provide one (Section 1.4).

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Pin Number	Pin Name	Description
U1	BOOT2	E1M boot-strap pins. Alif SoCs do not have boot-mode pins; not used on E1M-AEN. Leave floating.
U2	BOOT1	
V1	BOOT3	
V2	BOOT0	
X1	JTAG_TCK/SWDCLK	JTAG/SWD pins for programming and debug, 1.8 V, direct to the SoC JTAG0 pins (P4_4 TCK, P4_6 TDI, P4_5 TMS, P4_7 TDO); no pull-ups on the module. JTAG_nRST (Z1) is the SoC NSRST input, open drain, with a 20 kΩ pull-up to 1.8 V on the module; no carrier pull-up. See Section 7.
X2	JTAG_TDI	
Y1	JTAG_TMS/SWDIO	
Y2	JTAG_TDO	
Z1	JTAG_nRST	
AH1	ANT_2.4GHZ	Antenna feed (RF_ANT) from the on-module BDE-BW3501N. Route a 50 Ω trace to the antenna or connector.
AF1	ANT_5GHZ	5 GHz antenna. Not used on E1M-AEN (2.4 GHz only). Leave floating.
AD1	ANT_6GHZ	6 GHz antenna (Wi-Fi 6E). Not used on E1M-AEN. Leave floating.
A31	BL_LED_A	Boost output of the on-module backlight LED driver (KTD2801): connect to the anode of the LED string. Up to 36 V (driver over-voltage limit); never connect it to a logic input or to another supply. Assembly option without the driver: BL_PWM, 1.8 V SoC PWM output; contact Alp Lab.
B31	BL_LED_K	Feedback / current-sense input of the backlight driver (KTD2801 FB). Connect the LED string cathode here and the current-setting resistor R_{FB} from this pad to GND on the carrier: full-scale $I_{LED,max}$ = 200 mV / R_{FB}. The module has no R_{FB}. Leave floating if BL_PWM is used.

Table 4 E1M-AEN Power & Control Pins

2.2 Analog Pins

Pin Number	Pin Name	Peripheral	Description
A12	ANA_S6	AIN	Analog input channels, referenced to 1V8. SoC analog channel per pad: ANA_S0–ANA_S3 = SoC ANA_S0–ANA_S3 (P0_0–P0_3); ANA_S4 = ANA_S6 (P0_6); ANA_S5 = ANA_S8 (P1_0); ANA_S6 = ANA_S14 (P1_6); ANA_S7 = ANA_S15 (P1_7).
A13	ANA_S4		
A14	ANA_S2		
A15	ANA_S0		
B12	ANA_S7		
B13	ANA_S5		
B14	ANA_S3		
B15	ANA_S1		
A16	DAC0	DAC0	Analog output channel, referenced to 1V8.
B16	DAC1	DAC1	Analog output channel, referenced to 1V8.

Table 5 E1M-AEN Analog Pins

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2.3 Digital Pins

Pin Number	Pin Name	Peripheral	Description
AG2	IO3	GPIO	SoC general purpose input/output, 1.8 V. SoC pin per pad: IO0 = P9_1, IO2 = P12_5, IO3 = P3_2, IO4 = P4_3, IO5 = P7_4, IO6 = P9_7, IO7 = P4_0. Drive from the carrier only while VIO_OUT is high.
AG16	IO4		
AG18	IO6		
AG34	IO7		
AH18	IO5		
L2	IO0		
W2	IO2		
A18	IO11	GPIO	SoC GPIO: IO11 = P7_5. IO8 = P15_1, IO9 = P15_7 and IO10 = P15_5 are low-power GPIOs that can wake the SoC from STOP. Drive from the carrier only while VIO_OUT is high.
AG33	IO8		
AH34	IO9		
AH33	IO10		
E3	IO13	GPIO (Wi-Fi)	GPIOs of the on-module Wi-Fi / BLE module (CC3501E), 1.8 V; not connected to the Ensemble SoC. Wi-Fi module GPIO per pad: IO13 = GPIO_13, IO15 = GPIO_14, IO16 = GPIO_17, IO17 = GPIO_16, IO18 = GPIO_18, IO19 = GPIO_19, IO20 = GPIO_26, IO21 = GPIO_5, IO22 = GPIO_6, IO23 = GPIO_10, IO24 = GPIO_11. Valid only while Wi-Fi is powered. Never drive these pads while Wi-Fi is off: that back-powers the Wi-Fi module. Pull-downs are allowed. Avoid pull-ups; if one is unavoidable, use ≥ 100 kΩ to VIO_OUT and add its current to the standby figures. IO16 and IO17 are reserved by the current Alp SDK™ Wi-Fi firmware and are not available as customer I/O.
E3	IO15		
F3	IO16		
G3	IO17		
H3	IO18		
I3	IO19		
J3	IO20		
K3	IO21		
L3	IO22		
M3	IO23		
N3	IO24		
O3	IO25 (RTC_WAKE_N)		
P3		–	Real-time-clock wake output (E1M pad IO25), open drain, active low. Driven on the module by an N-MOSFET from the always-on power controller; no pull-up on the module. Goes low on an RTC alarm, timer or stand-by event and stays low until firmware clears the RTC flags. Valid in every power state while VDDIN is present. Carrier pull-up to its always-on rail, ≤ 5.5 V, ≥ 10 kΩ. Leave floating if not used.
Z2	AUDIO_CLK	–	Audio clock output.
AA1	PDM_C0	PDM0	Digital microphone interface.
AA2	PDM_D0		
AB1	PDM_C1	PDM1	Digital microphone interface (SoC PDM_C2 / PDM_D2: P11_4 / P5_4).
AB2	PDM_D1		
AD33	I2S0_SDI	I2S0	I^2S interface, 1.8 V (SoC I2S3: P9_2–P9_5).
AD34	I2S0_SDO		
AE33	I2S0_SCLK		
AE34	I2S0_WS		
AG6	I2S1_SDO	I2S1	I^2S interface, 1.8 V (SoC LPI2S, low-power I^2S).
AG7	I2S1_WS		
AH6	I2S1_SDI		
AH7	I2S1_SCLK		
AD2	I2C0_SDA	I2C0	

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Pin Number	Pin Name	Peripheral	Description
AE2	I2C0_SCL		I^2C interface, 1.8 V (SoC I2C2: P5_7 / P5_6). Shared with the on-module identity EEPROM at 0x50 and 0x58: carrier devices must not use these addresses. No pull-ups on the module: pull both lines up to VIO_OUT on the carrier (for example 4.7 kΩ), never to 3.3 V or an always-on rail.
AG17	I2C1_SCL	I2C1	I^2C interface, 1.8 V (SoC I2C1: P3_7 / P7_2). No pull-ups on the module: pull up to VIO_OUT on the carrier.
AH17	I2C1_SDA		
AG5	I3C_SCL	I3C	I^3C interface, 1.8 V (SoC P7_7 / P7_6). No pull-ups on the module: pull I3C_SDA up to VIO_OUT on the carrier; a pull-up on the push-pull I3C_SCL is optional.
AH5	I3C_SDA		
L1	SPI0_MISO	SPI0	SPI interface, 1.8 V (SoC SPI0). SPI0_CS0 = SoC SS0 (P5_2); SPI0_CS1 = SoC SS2 (P3_6).
M1	SPI0_CS0		
M2	SPI0_MOSI		
N1	SPI0_CS1		
N2	SPI0_SCLK		
AG8	SPI1_MISO	SPI1	SPI interface of the on-module Wi-Fi / BLE module (CC3501E), 1.8 V; not connected to the Ensemble SoC. Wi-Fi module pins: MISO = GPIO_34, MOSI = GPIO_33, SCLK = GPIO_32, CS0 = GPIO_31, CS1 = GPIO_15. Valid only while Wi-Fi is powered; never drive these pads while Wi-Fi is off.
AG9	SPI1_MOSI		
AG10	SPI1_SCLK		
AH8	SPI1_CS1		
AH9	SPI1_CS0		
F2	UART0_TX	UART0	UART interface, 1.8 V (SoC UART5: P3_5 TX / P3_4 RX).
G2	UART0_RX		
AG4	UART1_TX	UART1	UART interface, 1.8 V (SoC UART3: P1_3 TX / P1_2 RX).
AH4	UART1_RX		
A19	CAN_STBY	CAN0	Standard build (CAN PHY not fitted): B18 = CAN0_TX and B19 = CAN0_RX, 1.8 V SoC logic for a CAN transceiver on the carrier; A19 = SoC GPIO, 1.8 V. Never connect a CAN bus directly to these pads. CAN PHY assembly option: B18 = CANH, B19 = CANL (bus side, see Section 3.1), A19 = PHY standby input; contact Alp Lab.
B18	CAN0H/CAN0_TX		
B19	CAN0L/CAN0_RX		
A3	PWM6	PWM	PWM output.
A4	PWM4		
A5	PWM2		
A6	PWM0		
B3	PWM7		
B4	PWM5		
B5	PWM3		
B6	PWM1		
A10	ENC0_X	ENC0	Encoder input.
B10	ENC0_Y		
A9	ENC1_X	ENC1	Encoder input.
B9	ENC1_Y		
A8	ENC2_X	ENC2	Encoder input.
B8	ENC2_Y		
A7	ENC3_X	ENC3	Encoder input.
B7	ENC3_Y		
AG29	ETH0_DB_P	ETH0	

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Pin Number	Pin Name	Peripheral	Description
AG30	ETH0_DA_P		100 Mbit Ethernet, MDI side of the on-module DP83825 PHY: DA = TD± (transmit) and DB = RD± (receive) in MDI; Auto-MDIX can swap the pairs at link-up. Magnetics, connector and EMI/ESD protection go on the carrier. ETH0_LED0 is a 3.3 V output (DP83825 LED0, AVDD3V3 domain, independent of VDDIO); ETH0_LED1 is a 1.8 V output (DP83825 LED2, VDDIO). Both are also DP83825 bootstrap pins (auto-negotiation disable, RX_DV enable): wire carrier LEDs so that they do not change the strap levels at PHY reset.
AG31	ETH0_LED0		
AH29	ETH0_DB_N		
AH30	ETH0_DA_N		
AH31	ETH0_LED1		
AG11	SD_CLK	SD0	SD card or eMMC interface. SD_CLK, SD_CMD and SD_D0–SD_D3 pass through the on-module level translator and use SD_VDD levels (3.4 V); they are valid only while SD_VDD is on. SD_DET and SD_RST are 1.8 V SoC pads: pull SD_DET up to VIO_OUT, never to SD_VDD or 3.3 V.
AG12	SD_D0		
AG13	SD_D2		
AG14	SD_DET		
AH11	SD_CMD		
AH12	SD_RST		
AH13	SD_D1		
AH14	SD_D3		
P33	CSI0_C_P	CSI0	MIPI CSI-2 camera interface.
P34	CSI0_C_N		
Q33	CSI0_1_P		
Q34	CSI0_1_N		
R33	CSI0_0_P		
R34	CSI0_0_N		
D33	DSI0_C_P	DSI0	MIPI DSI display interface.
D34	DSI0_C_N		
E33	DSI0_1_P		
E34	DSI0_1_N		
F33	DSI0_0_P		
F34	DSI0_0_N		
AA32	CAM_D5	CAM_PAR	Parallel camera interface, 8-bit, 1.8 V. E1M CAM_D1–CAM_D8 = SoC CAM D0–D7 (P8_0–P8_7).
AB32	CAM_D6		
AC32	CAM_D7		
AD32	CAM_D8		
S32	CAM_VSYNC		
T32	CAM_HSYNC		
U32	CAM_XVCLK		
V32	CAM_PCLK		
W32	CAM_D1		
X32	CAM_D2		
Y32	CAM_D3		
Z32	CAM_D4		
B1	USB0_30_D_P	USB0	USB 2.0 interface (E1M standard USB0 D+/D-, VBUS and ID pads).
C1	USB0_30_D_N		
C2	USB0_VBUS		
D2	USB0_30_ID		

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Pin Number	Pin Name	Peripheral	Description
AH16	RTC_CLKOUT	–	Clock output of the on-module RTC (RV-3028 CLKOUT), buffered to 1.8 V on the module. Valid only while VIO_OUT is high (the buffer runs from the module 1.8 V rail).
AD3	DBG_TX	SE-UART	Secure Enclave UART of the Ensemble SoC, 1.8 V (dedicated pins, not GPIO). Used for programming MRAM with the Alif Security Toolkit and for the Secure Enclave console. Expose it on development and production carriers. DBG_TX has a 33 Ω series resistor; DBG_RX has 1 kΩ in series and a 1 MΩ pull-up to 1.8 V on the module. Drive DBG_RX only while VIO_OUT is high. SE-UART settings: 8N1 at 57 600 baud on the E4, E6 and E8 variants (E1M-AEN401, E1M-AEN601, E1M-AEN801, E1M-AEN803) and at 55 000 baud on the E3, E5 and E7 variants (E1M-AEN301, E1M-AEN501, E1M-AEN701); the Alif Security Toolkit negotiates the rate during its handshake. A wrong rate gives the toolkit error `Target did not respond`.
AE3	DBG_RX		

Table 6 E1M-AEN Digital Pins

2.4 Not Connected Pins

These pins carry an E1M standard function that is not implemented on E1M-AEN. They retain their standard name for cross-variant compatibility and must be left floating.

Pin Number	Pin Name	Description
AG27	ETH0_DD_P	ETH0 gigabit pairs (DC/DD) – E1M-AEN Ethernet is 100 Mbit. Leave floating.
AG28	ETH0_DC_P	
AH27	ETH0_DD_N	
AH28	ETH0_DC_N	
AG20	ETH1_DD_P	Second Ethernet (ETH1) – not implemented on E1M-AEN. Leave floating.
AG21	ETH1_DC_P	
AG22	ETH1_DB_P	
AG23	ETH1_DA_P	
AG24	ETH1_LED0	
AH20	ETH1_DD_N	
AH21	ETH1_DC_N	
AH22	ETH1_DB_N	
AH23	ETH1_DA_N	
AH24	ETH1_LED1	
A21	PCIE0_TX0_P	PCI Express (PCIE0) – not implemented on E1M-AEN. Leave floating.
A22	PCIE0_TX1_P	
A23	PCIE0_TX2_P	
A24	PCIE0_TX3_P	
A25	PCIE0_RX0_P	
A26	PCIE0_RX1_P	
A27	PCIE0_RX2_P	
A28	PCIE0_RX3_P	
A29	PCIE0_CLK_P	
B21	PCIE0_TX0_N	
B22	PCIE0_TX1_N	

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Pin Number	Pin Name	Description
B23	PCIE0_TX2_N	
B24	PCIE0_TX3_N	
B25	PCIE0_RX0_N	
B26	PCIE0_RX1_N	
B27	PCIE0_RX2_N	
B28	PCIE0_RX3_N	
B29	PCIE0_CLK_N	
I1	USB2_P	USB2 port – not used on E1M-AEN R3; the USB 2.0 interface is on the USB0 pads (B1, C1, C2, D2). Leave floating.
J1	USB2_N	
I2	USB2_VBUS	
J2	USB2_ID	
A2	USB_CC1	USB SuperSpeed lanes and USB-C configuration – not used on E1M-AEN. Leave floating.
B2	USB_CC2	
D1	USB0_30_RX0_P	
E1	USB0_30_RX0_N	
F1	USB0_30_TX0_P	
G1	USB0_30_TX0_N	
B33	DSI0_3_P	MIPI DSI0 lanes 2 and 3 – E1M-AEN DSI is 2-lane. Leave floating.
B34	DSI0_3_N	
C33	DSI0_2_P	
C34	DSI0_2_N	
H33	DSI1_3_P	Second MIPI DSI (DSI1) – not implemented on E1M-AEN. Leave floating.
H34	DSI1_3_N	
I33	DSI1_2_P	
I34	DSI1_2_N	
J33	DSI1_C_P	
J34	DSI1_C_N	
K33	DSI1_1_P	
K34	DSI1_1_N	
L33	DSI1_0_P	
L34	DSI1_0_N	
N33	CSI0_3_P	MIPI CSI0 lanes 2 and 3 – E1M-AEN CSI is 2-lane. Leave floating.
N34	CSI0_3_N	
O33	CSI0_2_P	
O34	CSI0_2_N	
T33	CSI1_3_P	Second MIPI CSI (CSI1) – not implemented on E1M-AEN. Leave floating.
T34	CSI1_3_N	
U33	CSI1_2_P	
U34	CSI1_2_N	
V33	CSI1_C_P	
V34	CSI1_C_N	
W33	CSI1_1_P	
W34	CSI1_1_N	
X33	CSI1_0_P	

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Pin Number	Pin Name	Description
X34	CSI1_0_N	

Table 7 E1M-AEN Not-connected Pins

2.5 Reserved Pins

Pin Number	Pin Name	Description
A33, A34, AA3, AB3, AC3, AG26, AG32, AH26, AH32, D32, E32, F32, G32, H32, I32, J32, K32, L32, M32, N32, O32, P32, Q3, Q32, R3, R32, S3, T3, U3, V3, W3, X3, Y3, Z3	RSVD	Do not connect. Used for production purposes.

Table 8 E1M-AEN Reserved Pins

Warning: Several reserved pads carry module-internal signals used in production. **W3** is the identity-EEPROM supply net, tied to the module 1.8 V rail through a 0 Ω link: never drive, load or jumper it (feeding it back-feeds the whole 1.8 V domain). **U3 / V3** are the 3.3 V programming port of the on-module power controller; they are also the private I^2C bus (3.3 V open drain, 4.7 kΩ pull-ups to 3.3 V on the module) shared by the power controller and the real-time clock. Leave them open in products: only Alp Lab's programming station uses them, with MODULE_EN held low. **S3** is the Wi-Fi module reset (active low; 100 kΩ pull-up to the Wi-Fi 3.3 V rail and driven by the power controller on the module; open drain only, never drive it high) and **Q3 / R3 / T3** its debug port (SWDIO / SWCLK / log UART TX, 1.8 V, only with Wi-Fi powered). All other reserved pads are not connected on R3; leave them floating for compatibility with later revisions.

3 Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power-supply voltage, including transients	VDDIN to GND	- 0.3	5.5	V
MODULE_EN, MODULE_STBY, RTC_WAKE_N		- 0.3	5.5	V
RTC backup input +S_CAP	V(S_CAP)	–	5.5	V
Analog input voltage	V(ANA_Sx)	- 0.3	1.98	V
Digital IO (1V8)		- 0.3	1.98	V
CAN0H/CAN0_TX, CAN0L/CAN0_RX, CAN_STBY – standard build, CAN PHY not fitted (1.8 V SoC logic)		- 0.3	1.98	V
CAN bus voltage (CAN0H / CAN0L) – CAN PHY assembly option only	V(CANx)	- 58	+58	V
Ethernet MDI (TD±, RD±)	V(MDI)	- 0.3	+4	V
Backlight output BL_LED_A (driven by the module; never apply an external voltage)	V(BL_LED_A)	–	36	V
Maximum junction temperature	T_J	- 40	+150	°C

Table 9 E1M-AEN Absolute Maximum Ratings

Warning: Stresses beyond Absolute Maximum Ratings may cause permanent damage. Operation at these conditions is not implied. The module has no input protection on VDDIN (on-module regulators are rated 6.0 V absolute maximum, input capacitors 6.3 V): the carrier board must provide over-voltage protection (a TVS ahead of an eFuse with over-voltage cutoff; a

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5 V TVS alone clamps well above 6 V) and inrush limiting, and keep VDDIN at or below 5.5 V including transients. Never apply a voltage to a 1.8 V pad while VIO_OUT is low (back-powering, see Section 6); MODULE_EN, MODULE_STBY and RTC_WAKE_N are 5 V tolerant and exempt.

3.2 Recommended Operating Conditions

The module is specified to meet the Electrical Characteristics in Section 3.3 over the conditions below. Operation outside this range is not guaranteed.

Parameter	Symbol	Min	Typ	Max	Unit
Module supply voltage	VDDIN	4.75	5.0	5.25	V
VDDIN rise time, 0 V to 4.75 V, monotonic	t_R	–	–	40	ms
VDDIN source capability, continuous / peak	I_{SRC}	1.0 / 1.5	–	–	A
VDDIN hold-up capacitance (effective, per A of total load on the VDDIN node)	C_{HOLD}	50	–	–	µF/A
Ambient operating temperature	T_A	- 40	–	+75	°C
Relative humidity (operating, non-condensing)	RH	TBD	–	TBD	%

Table 10 E1M-AEN Recommended Operating Conditions

Note: The standard module is rated − 40 °C to +75 °C ambient; the +75 °C limit is set by the Ensemble SoC. The usable ambient is further reduced by module self-heating, which depends on the workload and the carrier (see Thermal Characteristics). The backup element the carrier connects to +S_CAP sets the temperature range over which the RTC keeps time without 5 V (Section 4.2). A room-temperature assembly option with an on-module RTC backup supercapacitor is rated − 20 °C to +60 °C; contact Alp Lab.

3.3 Electrical Characteristics

Symbol	Description	Min	Nom	Max	Unit
Power supply					
I_{DDMAX}	Maximum I_{DD} current, module loads (compute + Wi-Fi TX coincident peak, calculated); carrier loads on SD_VDD, VIO_OUT, +V_CAM0/1 and the backlight add to this	–	–	834	mA
VIO_OUT (P1, P2), output only					
V_{VIO}	Output voltage	–	1.8	–	V
I_{VIO}	Load current	–	–	100	mA
$I_{VIO,START}$	Load current in the first 2 ms after VIO_OUT rises	–	–	50	mA
C_{VIO}	Carrier capacitance on VIO_OUT	–	–	2.5	µF
MODULE_EN, MODULE_STBY (5 V tolerant)					
V_{OH}	Carrier push-pull high level (if not open drain); 1.8 V, 3.3 V and 5 V logic all qualify	1.45	–	5.5	V
V_{OL}	Carrier low level at the E1 pin, at 3.3 µA	–	–	0.4	V
I_{LKG}	Carrier leakage when released (TVS included)	–	–	0.1	µA

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Symbol	Description	Min	Nom	Max	Unit
V_{REL}	Pin level when released (module-only level; never above 1.8 V)	1.2	–	1.5	V
I_{LOW}	Current sunk by the pin while held low	–	1.8	–	µA
RTC backup input (+S_CAP, AG15)					
$I_{LKG,CAP}$	Total carrier leakage on the pad (ESD diode, holder)	–	–	10	nA
R_{CHG}	Charge resistance of the RTC trickle charger at its 15 kΩ setting, internal Schottky diode included (the module adds 1 kΩ in series from the 3.3 V always-on rail), when firmware enables the charger (supercapacitor only)	12.5	15.5	17.4	kΩ
V_{CHG}	Supercapacitor voltage after charging by the module	–	3.05	–	V
$V_{TH,BKP}$	Store voltage above which the RTC runs from +S_CAP without VDDIN, with the RTC backup switchover set to Level Switching Mode; below it the clock stops	1.8	2.0	2.2	V
Analog inputs					
V(AINx)	Input voltage	0	–	1.8	V
Digital IOs (1.8 V LVCMOS)					
V_{OL}	Low-level output voltage (at rated I_{OL})	–	–	0.4	V
V_{OH}	High-level output voltage (at rated I_{OH})	1.4	–	–	V
V_{IL}	Low-level input voltage	–	–	0.63	V
V_{IH}	High-level input voltage	1.17	–	–	V
Adjustable LDO outputs (+V_CAM0 / +V_CAM1)					
+V_CAM0	Adjustable LDO output (TLV77201)	0.6	–	3.1	V
+V_CAM1	Adjustable LDO output (TLV77201)	0.6	–	3.1	V
I_{CAM}	Load current, +V_CAM0 + +V_CAM1 combined	–	–	170	mA
$I_{CAM,3V1}$	Load current per rail at a 3.1 V setting	–	–	100	mA
V_{FB}	CAM_VFB0 / CAM_VFB1 feedback reference; $V_{OUT} = V_{FB} \times (1 + R_{TOP} / R_{BOT})$ with the divider on the carrier	0.585	0.6	0.615	V
I_{FB}	Feedback-pin input current (T_J - 40 °C to +85 °C)	–	10	100	nA
I_{DIV}	Carrier divider current, $V_{OUT} / (R_{TOP} + R_{BOT})$	2	–	–	µA
C_{FF}	Optional feed-forward capacitor across R_{TOP}	0	–	100	pF
C_{CAM}	Carrier capacitance per rail (effective)	–	–	37	µF

Table 11 E1M-AEN Electrical Characteristics

Note: Digital IO levels assume 1.8 V LVCMOS signalling ($V_{IL} \le 0.35 \cdot VDDIO$, $V_{IH} \ge 0.65 \cdot VDDIO$). Confirm against the final Alif Ensemble SoC datasheet revision for the configured drive strength.

3.4 ESD & Latch-up Ratings

ESD ratings apply at module-level — i.e. directly to the LGA pads as exposed to a carrier-board assembly process. The values below reflect the Ensemble SoC silicon ratings as seen at the LGA pads. Pads wired directly to another on-module device carry that device's rating, which can be lower: the Ethernet LED pads ETH0_LED0 (AG31) and ETH0_LED1 (AH31) connect directly to the DP83825 PHY (± 1.5 kV HBM). With the exception of the SDIO / SD-card interface — which retains on-module ESD protection

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— the module does not integrate interface ESD or EMI protection; the carrier board must provide external ESD/EMI protection on all exposed external-facing interfaces, as described in the relevant interface sub-sections. The HFXO / LFXO clock pins are not exposed on the module.

Parameter	Standard	Min	Max	Unit
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001	± 2000	–	V
Charged Device Model (CDM)	ANSI/ESDA/JEDEC JS-002	± 250	–	V
Latch-up	JESD78	± 50	–	mA

Table 12 E1M-AEN ESD & Latch-up Ratings

3.5 Thermal Characteristics

The E1M-AEN dissipates heat primarily through the Ensemble SoC. The thermal-resistance figures below are the Ensemble SoC package values (FBGA194, junction-to-free-air in natural convection per the Alif datasheet); the realised module-level performance additionally depends on carrier-board copper area, airflow, and via stitching. Maximum junction temperature is the Ensemble SoC operating limit (absolute maximum +150 °C, see Section 3.1).

Parameter	Symbol	Typ	Max	Unit
Thermal resistance, junction-to-ambient (still air)	θ_{JA}	21.1	–	°C/W
Thermal resistance, junction-to-case	θ_{JC}	17.0	–	°C/W
Maximum junction temperature	$T_{J,max}$	–	+105	°C
Power dissipation derating, 50 × 50 mm carrier (estimated, see Figure 8)	P_D	67	–	mW/°C

Table 13 E1M-AEN Thermal Characteristics

The module-level thermal resistance depends on the carrier. Solder all 49 GND pads, each with at least one via to a solid GND plane; a carrier with ≥ 4 layers and ≥ 50 × 50 mm of connected GND copper gives a module-to-ambient thermal resistance of about 15 °C/W (estimated). Continuous Wi-Fi transmission combined with full compute load is the hottest use case; the application should cap Wi-Fi transmit power and duty at high temperature. Limit the backlight LED power to ≤ 0.8 W.

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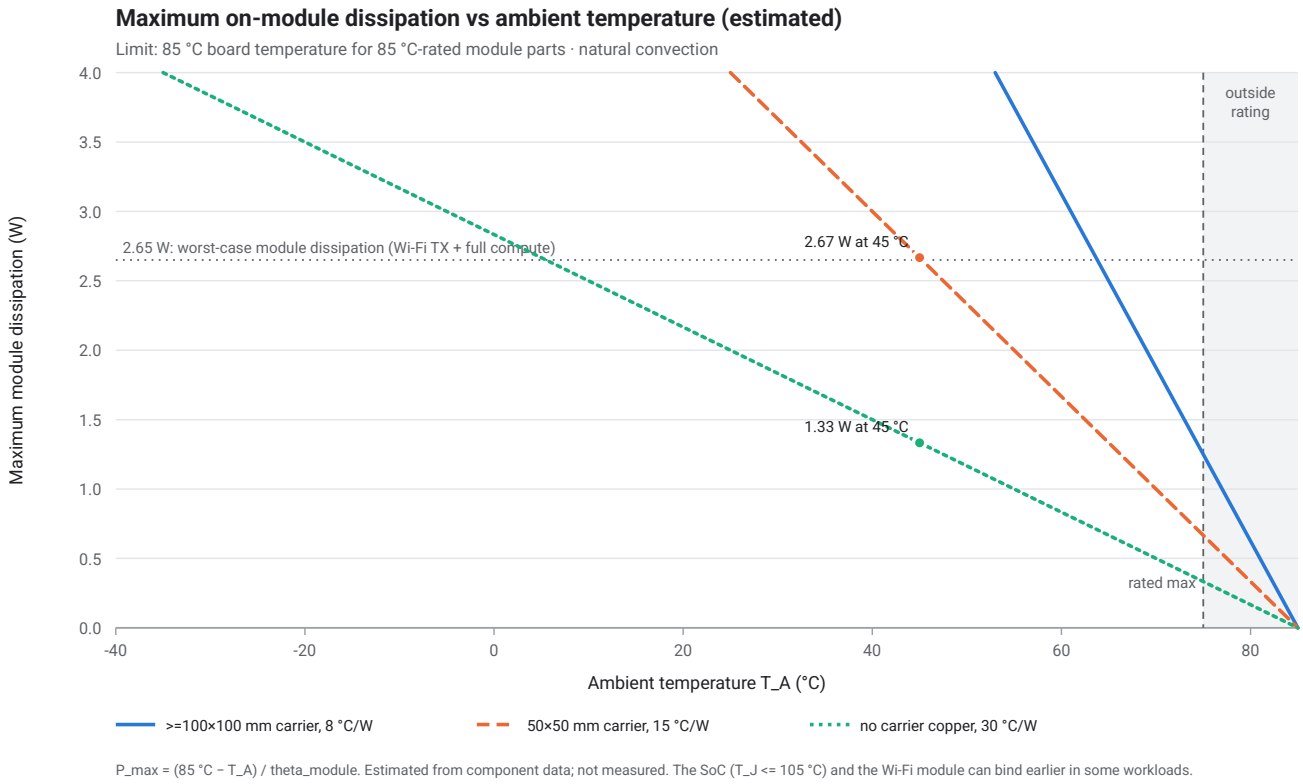


Figure 8 E1M-AEN Power-dissipation Derating (estimated)

4 Power

4.1 Power Architecture

All power rails on the module are generated and managed on-board from a single externally-supplied 5 V input on the VDDIN pads. The carrier board supplies the 5 V input and does not need to sequence any power rails.

The module power tree is split into three domains:

- **Always-on domain**, alive whenever 5 V is present: nano-power 3.3 V and 1.8 V regulators, the real-time clock (RV-3028) with its backup input +S_CAP for a carrier-side backup store (see Section 4.2), and a programmable power controller. The power controller filters MODULE_EN and MODULE_STBY, holds the module power latch, sequences the SoC supplies and PORn, and switches the Wi-Fi and SD card supplies on request from firmware.
- **SoC domain**: nano-power buck regulators for the SoC and the 1.8 V I/O rail (VIO_OUT), with an on-module brownout supervisor (2.9 V threshold on the 3.4 V SoC supply) that holds PORn low when the supply falls (R2 modules have no supervisor; see Section 1.4). It is off in self-off and when MODULE_EN is held low.
- **Switched islands**: the Wi-Fi / BLE module, the Ethernet PHY, the OSPI memories, the SD card supply and the camera LDOs each have their own switch and are off until firmware enables them. Firmware enables and parks them as the application uses each function; Alp SDK™ support for R3 power control is planned for a release after v0.17.0.

Because the module can switch itself off while MODULE_EN is high, VIO_OUT is the carrier's indication that the module is powered.

The E1M-AEN includes all necessary decoupling capacitors. Additional decoupling capacitors on the carrier board may improve performance further.

The module exposes the following regulated output rails to the carrier:

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Rail	Pins	Voltage	Max current	Purpose
VIO_OUT	P1, P2	1.8 V	100 mA	I/O reference for carrier-side level shifters. Output only; ≤ 2.5 µF carrier load.
+V_CAM0	Z34	0.6 – 3.1 V (adj.)	170 mA combined	Adjustable LDO (TLV77201), set via CAM_VFB0, switched by firmware. Camera rail or general-purpose carrier load.
+V_CAM1	AB34	0.6 – 3.1 V (adj.)		Adjustable LDO (TLV77201), set via CAM_VFB1, switched by firmware. Camera rail or general-purpose carrier load.
SD_VDD	AH10	3.4 V	212 mA	SD card supply, switched by firmware. No current limit on the module: a short on SD_VDD resets the module repeatedly. Protect the card socket on the carrier.

Table 14 Module Output Rails

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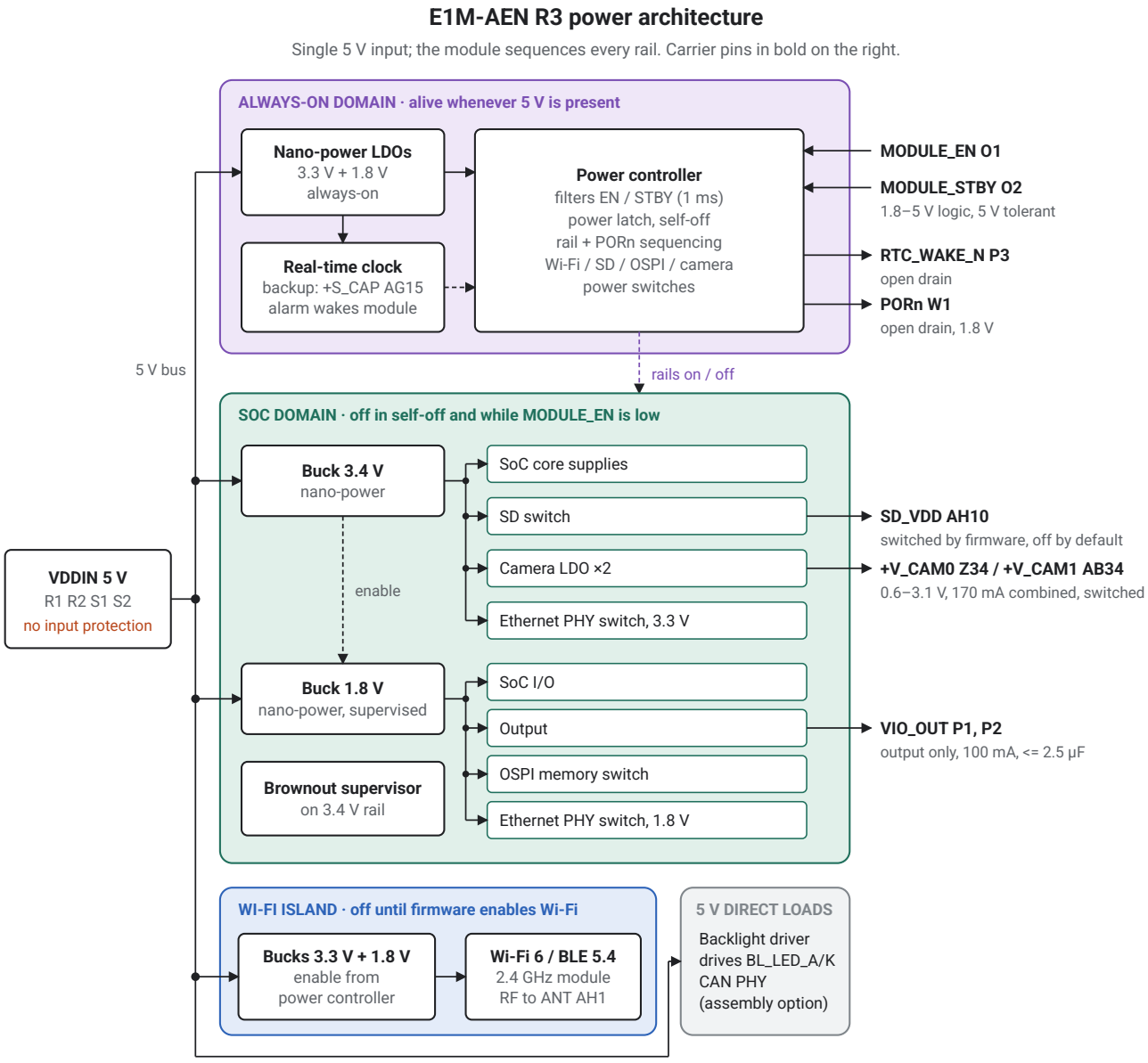


Figure 9 E1M-AEN Power Architecture

4.2 RTC Backup

The real-time clock runs from the module's always-on 3.3 V rail whenever 5 V is present. Without 5 V it needs a backup store, which the carrier provides on +S_CAP (AG15). The module has no backup element of its own in the standard build. Choose the store for the temperature range of the product; the carrier's element sets the range over which the clock keeps time without 5 V.

Backup	Carrier part	RTC trickle charger	Notes
Coin cell	BR-type primary lithium cell, rated − 40 °C to +85 °C, with a 100 Ω–1 kΩ series resistor between the cell and +S_CAP	**Disabled**	Keeps time for years without 5 V. The series resistor limits the cell current if a solder fault shorts the supply pins.
Supercapacitor, up to ≈ 100 mF	Supercapacitor rated ≥ 3.3 V and for the product's temperature range (standard parts are room-temperature products)	Enabled by firmware, 15 kΩ only	The module charges it through 15 kΩ to about 3.05 V; no charging circuit or other source is needed on the carrier. Example: 47 mF reaches 2.0 V in about 13 min and

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Backup	Carrier part	RTC trickle charger	Notes
			keeps time for about 4.6 days at 25 °C.
Supercapacitor, larger than ≈ 100 mF	Supercapacitor plus a carrier charger: 1 kΩ from the carrier 3.3 V rail and a low-leakage silicon diode to +S_CAP (not a Schottky)	**Disabled**	The module charger at 15 kΩ is too slow for a large store (470 mF takes about 2 h to reach 2.0 V). Example: 470 mF keeps time for about 30–40 days at 25 °C.
None	Tie +S_CAP to GND through 10 kΩ (RTC manufacturer recommendation); do not leave it floating	Disabled	Time is lost when 5 V is removed.

Table 15 RTC Backup Options

The figures in this section assume that firmware sets the RTC backup switchover to Level Switching Mode (LSM). The RTC then runs from +S_CAP only while the store is above about 2.0 V (2.2 V worst case); below that the clock stops. Size a supercapacitor from the backup time the product needs: about 2.3 h per mF between 3.05 V and 2.0 V at 25 °C (typical RTC backup current 115 nA plus 10 nA leakage), at least 1.5 h per mF at the RTC's maximum backup current of 180 nA, and much less at high temperature. Keep the total leakage on +S_CAP (ESD diode, holder, charger diode, board) ≤ 10 nA.

> **Warning:** Never enable the RTC trickle charger with a primary lithium cell fitted: the cell can leak, vent or burst. Firmware must configure the backup type to match the part on the carrier: trickle charger off for a coin cell or no store, on (15 kΩ charge path, never a lower value) only for a supercapacitor charged by the module. Never fit a carrier charger together with a coin cell. Alp SDK™ support for this setting follows R3 support in a later release; until then, configure the RTC trickle charger in your own firmware before fitting a cell.

4.3 Power-Up & Reset Sequence

No power-rail sequencing is required; the on-module power controller handles rail bring-up. The steps below are the recommended carrier-side bring-up order:

1. First, apply 5 V to VDDIN with MODULE_EN released. A carrier that wants the module to stay off holds MODULE_EN low before 5 V arrives.
2. Then wait for VIO_OUT high and PORn high: typically 206 ms, at most 290 ms after 5 V is applied or MODULE_EN is released.
3. Only then drive the E1 pads and begin communication with the module.

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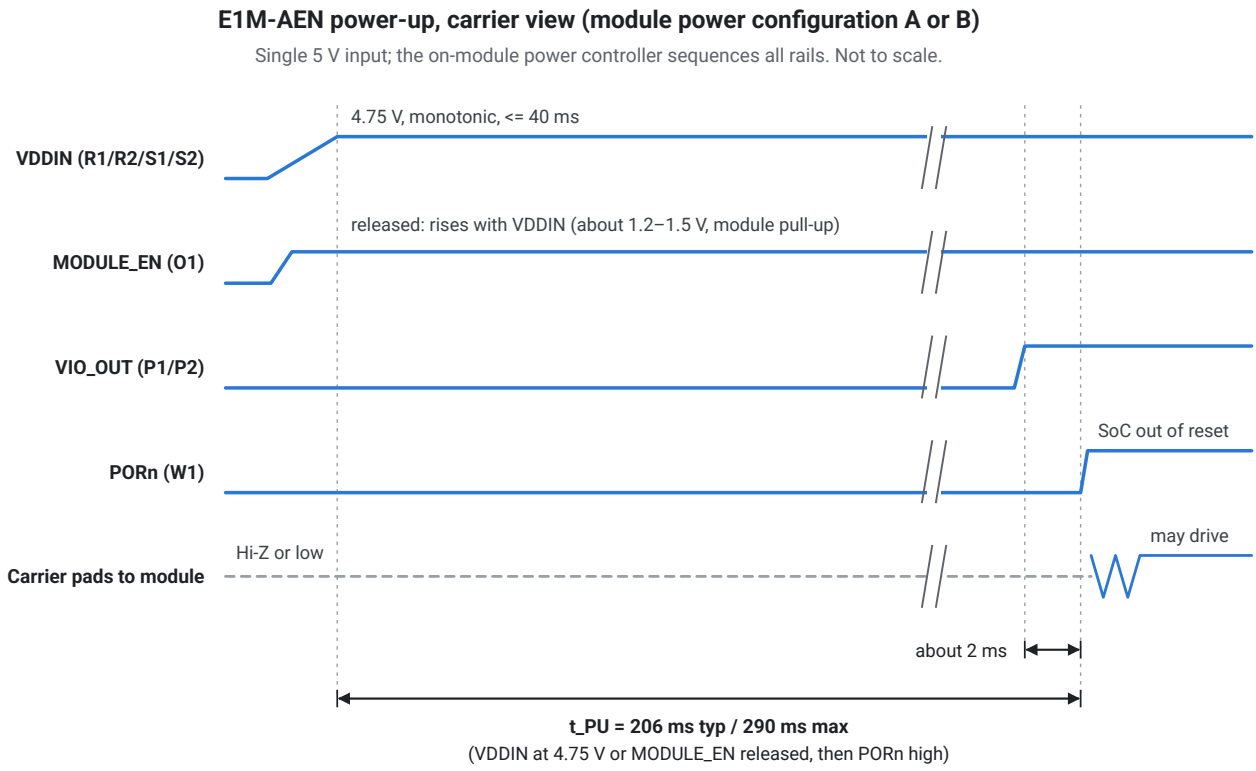


Figure 10 E1M-AEN Power-Up Timing (module level)

For power-down, first switch the module off (graceful power-off, see Section 6, or `MODULE_EN` low when the data does not matter) and wait for `VIO_OUT` low. Then remove `VDDIN`. An unplanned loss of 5 V is handled by the on-module supervisor, but writes in progress are lost; the carrier hold-up capacitance in the Recommended Operating Conditions keeps the SoC reset ordered.

> **Warning:** `MODULE_EN` low is a hard power cut with no notice to firmware. A write to MRAM or to the OSPI flash in progress at that moment is lost or corrupted. Use the graceful power-off (Section 6) and keep `MODULE_EN` for recovery.

4.4 Power Consumption

Current at `VDDIN`, typical at T_A = +25 °C, VDDIN = 5.0 V, E1M-AEN801 (E8). Wi-Fi, Ethernet, OSPI memory and camera supplies are off unless the row says otherwise. Active figures depend on the Ensemble variant and software workload.

Mode	Description	Min	Typ	Max	Unit
Active					
Run, compute	All cores and NPUs active, 400 MHz ACLK	–	111	TBD	mA
Run + Wi-Fi listen	As above, Wi-Fi receiving	–	136	TBD	mA
Run + Wi-Fi TX	As above, Wi-Fi TX 6 Mbps OFDM at 18.2 dBm	–	372	TBD	mA
Run + Wi-Fi TX, coincident peak	Compute and Wi-Fi transmit peaks together	–	–	834	mA
Low-power					
Idle	Core in WFI, clocks running, any interrupt wakes	–	1.28	–	mA
Low-power standby‡	Only low-power UART / I^2C clocked	–	64	–	µA
Connected standby	STOP, Wi-Fi associated at DTIM10, wake on Wi-Fi traffic	–	304	–	µA

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Mode	Description	Min	Typ	Max	Unit
STOP	4 KB backup RAM retained, RTC running, wake armed	–	3.84	TBD	µA
STOP, MODULE_STBY held low	As STOP, level protocol	–	6.6	TBD	µA
Self-off	All module rails off, RTC running, RTC or stand-by wake armed	–	1.14	TBD	µA
Shutdown (MODULE_EN low)	Module held off by the carrier, RTC running	–	2.94	TBD	µA
No VDDIN	RTC kept by the carrier backup store on +S_CAP, if fitted	–	0	–	µA

Table 16 E1M-AEN Power Consumption (typical, calculated)

Note: Preliminary. All figures are calculated from component datasheets at 25 °C (typical) and are not yet measured on R3 hardware. Low-power currents rise steeply with temperature (estimated: STOP about 15 µA at 50 °C and about 150 µA at 85 °C; self-off about 3 µA at 50 °C and about 17 µA at 85 °C). Retaining more SoC memory in STOP raises the STOP current. The low-power figures assume the CAN PHY is not fitted (standard build). The 1.5 A peak source requirement covers all module loads, including carrier loads on SD_VDD, VIO_OUT and the camera rails. ‡ SoC low-power mode; Alp SDK™ support TBD. Standby figures include capacitor leakage. Without VDDIN the RTC keeps time only if the carrier fits a backup store on +S_CAP (Section 4.2); the retention time is set by that store.

5 Boot Modes

Alif Semiconductor SoCs have no boot-mode strap pins; the boot flow is fixed and programmed into the internal ROM. The E1M BOOT0–BOOT3 strap pins defined in the E1M™ specification are therefore **not used** on E1M-AEN and should be left floating.

The boot ROM loads the application image from MRAM. External boot sources (OSPI flash, SD card) are selected in software once the boot ROM is running.

Note: Refer to the Alif Semiconductor Ensemble series boot reference manual for the internal boot sequence and image-signing requirements.

6 Reset, Module Enable & Power Control

The carrier controls the module with VDDIN, MODULE_EN and MODULE_STBY, and reads its state on VIO_OUT, PORn and RTC_WAKE_N. All other power sequencing is inside the module.

Pin	Direction	Description
MODULE_EN (01)	Input, 5 V tolerant	Low = module forced off and held off; a low-to-high transition powers the module on from any state. Low pulses shorter than 0.5 ms are ignored. Drive open drain, open collector or a switch to GND (preferred), or push-pull from 1.8 V, 3.3 V or 5 V logic with $V_{OH} \geq 1.45$ V; $V_{OL} \leq 0.4$ V at the E1 pin. No carrier pull-up is needed. Left open, the pad sits at about 1.2–1.5 V: that level exists on the module only, so a carrier that wants to read the line back fits its own pull-up. The pin sinks about 1.8 µA while held low.
MODULE_STBY (02)	Input, 5 V tolerant	Active low, same circuit and levels as MODULE_EN. Firmware selects a pulse protocol (each falling edge is a sleep request or a wake) or a level protocol (low = stay asleep). A low pulse ≥ 10 ms also wakes the module from self-off, provided firmware armed the RTC event input before it switched the module off.

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Pin	Direction	Description
PORn (W1)	Bidirectional, open drain	SoC reset, pulled up internally to 1V8. High = SoC out of reset. Pull low for ≥ 2 ms to reset the SoC with the module rails kept up. Never drive high and do not add a carrier pull-up.
VIO_OUT (P1, P2)	Output	High = module rails up (run or STOP). Low = module off.
RTC_WAKE_N (P3, IO25)	Output, open drain	Low after an RTC alarm, timer or stand-by wake event until firmware clears the RTC flags. Valid in every state while VDDIN is present.

Table 17 Reset, Enable & Power-control Signals

Warning: MODULE_EN and MODULE_STBY accept 1.8 V, 3.3 V and 5 V logic, and are 5 V tolerant (5.5 V maximum). Keep the carrier leakage on each pin, TVS included, at or below 0.1 µA. An unpowered host pin clamps MODULE_EN to about 0.5 V through its ESD diodes and turns the module off: if the module must stay up while the host is unpowered, buffer the line with an open-drain N-MOSFET on an always-on rail. Never drive an E1 pad while VIO_OUT is low: the pad back-powers the SoC I/O ring.

6.1 Module States

State	VDDIN	MODULE_EN	VIO_OUT	PORn	I_{VDDIN} typ	Leaves the state on
No 5 V	0 V	–	low	low	0	5 V return; boots if MODULE_EN is released
Shutdown	5 V	held low	low	low	2.94 µA	MODULE_EN release only
Self-off	5 V	high or open	low	low	1.14 µA	RTC alarm or timer; MODULE_STBY low ≥ 10 ms (stand-by wake armed by firmware); MODULE_EN low ≥ 2 ms then high
Booting	5 V	high or open	rising	low, then high	mA, firmware dependent	PORn high ≈ 204 ms after the wake event
Run / connected standby	5 V	high or open	high	high	304 µA – 372 mA	firmware, MODULE_STBY, MODULE_EN
STOP	5 V	high or open	high	high	3.84 µA (6.6 µA with MODULE_STBY held low)	MODULE_STBY, RTC, Wi-Fi, IO8 / IO10

Table 18 Module States Seen from the Carrier

The carrier cannot tell run from STOP on these pins: VIO_OUT and PORn stay high in both. A carrier that needs to know uses an application line on IO8 or IO10.

6.2 Control Timing

Parameter	Min	Typ	Max	Unit
MODULE_EN low pulse that is always ignored	–	–	0.5	ms
MODULE_EN low time that always powers the module off	2	–	–	ms
MODULE_EN low time for a full power cycle	25	–	–	ms
MODULE_EN high time after a low that always boots the module	2	–	–	ms

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Parameter	Min	Typ	Max	Unit
MODULE_STBY low pulse: sleep request, or wake from STOP	2	–	–	ms
MODULE_STBY high time between pulses	2	–	–	ms
MODULE_STBY low pulse: wake from self-off	10	–	–	ms
PORn reset pulse from the carrier	2	–	–	ms
VDDIN reaching 4.75 V, or MODULE_EN released, to PORn high	–	206	290	ms
Wake event (RTC, MODULE_STBY) in self-off to PORn high	–	204	–	ms
Carrier pads Hi-Z after PORn falls (recommended)	–	–	1	ms

Table 19 Carrier Control Timing

6.3 Carrier Sequences

Sleep and wake. Pull MODULE_STBY low for ≥ 2 ms (pulse protocol) or hold it low (level protocol). The module enters STOP; VIO_OUT and PORn stay high, so the carrier keeps its pads in a defined state and stops clocking them. To wake, give a second pulse (pulse protocol) or release the pin (level protocol).

Graceful power-off. First, request it over the application link, IO8 / IO10, or a long MODULE_STBY press (firmware policy). Firmware finishes its writes, arms its wake sources and switches the module off. Next, the carrier sees PORn fall and puts its pads Hi-Z within 1 ms. Then VIO_OUT decays. If PORn is still high after the firmware's shutdown time (2 s is a sensible host timeout), fall back to the forced power-off.

Wake from self-off. Give a MODULE_STBY low pulse ≥ 10 ms (firmware must have armed the RTC event input before self-off), or pulse MODULE_EN low ≥ 2 ms and release it, or let the RTC alarm fire. RTC_WAKE_N goes low on RTC and stand-by wakes.

Forced power-off (recovery). Pull MODULE_EN low for ≥ 2 ms. Hold it low for ≥ 25 ms for a full power cycle (pulses shorter than about 21 ms reset the SoC but keep its supply up), or keep it low to hold the module off; release it to cold-boot. No notice reaches firmware (see the warning in Section 4.3).

SoC reset only. Pull PORn low for ≥ 2 ms with an open-drain output, then release it. The module rails, the RTC and the power latch stay as they are. No notice reaches firmware: an MRAM write in progress is lost or corrupted.

Configuration	MODULE_EN	MODULE_STBY	Deepest state	Notes
Always on	open	open	Self-off, RTC wake only	Boots on 5 V insertion. After self-off only an RTC alarm or a 5 V cycle (≥ 1 s off) wakes it; if firmware fails to arm a wake, only the 5 V cycle does.
One power button	open (optional recessed power-cycle button to GND: a hard power cut, see Section 4.3)	momentary button to GND	Self-off	Short press while running = sleep, long press = power off (firmware policy); press in STOP = wake; press in self-off = wake if firmware armed the stand-by wake. No carrier pull-up or debounce capacitor needed; low-leakage ESD diode only.
Host controlled	host open-drain output, or push-pull 1.8–5 V	host open-drain output, or push-pull 1.8–5 V	Shutdown (2.94 µA) or self-off	Host reads VIO_OUT and PORn for state; RTC_WAKE_N to a host wake input with a pull-up to the host always-on rail. If the host can be unpowered while the module must stay up, buffer MODULE_EN with an open-drain N-MOSFET (see the warning above).

Table 20 Reference Carrier Configurations

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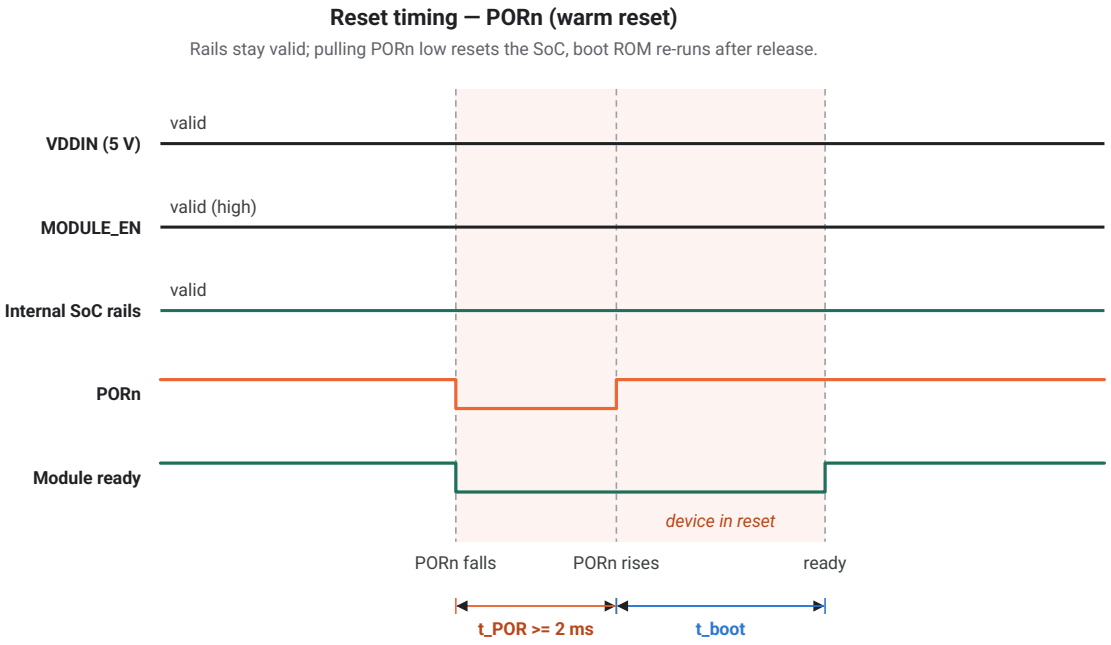


Figure 11 E1M-AEN Reset Timing (PORn warm reset)

7 JTAG / SWD Debug

The E1M-AEN exposes a 5-pin JTAG/SWD interface for programming and debug. Signals operate at 1.8 V; carrier-board level shifters are required for 3.3 V debug probes. Use VIO_OUT as the probe's target-voltage reference and disable any probe target-power output. The SE-UART (DBG_TX / DBG_RX, AD3 / AE3) is the second programming path; expose both on development carriers.

Pin	Signal	Description
Z1	JTAG_nRST	Active-low system reset request from the debug probe, open drain. 20 kΩ pull-up to 1.8 V on the module; no carrier pull-up.
X1	JTAG_TCK / SWDCLK	Test clock (JTAG) or serial-wire clock (SWD).
X2	JTAG_TDI	Test data in (JTAG only).
Y2	JTAG_TDO	Test data out (JTAG only).
Y1	JTAG_TMS / SWDIO	Test mode select (JTAG) or serial-wire I/O (SWD).

Table 21 JTAG / SWD Pinout

> **Note:** Alp Lab recommends exposing the JTAG/SWD pins on a 10-pin Cortex-M debug header on the carrier board. Refer to the E1M Hardware Design Guide for the reference connector pinout.

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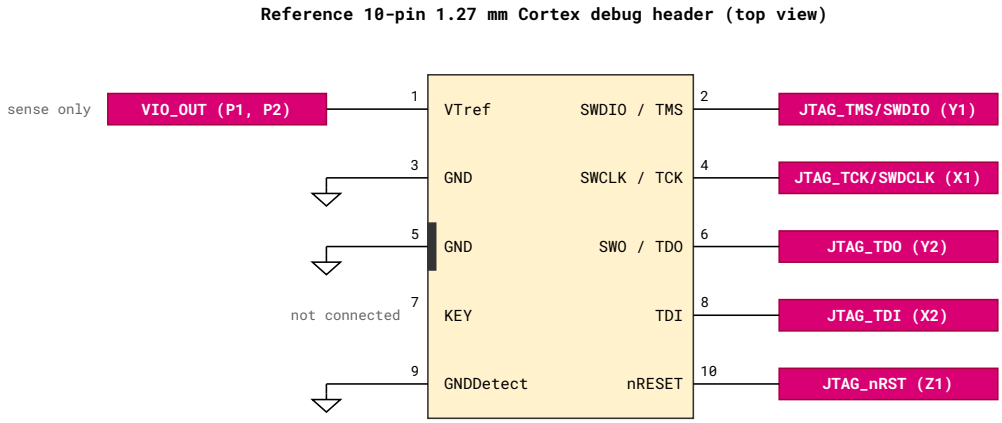


Figure 12 Reference JTAG / SWD Header Pinout

8 Interfaces

8.1 Ethernet

E1M-AEN has one 100 Mbit Ethernet PHY: the TI DP83825. The PHY answers on MDIO address 0 (address straps left at their internal pull-down default) and reports PHY identifier `0x2000a140` (PHYIDR1 = `0x2000`, PHYIDR2 = `0xa140`; the low four bits are the silicon revision). It connects to the SoC over RMII, with the 50 MHz reference clock from an on-module oscillator. The interface does not include on-module EMI or ESD protection; the user must provide an external magnetics transformer, connector, and EMI/ESD protection on the carrier board.

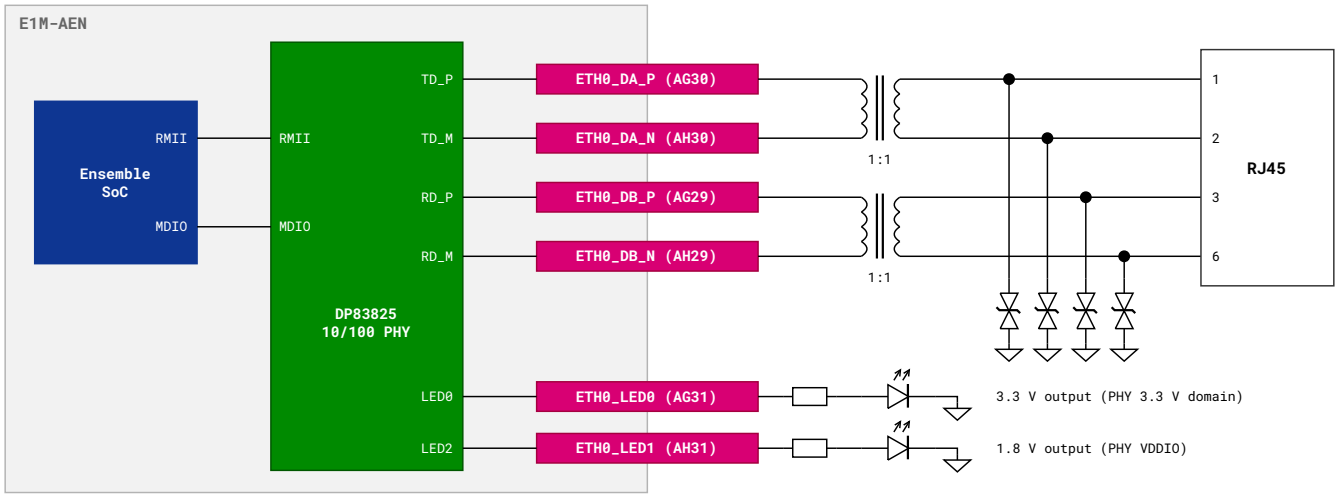


Figure 13 E1M-AEN Ethernet Connection

The PHY is configured as follows:

Function	Setting	Description
Auto-Negotiation	Enabled	Auto-Negotiation is enabled by default. ETH0_LED0 (AG31) is the DP83825 LED0 pin and also its auto-negotiation-disable strap. ETH0_LED1 (AH31) is the DP83825 50MHzOut/LED2 pin (LED2 in the module's RMII follower mode) and also its RX_DV-enable strap; strapped high, it turns the RMII CRS_DV pin into RX_DV and breaks the link to the SoC. Both straps default low through the PHY's internal pull-downs and must read below 0.6 V at PHY reset: never

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Function	Setting	Description
		pull these pads up on the carrier, and drive LEDs active high (pad, resistor, LED, GND). ETH0_LED0 swings to 3.3 V (PHY 3.3 V domain) and ETH0_LED1 to 1.8 V (PHY VDDIO): never connect ETH0_LED0 to a 1.8 V-only input, and use a transistor or buffer for an LED on ETH0_LED1 whose forward voltage is near or above 1.8 V.
Auto MDI/MDIX	Enabled	Auto-MDIX is enabled by default.

Table 22 Ethernet PHY Configuration

Note: The DP83825 MDI pins (TD±, RD±) are rated ± 5 kV HBM (ANSI/ESDA/JEDEC JS-001); all other PHY pins, including ETH0_LED0 and ETH0_LED1, are rated ± 1.5 kV HBM. These are component handling ratings, not IEC 61000-4-2 system ratings: external magnetics, connector, and IEC 61000-4-2 ESD protection are required on the carrier board.

Note: Software status (Alp SDK™ v0.17.0): there is no Alp SDK chip driver for the PHY (driver status “none”), so there is no ALP_SDK_CHIP_DP83825 configuration symbol. The Ethernet link and a DHCP lease are demonstrated on E8 silicon by the example examples/aen/aen-ethernet-link. The managed-MDIO path (MDIO_DWMAC_ALIF with the upstream phy_ti_dp83825 driver) has been exercised at the MDIO layer only; link and traffic over it are not yet proven.

8.2 USB

E1M-AEN has one USB 2.0 interface. It supports Full-Speed (12 Mbit/s) and High-Speed (480 Mbit/s) bit rates and can operate as device or host.

Pin Number	Pin Name	Peripheral	Description
B1	USB0_30_D_P	USB0	Route USB0_30_D_P and USB0_30_D_N as a differential pair with 90 Ω impedance.
C1	USB0_30_D_N		
D2	USB0_30_ID		Low: Host mode. NC: Device mode.
C2	USB0_VBUS		Connect to USB VBUS 5 V.

Table 23 E1M-AEN USB Interface

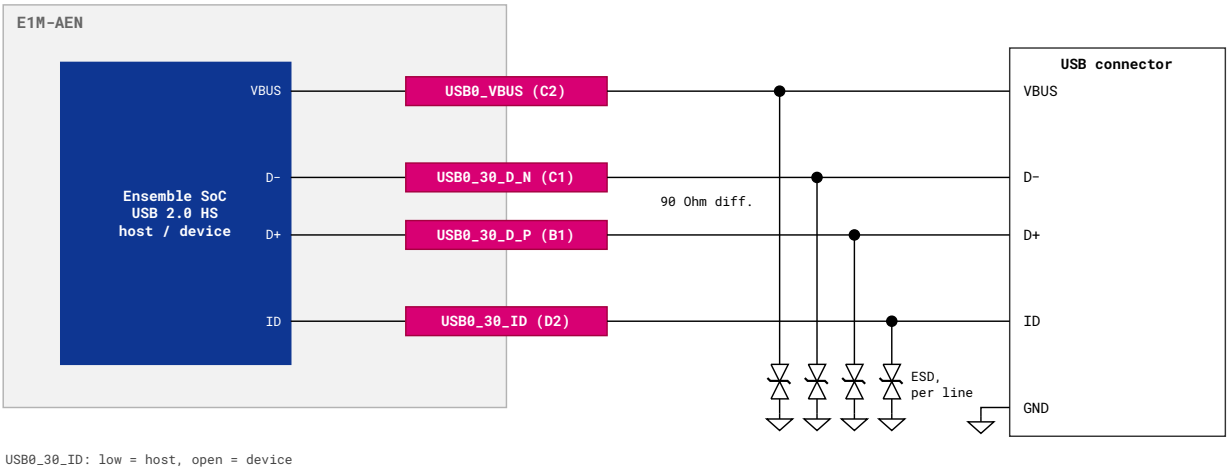


Figure 14 E1M-AEN USB 2.0 Carrier Connection

Note: The USB pads connect directly to the Ensemble SoC USB 2.0 PHY. The module has no USB ESD protection and no VBUS switch. Add a low-capacitance ESD array at the connector on USB0_30_D_P, USB0_30_D_N, USB0_VBUS and USB0_30_ID, and route the data pair as a 90 Ω differential pair.

Note: On R3 the USB 2.0 interface is on the E1M standard USB0 pads B1 / C1 / C2 / D2. The USB2 pads (I1 / J1 / I2 / J2) and the USB0 SuperSpeed lanes are not connected and must be left floating. On R2 modules USB 2.0 is on the USB2 pads (Section 1.4).

8.3 Serial Interfaces

8.3.1 I²C

E1M-AEN exposes two I²C interfaces: I²C0 (I2C0_SDA AD2, I2C0_SCL AE2), which also carries the on-module identity EEPROM, and I²C1 (I2C1_SDA AH17, I2C1_SCL AG17). Refer to the Alif Semiconductor Ensemble series datasheet for full details. The module has no pull-ups on these pads: pull SDA and SCL up to VIO_OUT (1.8 V) on the carrier, for example 4.7 kΩ on I²C0 (see Identity EEPROM and I²C0). Never pull them up to 3.3 V.

8.3.2 I³C

E1M-AEN exposes one I³C interface (I3C_SDA AH5, I3C_SCL AG5). Refer to the Alif Semiconductor Ensemble series datasheet for full details. The module has no pull-ups on these pads: pull I3C_SDA up to VIO_OUT (1.8 V) on the carrier. The I³C controller drives I3C_SCL push-pull, so a pull-up on I3C_SCL is optional.

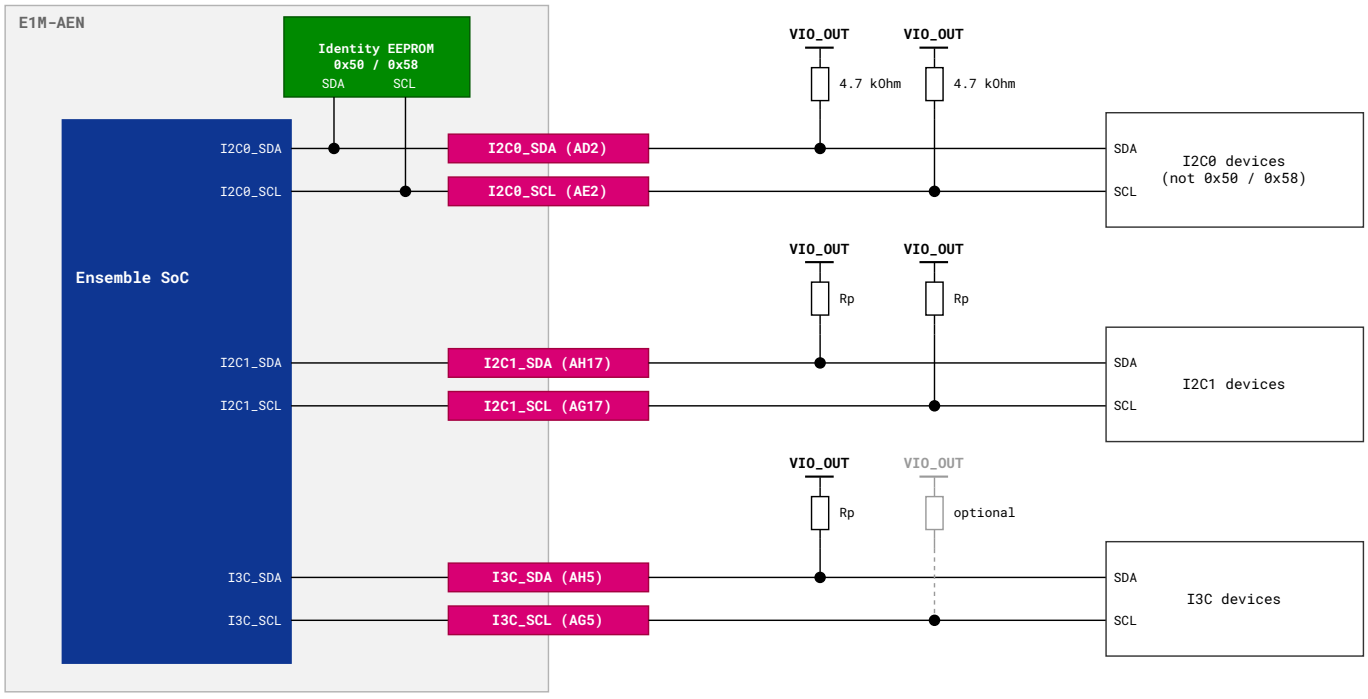


Figure 15 E1M-AEN I²C / I³C Carrier Pull-ups

8.3.3 UART

E1M-AEN exposes two UART interfaces. Refer to the Alif Semiconductor Ensemble series datasheet for full details.

Note: Both UART interfaces (UART0 on F2 / G2, UART1 on AG4 / AH4) are driven directly by the Ensemble SoC. The SE-UART (DBG_TX / DBG_RX) is separate; see JTAG / SWD Debug.

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8.3.4 SPI

E1M-AEN exposes two SPI interfaces. Refer to the Alif Semiconductor Ensemble series datasheet for full details.

SPI0 (SPI0_SCLK N2, SPI0_MOSI M2, SPI0_MISO L1, SPI0_CS0 M1, SPI0_CS1 N1) is driven directly by the Ensemble SoC at 1.8 V.

Note: SPI1 (AG8, AG9, AG10, AH8, AH9) is the SPI interface of the on-module Wi-Fi / BLE module, not of the Ensemble SoC. It is valid only while Wi-Fi is powered. Never drive these pads while Wi-Fi is off, and avoid pull-ups on them (if one is unavoidable, use ≥ 100 kΩ to VIO_OUT).

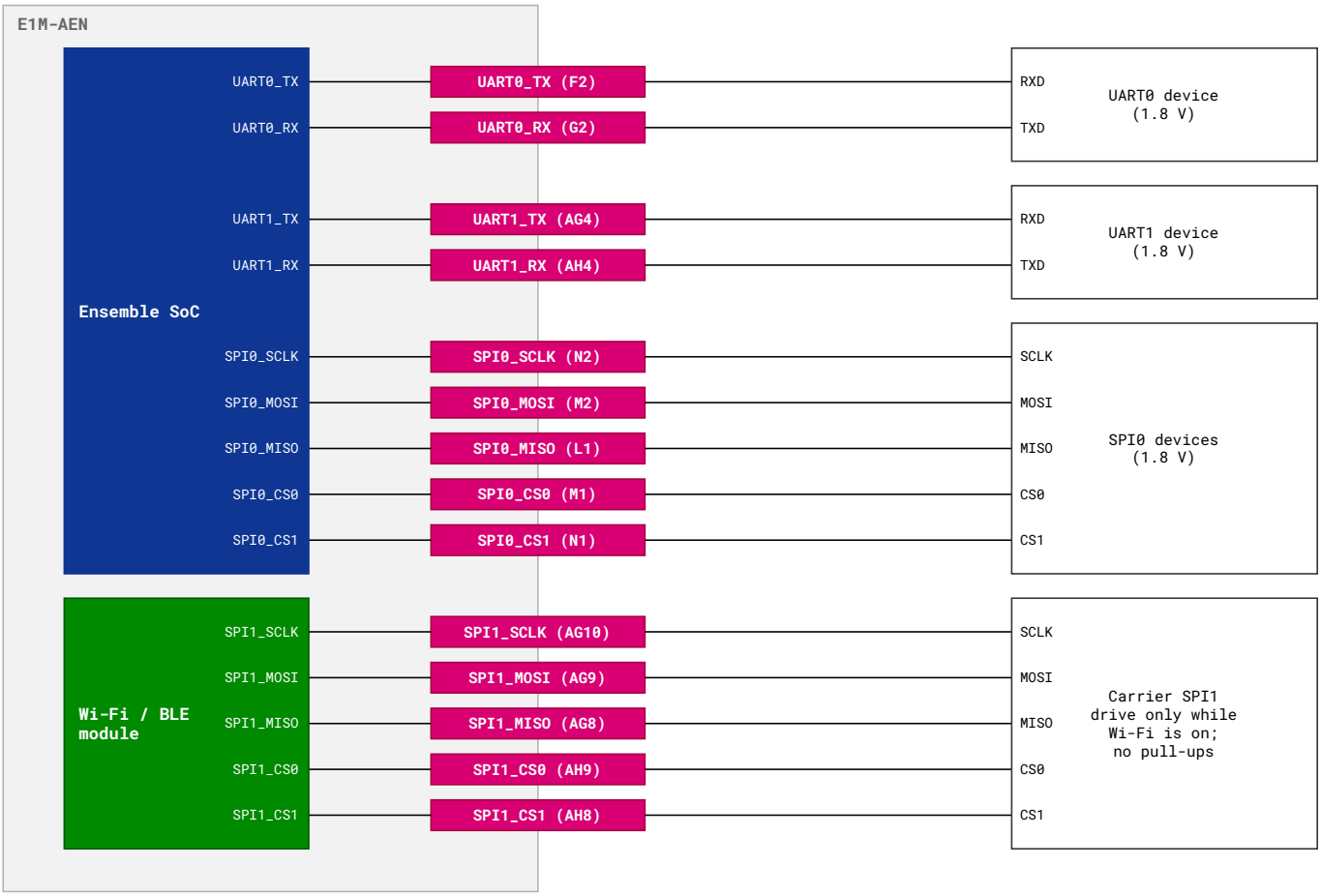


Figure 16 E1M-AEN UART and SPI Pads

8.3.5 I²S

E1M-AEN exposes two I²S interfaces. Refer to the Alif Semiconductor Ensemble series datasheet for full details.

8.3.6 CAN Bus

E1M-AEN includes an optional CAN-BUS PHY (TI TCAN1044AVDRBRQ1, assembly option) to simplify carrier-board hardware design.

Warning: In the standard build the CAN PHY is **not fitted**: CAN0H/CAN0_TX (B18) and CAN0L/CAN0_RX (B19) are then the SoC CAN TX / RX signals at 1.8 V (Digital IO absolute maximum 1.98 V), and the carrier must provide a CAN transceiver. Never connect a CAN bus directly to B18 / B19 on a module without the PHY: this permanently damages the SoC. The ± 58 V bus rating applies only to modules with the PHY fitted.

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On modules with the PHY fitted, the PHY runs from VDDIN and is not included in the low-power figures; the carrier must not pull CAN_STBY (A19) low, because low selects the PHY normal mode (several mA), and must add termination, ESD, and EMI protection components on the carrier board.

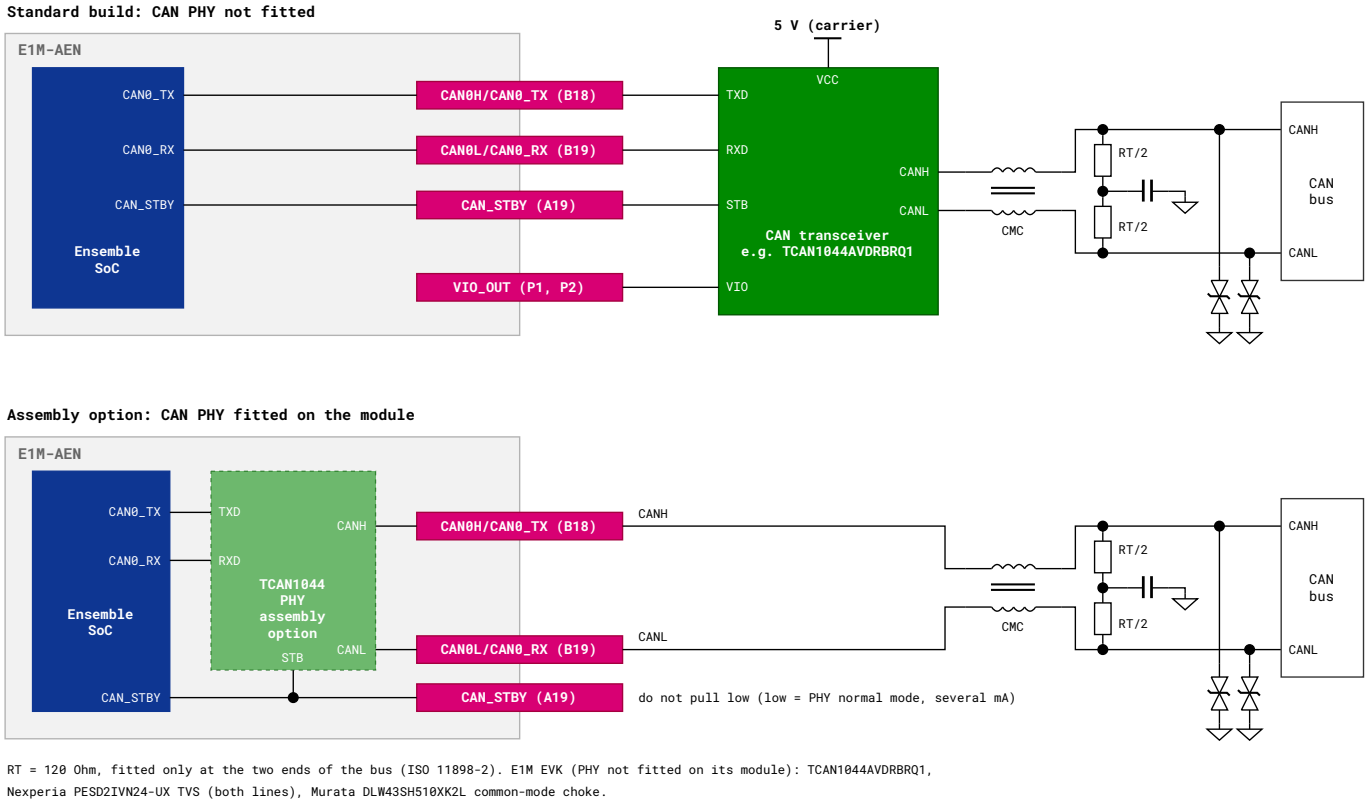


Figure 17 E1M-AEN CAN Connection: Standard Build and CAN PHY Assembly Option

> **Note:** The TCAN1044AVDRBRQ1 bus pins withstand ± 8 kV unpowered contact discharge and ± 15 kV air discharge per ISO 10605.

8.4 Wireless Module & Antenna

E1M-AEN includes an on-board BDE-BW3501N 2.4 GHz Wi-Fi 6 and Bluetooth LE 5.4 combo module, based on the Texas Instruments SimpleLink™ CC3501E wireless MCU SoC. The module is backward-compatible with 802.11 b/g/n. Its single-stream radio supports 20 MHz channels with application throughput up to 20 Mbps (UDP), and WPA / WPA2 / WPA3 personal and enterprise security. In the standard build the module ANT output is brought out to the ANT_2.4GHZ pad (AH1).

The Wi-Fi / BLE module has its own supplies, which are off until firmware enables Wi-Fi; between uploads the radio can be switched fully off. The Wi-Fi module GPIOs on the E1 pads (Section 2.3) are valid only while Wi-Fi is powered.

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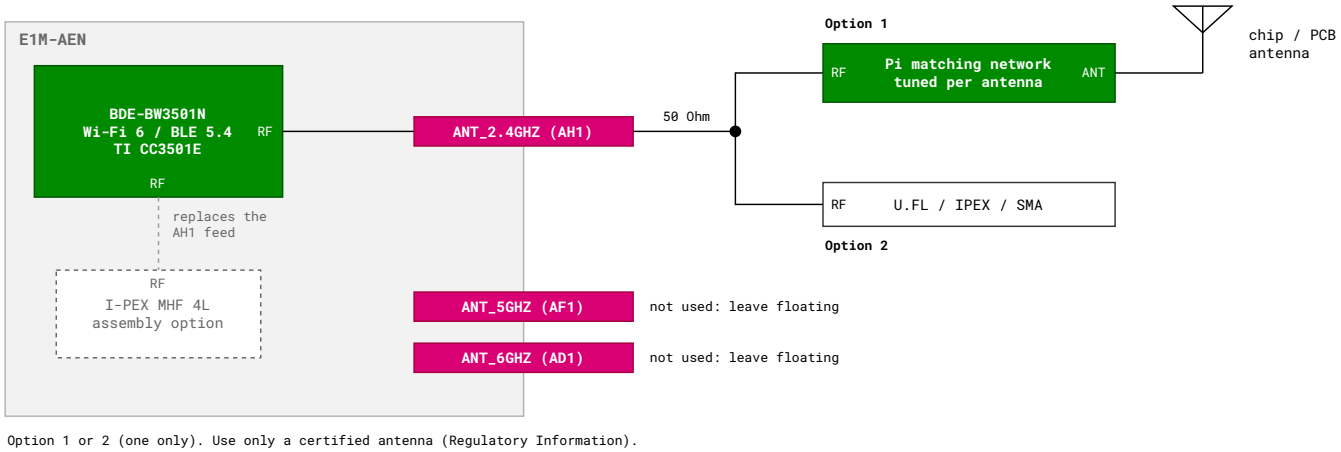


Figure 18 E1M-AEN Antenna Connection

8.4.1 RF Characteristics

Symbol	Description	Min	Typ	Max	Unit
Wi-Fi 6 (802.11ax, 2.4 GHz)					
f_{op}	Operating frequency range	2412	–	2472	MHz
P_{TX}	TX output power (HE MCS0)	–	18.2	–	dBm
P_{TX}	TX output power (HE MCS7)	–	15.7	–	dBm
P_{RX}	RX sensitivity (HE MCS0, 4K)	–	-89	–	dBm
P_{RX}	RX sensitivity (HE MCS7, 4K)	–	-70	–	dBm
η	Max application throughput (UDP)	–	20	–	Mbps
Bluetooth LE 5.4					
f_{op}	Operating frequency range	2402	–	2480	MHz
P_{TX}	TX output power (max setting)	–	16.3	–	dBm
P_{RX}	RX sensitivity (LE 1M, 37-byte)	–	-97.5	–	dBm
P_{RX}	RX sensitivity (LE Coded, 125 kbps)	–	-103.5	–	dBm

Table 24 E1M-AEN Wi-Fi 6 / BLE RF Characteristics

> **Note:** Radio figures are BDE-BW3501N module specifications (typical, averaged across all channels). Values at the carrier-board antenna are reduced by trace and connector losses; the path from the wireless module through AH1 to the carrier adds about 0.12 dB at 2.45 GHz with a return loss of about − 21 dB (simulated, not measured; copper loss not included, expect about 0.1–0.15 dB more).

8.4.2 Antenna Options

The E1M-AEN antenna port can be routed three ways:

1. **Carrier-board PCB antenna** (standard build) — route the ANT_2.4GHZ pad (AH1) out as a 50 Ω controlled-impedance coplanar trace to a chip or PCB antenna on the carrier board. Surround the AH1 landing with GND and place a pi matching network next to the antenna.
2. **Carrier-board RF connector** (standard build) — extend the 50 Ω trace to a U.FL / IPEX / SMA connector on the carrier board.
3. **On-module I-PEX MHF 4L connector** (assembly option) — the RF output is routed to the on-module connector instead of AH1. Contact Alp Lab for this assembly variant.

Maximum antenna gain to maintain regulatory compliance is TBD dBi.

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8.4.3 Regulatory Information

The on-module Wi-Fi 6 / BLE 5.4 combo is pre-certified for the regions listed below. Reusing the module's certifications on the customer's end product requires following the integration guidelines in the relevant certification reports.

Region	Standard	Certificate ID	Notes
United States	FCC Part 15	TBD	Modular grant pending.
Europe	RED / CE	TBD	–
Canada	ISED RSS-247	TBD	–
Japan	MIC (Japan)	TBD	–

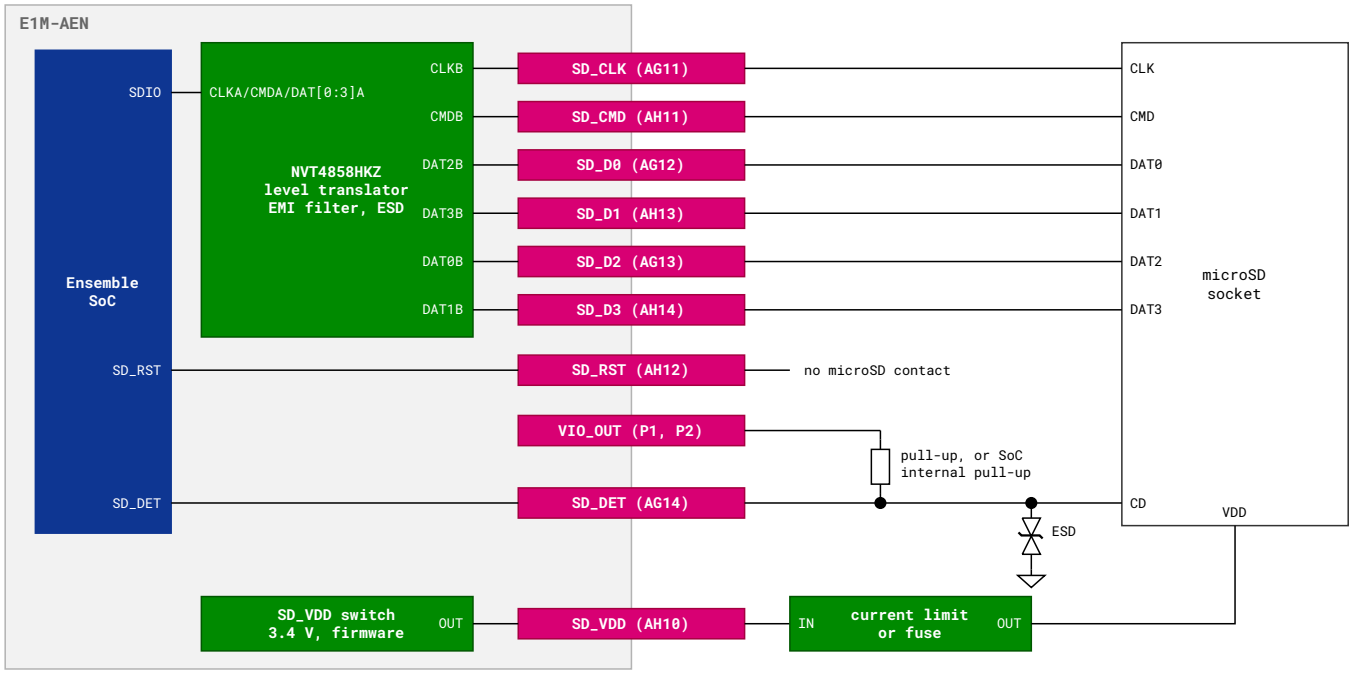
Table 25 Wireless Regulatory Approvals

Note: The on-module BDE-BW3501N wireless module is rated for ± 4 kV contact-discharge and ± 8 kV air-discharge ESD per EN 301-489. This is a module-level figure for the wireless subsystem; E1M-AEN pad-level HBM/CDM ratings are listed in the ESD & Latch-up Ratings table.

Warning: Certifications apply only when the module is used with the antenna(s) listed in the certification report. Using an unlisted antenna voids the modular grant and requires re-certification on the customer's end product.

8.5 SD Card

E1M-AEN supports an external µ SD card over the SDIO interface. The SDIO clock, command and data lines pass on the module through an NXP NVT4858HKZ level translator (card side at SD_VDD, 3.4 V), which integrates an EMI filter and ESD protection. SD_DET (AG14) and SD_RST (AH12) are **not** translated: they are 1.8 V SoC pads with no on-module ESD protection. Pull SD_DET up to VIO_OUT only, never to SD_VDD or 3.3 V, and add ESD protection on the carrier. A µ SD socket has no contact for SD_RST: leave it floating if it is not used.



SD_CLK, SD_CMD, SD_D0–SD_D3: connect directly; no carrier series resistors, pull-ups or ESD. SD_RST: leave floating if unused.

Figure 19 E1M-AEN SD Card Connection

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Note: The NVT4858HKZ provides IEC 61000-4-2 level 4 ESD protection: ± 8 kV contact discharge and ± 15 kV air discharge.

8.6 MIPI DSI Display & Backlight Controller

The Alif Ensemble series exposes a 2-lane MIPI DSI interface (D-PHY Tx, MIPI DSI v1.2 / D-PHY v1.2) for an external display: up to 1.25 Gbps per lane (2.5 Gbps aggregate), video mode only. The maximum panel resolution and frame rate are limited by the pixel clock and the available DSI link bandwidth (2 lanes × 1.25 Gbps); the Alif E8 datasheet v1.0 (§3.20.2) does not specify a fixed maximum display resolution. The Ensemble series also includes a 2D GPU (D/AVE) that can accelerate display rendering.

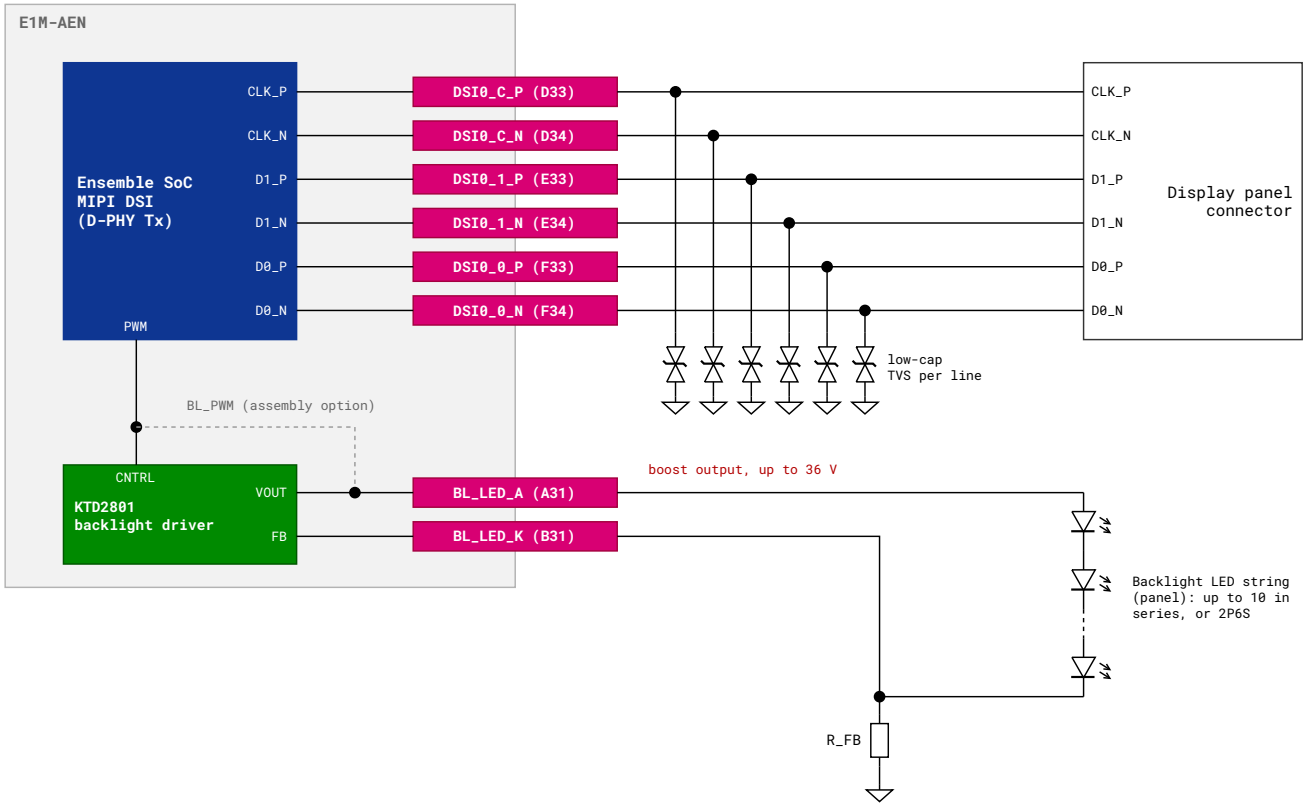


Figure 20 E1M-AEN MIPI DSI and Backlight Connection (carrier side)

The MIPI display and camera interfaces exposed on the module are summarised below.

Interface	Lanes	Rate / lane	Aggregate	Max resolution
MIPI DSI (display, D-PHY Tx)	2	1.25 Gbps	2.5 Gbps	bandwidth-limited†
MIPI CSI-2 (camera, D-PHY Rx)	2	2.5 Gbps	5.0 Gbps	up to 2 MP (1920 × 1080)

Table 26 E1M-AEN MIPI Interface Summary

Note: † The Alif E8 datasheet v1.0 (§3.20.2) specifies no fixed maximum DSI display resolution; the panel ceiling is set by the pixel clock and the 2-lane × 1.25 Gbps D-PHY Tx link bandwidth (video mode only). The 1920 × 1080 (2 MP) figure is the ISP / camera-input ceiling, not a DSI display limit.
Both interfaces conform to MIPI D-PHY v1.2. The CSI-2 host supports up to 16 interleaved virtual channels; the DSI supports bidirectional / escape mode on data lane 0. Neither interface includes on-module EMI or ESD protection — protect the lanes with a low-capacitance TVS array on the carrier board.

E1M-AEN has a backlight boost driver (Kinetic KTD2801ECD-TR) for external screens, controlled by a SoC PWM output (Alp SDK™ driver planned). Connect the LED string anode to BL_LED_A (A31) and its cathode to BL_LED_K (B31), which is the driver feedback

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input. The driver supports up to 10 LEDs in series, or 2P6S, and integrates a 36 V over-voltage-protection (OVP) threshold on its boost switch node. BL_LED_A carries the boost output (up to 36 V): never connect it to a logic input, and rate the carrier traces and connector for it.

On the assembly variant without the on-module driver, BL_LED_A (A31) instead carries the 1.8 V backlight PWM (BL_PWM) from the SoC for an external backlight driver; leave BL_LED_K floating in that case. Contact Alp Lab for this variant. The MIPI DSI interface does not include on-module EMI or ESD protection; protect the DSI lanes with a low-capacitance TVS array on the carrier board.

Set the full-scale LED current with the feedback resistor R_{FB}, placed on the carrier between BL_LED_K (B31) and GND. Dimming lowers the current below this value:

$$I_{\mathrm{LED,max}} = 200\frac{\mathrm{mV}}{R_{\mathrm{FB}}}$$

8.7 MIPI CSI Camera

The Alif Ensemble series has a 2-lane MIPI CSI-2 interface (D-PHY Rx, MIPI CSI-2 v1.2 / D-PHY v1.2) for an external camera: up to 2.5 Gbps per lane (5.0 Gbps aggregate), up to 16 interleaved virtual channels, and input resolution up to 2 MP (1920 × 1080). On the E4, E6, and E8 variants the Ensemble SoC also integrates an on-die ISP and JPEG encoder for accelerated image processing (see Section 8.7.1); the E3, E5, and E7 variants do not.

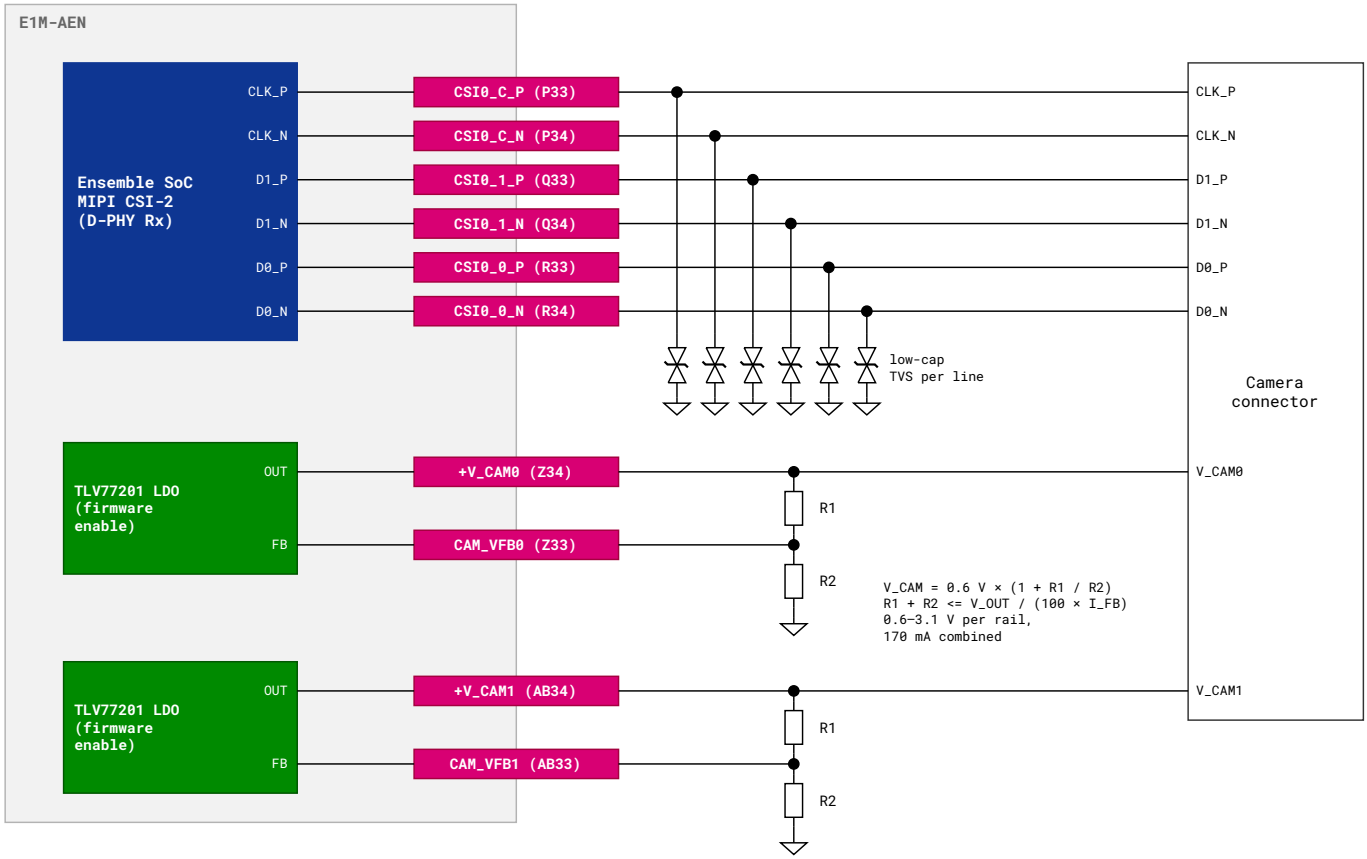


Figure 21 E1M-AEN MIPI CSI-2 Camera Connection and Camera Rails (carrier side)

8.7.1 On-die ISP & JPEG Encoder (E4 / E6 / E8)

On the E4, E6, and E8 variants the Ensemble SoC integrates an Image Signal Processor (ISP) in the data path between the camera interfaces (MIPI CSI / parallel CPI) and memory, plus a JPEG encoder for still-image and Motion-JPEG capture. Both blocks are clocked at up to 400 MHz. The E3, E5, and E7 variants omit both.

The **ISP** processes up to 2 MP (1920 × 1080) at up to 200 FPS (2 MP image, 100 MHz pixel clock), down to a 64 × 64 minimum output, and offers:

- Input formats: 8-, 10-, 12-bit Bayer; 8-, 10-bit YUV (BT.601 / BT.656); 8-, 10-bit monochrome

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- Black-level subtraction, digital gain, demosaicing (Bayer → RGB), and gamma correction
- Colour-space conversion (RGB → YUV), YUV422 → YUV444 → RGB
- Crop / Region-of-Interest, binning, and down-scaling
- Frame-rate control (configurable 60 FPS – 1 FPS)
- Auto-exposure (AE) and auto-white-balance (AWB)

The **JPEG encoder** compresses up to 2 MP at 200 FPS (32 × 32 minimum, 16K maximum frame width) and offers:

- JPEG ISO/IEC 10918-1 / ITU-T T.81 baseline (Huffman, interleaved YUV420)
- Motion-JPEG (T.81 Annex H) in an AVI container
- Encoding colour space YUV 4:0:0 / 4:2:0 / 4:2:2, 8-bit depth
- Rate control (target bits per picture), slice-mode encoding, 4:2:2 → 4:2:0 conversion, and multi-region alpha blending

> **Note:** These are Ensemble SoC hardware capabilities. Software status in Alp SDK™ v0.17.0 (E8 variants only, E1M-AEN801 and E1M-AEN803): the ISP-Pico backend of `<alp/camera.h>` is bench-verified on the E8 (E1M-AEN803 with an OV5647 camera; examples `aen-isp-capture` and `aen-isp-ov5647-viewfinder`). The Hantro VC9000E JPEG encoder backend of `<alp/jpeg.h>` is bench-verified on E1M-AEN801; its API is marked experimental and can still change. Bench verification so far covers the E8 only. See **AN-003: MIPI CSI Camera** for details before selecting a variant for its ISP.

E1M supports direct camera implementation via on-board LDOs. The LDOs run from the module's 3.4 V domain, so each output can be set between 0.6 V and 3.1 V; the two rails together supply at most 170 mA (100 mA per rail at a 3.1 V setting). At low output voltages the LDO dissipates more: at T_A = 75 °C one rail is limited to about 96 mA at a 1.2 V setting. Both rails are off until firmware enables them. The divider (R_1 from +V_CAMx to CAM_VFBx, R_2 from CAM_VFBx to GND) is on the carrier; place it as close as possible to the CAM_VFBx pins. The MIPI CSI interface does not include on-module EMI or ESD protection; protect the CSI lanes with a low-capacitance TVS array on the carrier board.

The output voltage is set by the divider:

$$V_{\mathrm{CAM}} = 0.6\ \mathrm{V} \times \left(1 + \frac{R_1}{R_2}\right)$$

To minimize feedback-pin current error, set the divider current to 100 × the maximum feedback-pin current. The resulting series resistance limit is:

$$R_1 + R_2 \leq \frac{V_{\mathrm{OUT}}}{I_{\mathrm{FB}} \times 100}$$

where $I_{\mathrm{FB,nom}} = 10\ \mathrm{nA}$ and $I_{\mathrm{FB,max}} = 100\ \mathrm{nA}$.

8.8 Parallel Camera

E1M-AEN provides an 8-bit parallel camera interface (CAM_PAR) for sensors that do not use MIPI CSI-2. The interface comprises the 8 data lines CAM_D1–CAM_D8, pixel clock CAM_PCLK, horizontal and vertical sync CAM_HSYNC / CAM_VSYNC, and the sensor master-clock output CAM_XVCLK. Sensor power can be supplied from the on-module adjustable LDO outputs (+V_CAM0 / +V_CAM1).

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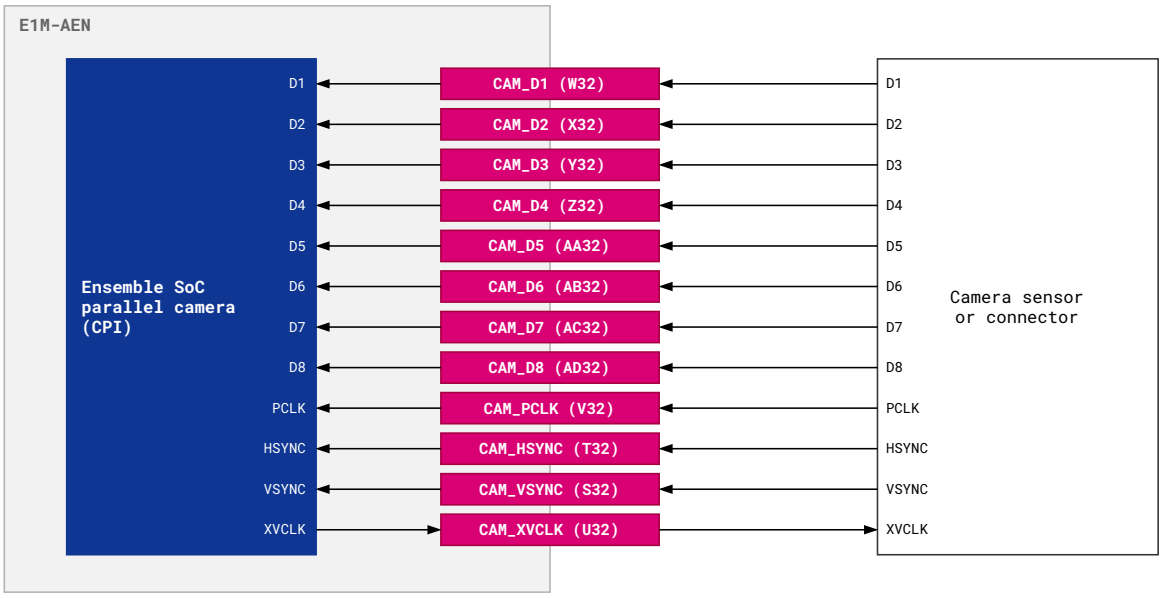


Figure 22 E1M-AEN Parallel Camera Pads

8.9 Microphone – PDM

E1M supports up to 4 digital microphones over 2 PDM interfaces (PDM_C0 / PDM_D0 on AA1 / AA2, PDM_C1 / PDM_D1 on AB1 / AB2). Each interface carries two microphones that share the clock and the data line: strap the L/R (channel select) pin of one microphone to GND (left) and of the other to its supply (right). The PDM pads are 1.8 V SoC pads: use microphones whose I/O runs at 1.8 V, and drive or pull up these pads only while VIO_OUT is high.

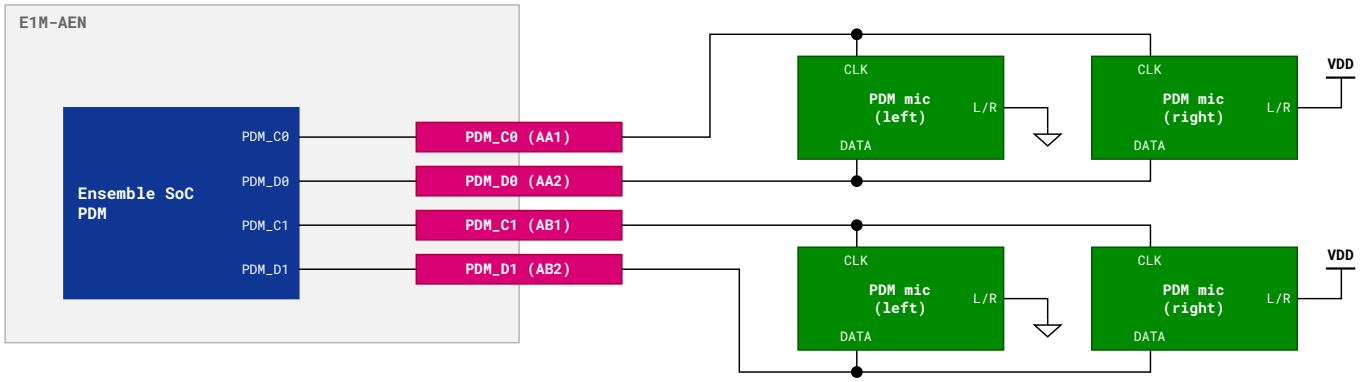


Figure 23 E1M-AEN PDM Microphone Connection (two microphones per data line)

Refer to the E1M hardware design guide for full details.

8.10 Analog Inputs

E1M provides 8 analog input channels. The Alif Ensemble series has a 12-bit ADC with a 5 Msps sampling rate. Analog inputs are referenced to 1V8.

R3 does not fit a standalone voltage reference; the ADC reference pin of the Ensemble SoC is decoupled on the module only (the 0.1 % 1.8 V reference option of R2 is removed).

Refer to the Alif Ensemble series datasheet for electrical characteristics.

8.11 Analog Outputs

E1M provides 2 analog output channels. The Alif Ensemble series has a 12-bit DAC with a 1 kHz sampling rate. Analog outputs are referenced to 1V8.

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Refer to the Alif Ensemble series datasheet for electrical characteristics.

8.12 Memories

E1M-AEN offers several memory options. The Alif Ensemble series has internal ROM and RAM of up to 5.5 MB and 13.5 MB respectively.

Two optional external memories sit on the single OSPI bus (OSPI0) of the Ensemble SoC, selected by chip select: a HyperRAM on `OSPI0` chip select SS0 and an octal NOR flash on chip select SS1. Both run from a switched 1.8 V supply that is off until firmware enables it. The OSPI bus is not available on the module pads. Which memories are fitted depends on the variant:

Variant	HyperRAM (RAM)	NOR flash
`E1M-AEN801`	`Not fitted`	`Not fitted`
`E1M-AEN803`	`Fitted, 512 Mbit`	`Fitted, 256 Mbit`
`E1M-AEN301, 401, 501, 601, 701`	`Assembly option`	`Assembly option`

Table 27 External Memory per Variant

The Alp SDK™ build metadata marks the E1M-AEN301, 401, 501, 601 and 701 memories as a BOM assembly option; contact Alp Lab for an assembly variant with external memory. External memories are useful when additional RAM or storage is required.

8.12.1 Identity EEPROM and I²C0

A 128 Kbit I²C identity EEPROM (onsemi N24S128C4DYT3G) is fitted on the module. It is connected to the E1M I²C0 bus, which is also available on the carrier: `I2C0_SDA` (AD2) and `I2C0_SCL` (AE2).

- **Addresses (7-bit):** `0x50` is the memory array. `0x58` holds the identity objects of the same part (Secure Data Page, 128-bit factory Unique ID, lock status and configuration register). Both addresses acknowledge. Carrier devices on I²C0 must not use `0x50` or `0x58`.
- **Supply:** the EEPROM is powered from the module 1.8 V rail, so it responds only while `VIO_OUT` is high. Do not power it from any pad (see the reserved pad W3 warning in Section 2.5).
- **Pull-ups:** the module has no pull-up resistors on I²C0. The carrier must pull `I2C0_SDA` and `I2C0_SCL` up to `VIO_OUT` (for example 4.7 kΩ), never to 3.3 V and never to an always-on rail. A carrier device that stays powered while the module is off must not hold the bus low (use an I_{off}-protected device or an isolator).
- **Content and write access:** the EEPROM holds the module identity programmed in production (SKU, serial number and hardware revision). It has no write-protect pin. Carrier firmware must treat it as read-only unless Alp Lab documents a user area.

> **Warning:** Do not place any other device at I²C address `0x50` or `0x58` on I²C0. An address conflict corrupts reads of the module identity and can make the bus unusable. Do not drive, load or jumper reserved pad W3: it is the EEPROM supply net, and feeding it back-feeds the whole 1.8 V domain.

8.12.2 Application MRAM Partition Map

The Alp SDK™ (v0.17.0) divides the 5.5 MB (5632 KiB) application MRAM of the Ensemble SoC for Zephyr builds as follows. The map is the same for all seven E1M-AEN variants.

Region	Size	Base address	Use
`mcuboot`	`64 KiB`	`0x80000000`	`Boot loader.`
`he_slot0`	`2688 KiB`	`0x80010000`	`Application image of the Cortex-M55 HE core.`
`hp_slot0`	`2688 KiB`	`0x802b0000`	`Application image of the Cortex-M55 HP core.`
`reserved`	`64 KiB`	`0x80550000`	`Reserved. Do not use.`
`storage`	`96 KiB`	`0x80560000`	`Application settings and data storage.`

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Region	Size	Base address	Use
atoc	32 KiB	0x80578000	Owned by the Secure Enclave (boot table). Write authority: Secure Enclave only.

Table 28 Application MRAM Partition Map (Alp SDK v0.17.0)

Warning: The **atoc** band (`0x80578000`, 32 KiB) holds the Secure Enclave boot table. The Alif Security Toolkit places the application table at the top of the MRAM window (`0x80580000`) and grows it downward. Never write or erase this band from an application, a production test, logging or a factory reset. Keep every MRAM erase range below `0x80578000`. Erasing the boot table can leave the module unable to boot until it is reprogrammed over the SE-UART. Alp SDK releases before v0.16.0 declared `storage` as 128 KiB, which overlaps the boot table: do not use erase ranges taken from such a build.

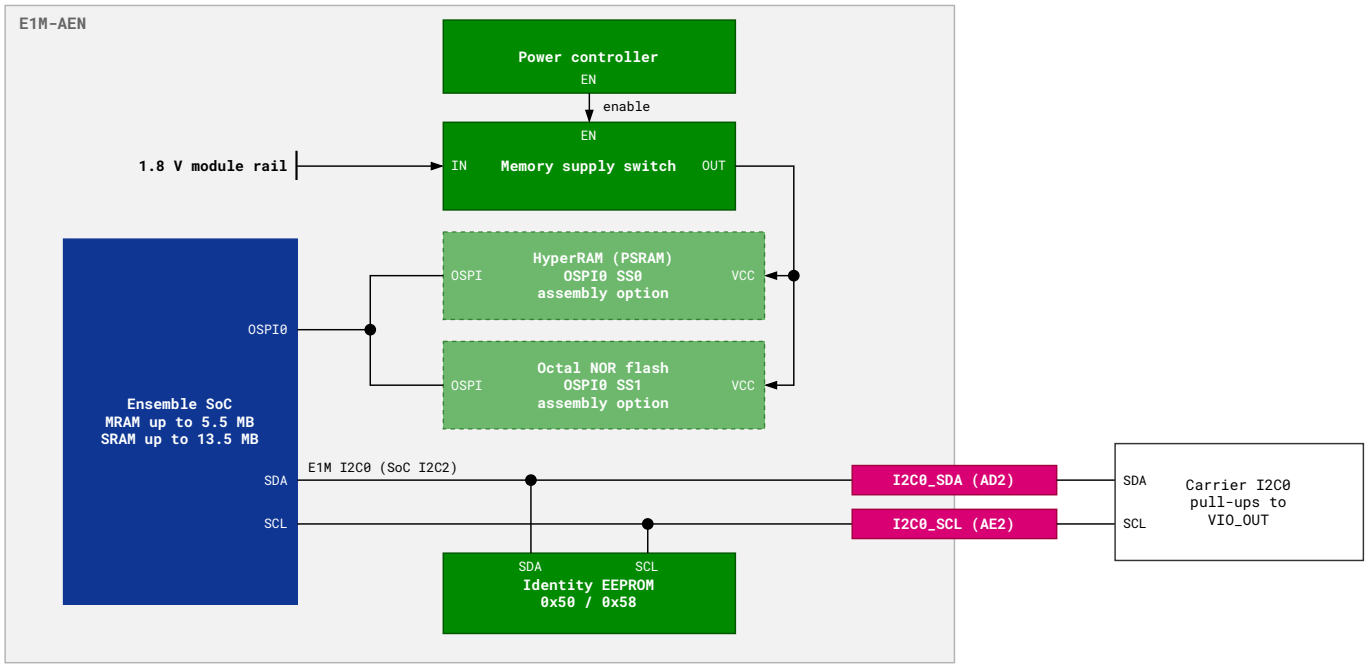


Figure 24 E1M-AEN Memory Options

9 Environmental & Reliability

9.1 Operating & Storage Conditions

Parameter	Symbol	Min	Max	Unit
Ambient operating temperature	T_A	- 40	+75	°C
Storage temperature	T_{STG}	- 40	+125	°C
Relative humidity (operating, non-condensing)	RH	TBD	TBD	%

Table 29 Environmental Conditions

9.2 Reflow Profile

The E1M-AEN is qualified per IPC/JEDEC J-STD-020 to MSL TBD. Figure 25 shows the recommended lead-free reflow profile: the measured E1M-AEN profile, smoothed, without its zone-boundary kink (JTR1000 convection reflow oven, ALPHA OM338 (SAC, Pb-free) solder paste, VCAM i612D profiler sampling every 0.5 s). Over the measured run the peak package temperature was 240.9–244.3 °C and the time at or above 220 °C 56.5–60.0 s (the measured ranges in the table below); the SAC liquidus is 217

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°C. Customers must keep the process within the recommended window in the table below and follow the dry-pack handling instructions in Section 14.2.

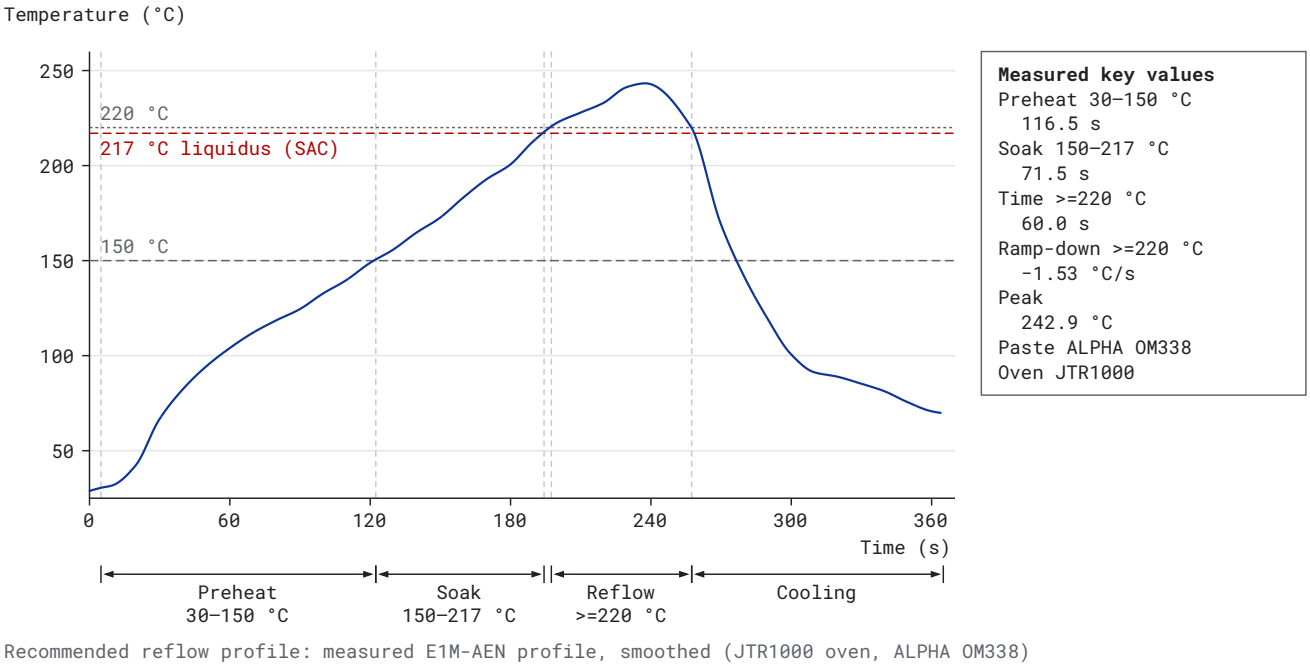


Figure 25 Recommended reflow profile: measured E1M-AEN profile, smoothed (JTR1000 oven, ALPHA OM338)

Parameter	Window min	Window max	Measured	Unit
Preheat time, 30–150 °C	60	160	116.5–122.0	s
Soak time, 150–217 °C	60	120	70.5–73.5	s
Time at or above 220 °C	45	90	56.5–60.0	s
Ramp-down slope at or above 220 °C	-4	-0.5	-1.53 to -1.66	°C/s
Peak package temperature	230	250	240.9–244.3	°C

Table 30 Reflow Profile Parameters (Pb-free): recommended window and measured values

9.3 Reliability Data

Parameter	Symbol	Value	Unit
Mean Time Between Failures (Telcordia SR-332, T_A = +25 °C)	MTBF	TBD	h
Moisture Sensitivity Level	MSL	TBD	–
Qualified shelf life (in dry-pack)	–	TBD	months

Table 31 Reliability Targets

10 Software & Operating System Support

The E1M-AEN is supported by the open-source **Alp SDK™**, which provides a unified HAL across all E1M variants. Out of the box, the SDK supports:

- **Bare-metal** application development on the Cortex-M55 real-time cores.
- **Zephyr RTOS** on the Cortex-M55 cores (Alp SDK™ board targets `alp_e1m_aen<NNN>_m55_hp` / `_m55_he`).

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- **Linux** on the Cortex-A32 application cores (E5/E6/E7/E8 variants) is planned but cannot be built yet: in Alp SDK™ v0.17.0 no E1M-AEN Yocto machine builds, and the build planner withholds the `bitbake` command for E1M-AEN Linux cores (`yocto-machine-unbuildable`). The E3/E4 variants are M55-only and do not support Linux.

Note: Alp SDK™ v0.17.0 supports E1M-AEN hardware revision R2. R3 support (power controller, switched supplies, self-off) follows in a later SDK release. In v0.17.0, Zephyr board targets exist for E1M-AEN801 and E1M-AEN803 (M55-HP and M55-HE), E1M-AEN401 and E1M-AEN601 (M55-HP); E1M-AEN301 / 501 / 701 Zephyr targets are not yet available, and no A32 Linux image is buildable for any variant.

Variant	Bare-metal (M55)	Zephyr (M55)	Linux (A32)
E1M-AEN301 (E3)	Yes	Planned	–
E1M-AEN401 (E4)	Yes	Yes	–
E1M-AEN501 (E5)	Yes	Planned	Planned
E1M-AEN601 (E6)	Yes	Yes	Planned
E1M-AEN701 (E7)	Yes	Planned	Planned
E1M-AEN801 (E8)	Yes	Yes	Planned
E1M-AEN803 (E8)	Yes	Yes	Planned

Table 32 Software Support Matrix

Note: See the Alp SDK™ repository, the documentation, the VS Code extension, and the E1M-AEN Hardware Design Guide for bring-up instructions, BSP layout, and SDK API reference. For support, contact contact@alplab.ai.

11 Reference Schematic

The minimum carrier-board design below brings up an E1M-AEN with a single 5 V input, a power button, an optional reset button, a module-on status input from `VIO_OUT`, and a JTAG/SWD debug header. All other interfaces (Ethernet, USB, MIPI, camera, display) are optional and described in Section 8.

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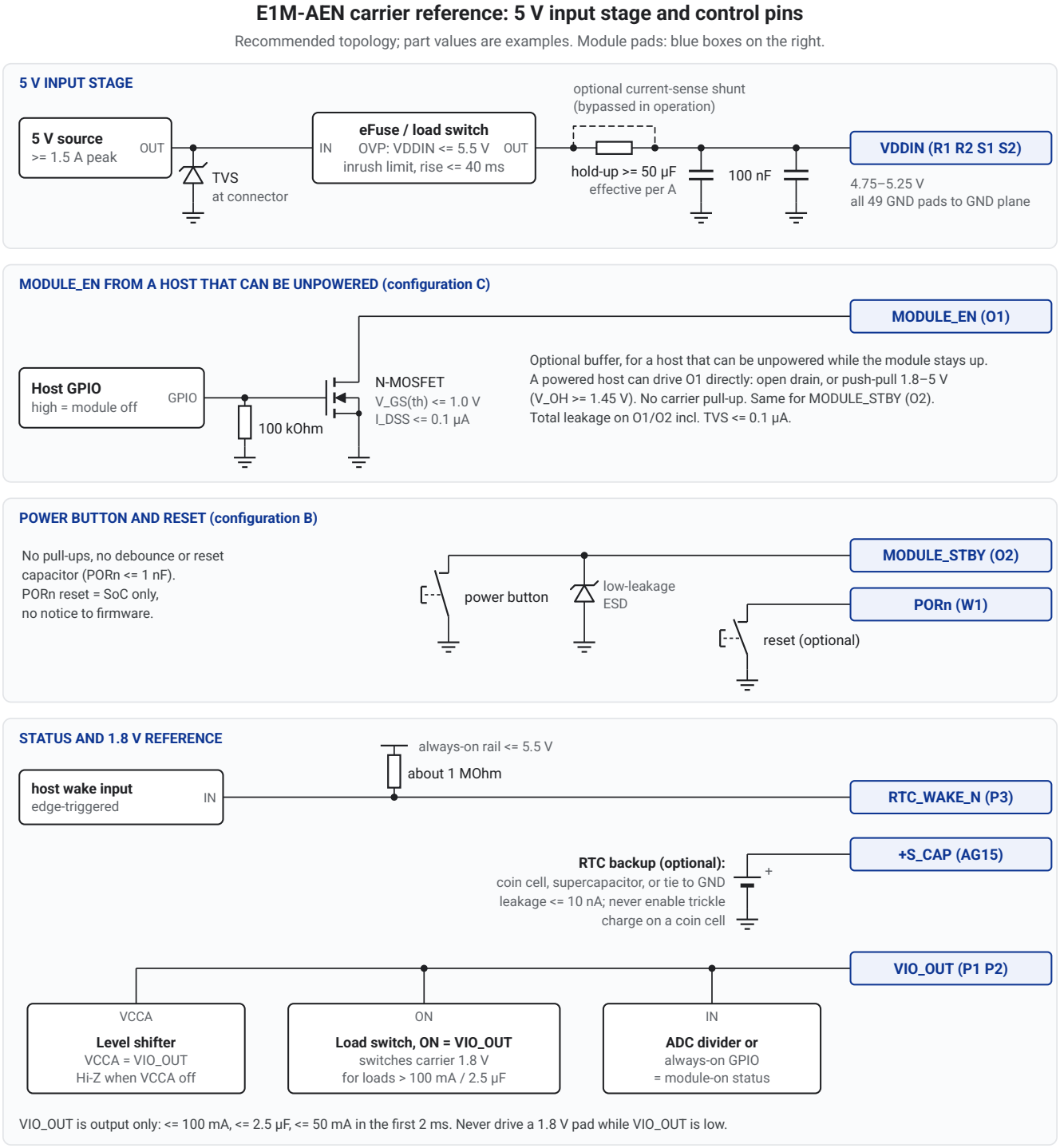


Figure 26 E1M-AEN Minimum Reference Circuit (power and control)

Required external components:

- 5 V power source, 4.75–5.25 V, ≥ 1.0 A continuous / ≥ 1.5 A peak, to VDDIN (R1, S1, R2, S2), with over-voltage protection that keeps VDDIN ≤ 5.5 V (TVS ahead of an eFuse with OVP) and inrush limiting.
- Hold-up capacitance close to VDDIN: ≥ 50 µF effective per A of total load on the VDDIN node (for example ≥ 47 µF effective for the 834 mA module peak), plus 100 nF.
- Power button between MODULE_STBY (O2) and GND (optional; sleep / wake / power off by firmware policy). No pull-up or debounce capacitor.
- Reset push-button between PORn (W1) and GND (optional, SoC reset only; reference design uses an ALPS SKSGACE010 tactile switch). No capacitor on PORn (≤ 1 nF). A reset stops the SoC with no notice to firmware; an MRAM write in progress is lost.

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- MODULE_EN (O1) left open, or driven open drain or push-pull from 1.8–5 V logic (see Section 6).
- RTC backup on +S_CAP (AG15): a coin cell, a supercapacitor, or a tie to GND if no backup is needed (optional; see Section 4.2). Never enable the RTC trickle charger with a coin cell fitted.
- 10-pin Cortex debug header on JTAG/SWD pads (optional, for development; reference design uses a Samtec FTSH-105-01-F-DV 1.27 mm header).

Optional carrier-board components are described per interface in Section 8, and in detail in the E1M-AEN Hardware Design Guide, whose Power Architecture & Carrier Power Design chapter covers the 5 V input stage, the control-pin circuits and the power sequences.

12 Compliance & Certifications

12.1 Environmental Compliance

Standard	Description	Status
RoHS 3 (EU 2015/863)	Restriction of hazardous substances	Compliant
REACH (EC 1907/2006)	Substances of very high concern	Compliant
Halogen-free (IEC 61249-2-21)	Br + Cl content limits	TBD
Conflict minerals (Dodd-Frank §1502)	Tin, tungsten, tantalum, gold sourcing	TBD

Table 33 Environmental Compliance

12.2 Wireless Certifications

See Section 8.4.3 for the per-region wireless certification IDs.

12.3 Functional Safety & Industry-specific Compliance

The E1M-AEN is not currently certified for safety-critical applications (IEC 61508, ISO 26262, IEC 62304, etc.). Contact Alp Lab for the most recent qualification status.

13 Mechanical & Footprint Dimensions

All dimensions are in mm unless otherwise noted.

Parameter	Symbol	Min	Max	Unit
Module length	L	34.9	35.1	mm
Module width	W	34.9	35.1	mm
Module height (PCB + tallest component)	H	–	TBD	mm
Module mass	m	–	TBD	g

Table 34 E1M-AEN Mechanical Dimensions

13.1 Recommended PCB Land Pattern

The recommended carrier-board land pattern follows IPC-7351 nominal density for LGA packages. The module uses a 1.0 mm pad grid with 0.4 mm round, non-solder-mask-defined pads. Pad geometry, stencil aperture, and solder-mask opening details are below. The courtyard is 2.0 mm around the module outline (39.0 × 39.0 mm overall). The dashed outline inside the pad ring is the carrier through-cutout of mounting option (b) (see Section 13.2).

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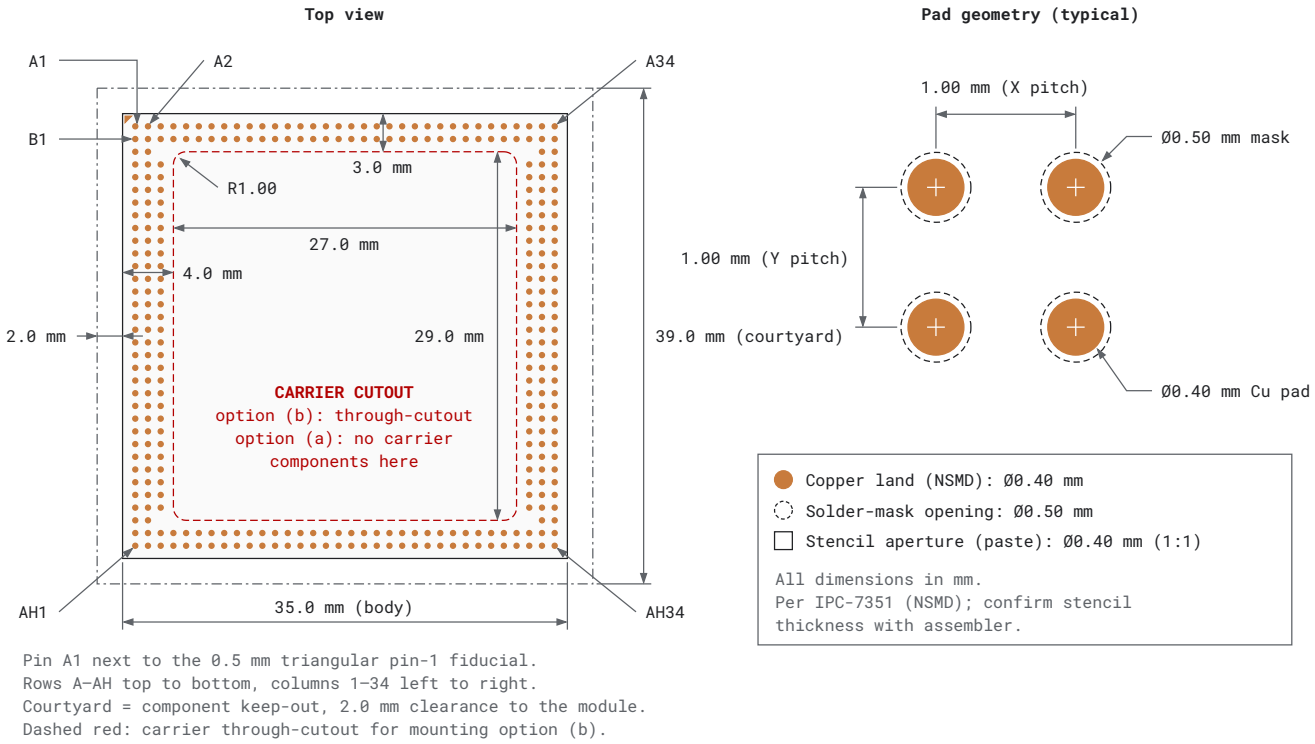


Figure 27 E1M-AEN Recommended Land Pattern (top view)

Parameter	Symbol	Value	Unit
Pad pitch (signal grid)	p	1.0	mm
Copper pad diameter	–	0.40 (dia.)	mm
Pad type	–	Round, NSMD	–
Solder-mask opening diameter	–	0.50 (dia.)	mm
Stencil aperture (1:1)	–	0.40 (dia.)	mm
Stencil material	–	Nano-coated steel mesh	–
Stencil thickness (recommended)	t	0.08	mm
Courtyard (2.0 mm clearance to the module outline)	–	39.0 × 39.0	mm
Carrier through-cutout, mounting option (b) (across × down)	–	27.0 × 29.0, R1.00 corners	mm
Cutout position from the module left / top edge	–	4.0 / 3.0	mm

Table 35 Land Pattern Parameters

13.2 Mounting and Keep-Out Zones

The module **shall not** be placed directly on the carrier board. One of two mounting options shall be used:

1. **Spacer PCB** — a spacer PCB between the module and the carrier board. The spacer PCB is soldered on both faces: the module LGA pads to the spacer, and the spacer to the carrier board.
2. **Carrier cutout** — a through-cutout in the carrier board the size of the module's central cavity: 27.0 mm across × 29.0 mm down, R1.00 corners, its left edge 4.0 mm from the module's left edge and its top edge 3.0 mm from the module's top edge (top view). It is drawn dashed in Figure 27.

The spacer thickness, the module height and the maximum component height on the module bottom side are not specified in this revision (TBD).

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Keep-out regions, shown in Figure 27:

- **Courtyard** — keep a 2.0 mm component-free clearance around the module outline (39.0 × 39.0 mm overall) for placement tolerance, inspection, and rework access.
- **Inside the pad ring** — with either option, place no carrier components inside the cutout outline (the cavity outline given above). With a carrier cutout (option b), the area is removed from the carrier; with a spacer PCB (option a), the carrier area under the cavity is kept clear. Signal routing beneath the module is permitted on inner layers and on the top layer between pads, outside the cutout.

RF traces (especially the antenna feed) must be routed away from high-current digital paths.

13.3 Module Marking

Each module is laser-marked on the top side with the following fields:

- Manufacturer logo (Alp Lab)
- Product name: E1M-AEN
- Production date code (YYWW)
- Serial number

The full MPN is not marked on the module. Wireless regulatory marks (FCC ID, ISED IC, MIC, etc.) are carried on the on-board wireless module, not on the E1M-AEN SoM.

14 Packaging

14.1 Trays

The E1M-AEN is supplied exclusively in JEDEC-compliant matrix trays. Tape & reel is not offered for this module.

Parameter	Symbol	Value	Unit
Tray standard	–	JEDEC matrix tray	–
Units per tray	–	TBD	pcs
Trays per dry-pack bag	–	TBD	pcs

Table 36 Tray Specifications

14.2 MSL & Handling

The E1M-AEN is classified to Moisture Sensitivity Level (MSL) TBD per IPC/JEDEC J-STD-020. Modules are shipped in dry-pack with desiccant and a humidity-indicator card.

After opening the dry-pack:

- Floor life: TBD hours at <= 30 °C / <= 60% RH.
- If floor life is exceeded before reflow, bake at TBD °C for TBD h before assembly.

Refer to IPC/JEDEC J-STD-033 for full moisture/reflow handling procedures.

15 Ordering Information

15.1 MPN Decoder

Field	Example	Description
Family	E1M	Edge-1 AI Module standard footprint.

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Field	Example	Description
Product line	AEN	Alif Ensemble. Other product lines are denoted by different three-letter codes (e.g. V2N for Renesas RZ/V2N).
SoC variant	7	Last digit of the Ensemble variant (E_x).
Memory option	0	Reserved for memory-config index; 0 = on-die memory only.
Assembly variant	1	Customer configuration code: selects which optional components are populated (e.g. wireless module, Ethernet PHY, CAN PHY, camera LDOs, connectors, external memory). 1 is the standard build; 3 is the standard build plus both external OSPI memories (E1M-AEN803). Contact Alp Lab for custom assembly variants.

Table 37 E1M-AEN MPN Convention

Note: Example: **E1M-AEN701** = E1M form factor, Alif Ensemble line, E7 SoC, on-die memory only, standard assembly variant 1.

15.2 Ordering Matrix

MPN	Main CPU	RAM int.	AP cores (A32)	NPU (Ethos U55 / U85)	ISP / JPEG
E1M-AEN701	AE722F80F55D5LS	13.5 MB	2 × 800 MHz	1 × 46 GOPS + 1 × 204 GOPS	No
E1M-AEN501	AE512F80F55D5LS	13.5 MB	1 × 800 MHz	1 × 46 GOPS + 1 × 204 GOPS	No
E1M-AEN301	AE302F80F55D5LE	13.5 MB	–	1 × 46 GOPS + 1 × 204 GOPS	No
E1M-AEN801	AE822FA0E5597LS0	9.75 MB	2 × 800 MHz	1 × 46 GOPS + 2 × 204 GOPS	Yes
E1M-AEN601	AE612FA0E5597LS0	9.75 MB	1 × 800 MHz	1 × 46 GOPS + 2 × 204 GOPS	Yes
E1M-AEN401	AE402FA0E5597LE0	9.75 MB	–	1 × 46 GOPS + 2 × 204 GOPS	Yes
E1M-AEN803	AE822FA0E5597LS0	9.75 MB	2 × 800 MHz	1 × 46 GOPS + 2 × 204 GOPS	Yes

Table 38 Ordering Information

All configurations above include:

- 5.5 MB internal MRAM. External OSPI memory: E1M-AEN803 fits 512 Mbit HyperRAM + 256 Mbit NOR flash; E1M-AEN801 fits none; E1M-AEN301 / 401 / 501 / 601 / 701 have on-die memory only in the standard build (external memory is an assembly option)
- Real-time cores: 1 × 160 MHz + 1 × 400 MHz Cortex-M55
- Operating temperature: − 40 °C to +75 °C
- 2.4 GHz Wi-Fi 6 + BLE 5.4 combo module (BDE-BW3501N)
- 100 Mbit Ethernet PHY
- Display backlight driver
- 2 LDOs for external cameras
- RTC backup supercapacitor **not fitted** (DNP) on every order code. The RTC backup store is on the carrier, connected to +S_CAP (AG15): see Section 4.2.
- On-module RF connector (I-PEX MHF 4L) **not fitted** (DNP); the RF output is pad AH1 (ANT_2.4GHZ).

Note: An on-module RTC backup supercapacitor is available only as a custom assembly variant for room-temperature products. Modules with it fitted are rated − 20 °C to +60 °C, the rating of the supercapacitor. Contact Alp Lab.

RoHS-compliant. Contact Alp Lab for custom assembly variants (lead finish, ball material, etc.).

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16 References & Related Documents

Ref.	Title	Source
[1]	Alif Semiconductor Ensemble Series Datasheet	Alif Semiconductor
[2]	Alif Semiconductor Ensemble Series Reference Manual	Alif Semiconductor
[3]	E1M™ Specification	github.com/alplabai/e1m-spec
[4]	E1M-AEN Hardware Design Guide	Alp Lab (HG-AEN-001)
[5]	Alp SDK™ Repository	github.com/alplabai/alp-sdk
[6]	Alp SDK™ Documentation	docs.alplab.ai
[7]	Alp SDK™ VS Code Extension	github.com/alplabai/alp-sdk-vscode
[8]	BDE-BW3501 Wi-Fi 6 / BLE Module Datasheet	BDE Technology
[9]	IPC/JEDEC J-STD-020 – Reflow Profile	JEDEC
[10]	IPC/JEDEC J-STD-033 – Moisture/Reflow Handling	JEDEC

Table 39 Related Documents

17 Revision History

Revision	Changes	Date
0.1	• Initial draft.	December 2025
0.2	• Memory options updated with the correct diagram. • Wi-Fi throughput updated to 20 Mbps.	April 2026
0.3	• SoM-typical sections added: Recommended Operating Conditions, ESD & Latch-up, Thermal Characteristics, Power Sequence, Boot Modes, Reset & Module Enable, JTAG/SWD Debug, Wireless RF & Regulatory, Environmental & Reliability, Software Support, Reference Schematic, Compliance, Land Pattern, Packaging (Trays), MPN Decoder, References, Legal Notices.	May 2026
0.4	• Pin tables regenerated and verified against the E1M specification and the production board netlist (all 312 pads). • Corrected power pins (VIO_OUT, MODULE_EN/STBY); removed non-existent IO_EN and +3V3_OUT; unused standard pins named “leave floating”. • Wireless module identified as dual-band BDE-BW3551N (CC3551E) with measured RF characteristics. • USB 2.0 corrected to the USB2 pins. • +V_CAM rails documented as adjustable TLV77201 LDOs. • Ordering Matrix simplified; MPN decoder last field corrected to Assembly variant. • Updated repository / documentation / contact links. • On-module interface ESD/EMI protection removed except on the SDIO / SD-card interface; carrier board must now provide ESD/EMI protection on Ethernet, MIPI DSI, and MIPI CSI. • Reflow profile populated (Pb-free, ALPHA OM338, peak 241–244 °C); SMT stencil specified (nano-coated steel mesh, 0.08 mm). • Pin-out drawing redrawn as a top-view, colour-coded 312-pad diagram.	June 2026
0.5	• Pin tables re-verified against the production board netlist (E1M-AEN 2626-R2, all 312 pads). • IO21 (L3) and IO22 (M3) moved from the Digital Pins table to Not-connected Pins – both pads are unbonded on E1M-AEN, like IO23–IO25. • Module Output Rails: corrected VIO_OUT pins from AC1/AC2 (GND) to P1/P2.	June 2026
0.6	• Corrected NPU configuration in the key-features list: E4/E6/E8 carry 2 × Ethos-U55 + 1 × Ethos-U85 (previously mislisted as 3 × Ethos-U55). Verified against the Alif E4/E6/E8 datasheets (454 GOPS total: 46 + 204 + 204).	July 2026

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Revision	Changes	Date
	• Ordering-table NPU column relabelled “Ethos U55 / U85” to reflect the Ethos-U85 (NPU-HG) on the E4/E6/E8 parts.	
0.7	• Cover page: replaced the block-diagram placeholder with front/back product photos of the E1M-AEN module (rev 1726-R4A).	July 2026
0.8	• Cover page: added an “Edge-1 AI Module” sub-heading; resized cover photos so the Applications section fits on page 1. • Absolute Maximum Ratings: added CAN bus (± 58 V), Ethernet MDI (- 0.3 to +4 V), and backlight boost switch node (- 0.3 to +40 V) rows. • Removed the duplicated module-supply-voltage row from Electrical Characteristics (retained in Recommended Operating Conditions). • Documented interface ESD protection: Ethernet DP83825I (± 5 kV IEC 61000-4-2), CAN TCAN1044AVDRBRQ1 (ISO 10605 ± 8 kV contact / ± 15 kV air), SD-card NVT4858HKZ (IEC 61000-4-2 level 4, ± 8 kV / ± 15 kV). • Named the backlight controller (KTD2801ECD-TR, 36 V OVP).	July 2026
0.9	• Recommended Operating Conditions and Environmental Conditions: removed the S/E temperature grades and the +105 °C E-grade and junction-operating rows; the module is now specified over a single – 40 °C to +85 °C ambient range. • Power Architecture: clarified that no power-rail sequencing is required (PMIC-managed rail bring-up), separate from the carrier-side control-signal bring-up steps in the Power-Up & Reset Sequence. • MIPI CSI Camera: added an “On-die ISP & JPEG Encoder (E4 / E6 / E8)” subsection detailing the Ensemble ISP and JPEG-encoder feature sets (verified against the Alif E8 datasheet v1.0 §3.19.3–3.19.4); noted the blocks are absent on E3 / E5 / E7 and not yet exposed through the Alp SDK. • MIPI DSI / CSI: stated interface throughput and resolution (DSI 2-lane × 1.25 Gbps, up to FHD; CSI-2 2-lane × 2.5 Gbps, up to 2 MP) and added a MIPI Interface Summary table (verified against the Alif E8 datasheet v1.0).	July 2026
0.10	• MIPI DSI Display: removed the incorrect “up to FHD (1080p)” display-resolution claim. The Alif E8 datasheet v1.0 (§3.20.2) specifies no fixed DSI panel resolution — the maximum is limited by the pixel clock and the 2-lane × 1.25 Gbps D-PHY Tx link bandwidth (video mode only). The 1920 × 1080 (2 MP) figure applies to the ISP / camera-input path, not the DSI display output. DSI lane rate (1.25 Gbps/lane, 2.5 Gbps aggregate) re-confirmed correct against the datasheet.	July 2026
0.11	• Updated for module hardware revision R3; added a Hardware Revisions section listing the carrier-visible changes from R2. • USB 2.0 moved to the USB0 pads B1 / C1 / C2 / D2; I1 / J1 / I2 / J2 are not connected on R3. • IO8 / IO9 / IO10 / IO11 are now SoC GPIOs (P15_1 / P15_7 / P15_5 / P7_5); IO21–IO24 are Wi-Fi module GPIOs; IO25 (P3) is the new RTC_WAKE_N output. Wi-Fi module GPIOs are marked valid only while Wi-Fi is powered. • Power architecture rewritten: always-on domain with RTC and power controller, switched supply islands, self-off with RTC self-wake. Replaced the “integrated PMIC” description. • New Reset, Module Enable & Power Control chapter: MODULE_EN / MODULE_STBY levels (5 V tolerant), module states, control timing, carrier sequences and reference configurations. PORn minimum pulse 2 ms; power-up to PORn high 206 ms typ / 290 ms max. • VDDIN range 4.75–5.25 V, absolute maximum 5.5 V including transients; supply rise time, source capability and hold-up requirements added. • VIO_OUT limited to 100 mA and 2.5 µF; +V_CAM0 / +V_CAM1 0.6–3.1 V, 170 mA combined. • Power Consumption table populated with calculated typical values (preliminary, not yet measured). • Wireless corrected to the 2.4 GHz-only BDE-BW3501N (CC3501E); 5 GHz figures removed; on-module RF connector is an I-PEX MHF 4L assembly option. • Reserved-pad warning added (W3, U3 / V3, S3, Q3 / R3 / T3); I^2C0 addresses 0x50 / 0x58 reserved by the module EEPROM; carrier thermal rules added.	October 2026

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Revision	Changes	Date
	• New variant E1M-AEN803 (E8 with 512 Mbit HyperRAM + 256 Mbit NOR flash): variant summary, ordering matrix, MPN assembly code 3, software support. • Memories: new Identity EEPROM and I²C0 subsection (addresses 0x50 / 0x58, supply only while VIO_OUT is high, carrier pull-ups to VIO_OUT, read-only guidance). Audit corrections: standard-build CAN pads are 1.8 V logic (CAN PHY not fitted); BL_LED_A and SD_VDD output ratings; SD_DET / SD_RST are 1.8 V pads; SD_VDD and MODULE_STBY R2 → R3 rows; internal memory sizes, latch-up rating, Software Support Matrix and SDK status corrected. • Debug pads: AD3 / AE3 documented as the Secure Enclave UART (programming path, dedicated pins); JTAG_nRST pull-up stated; +S_CAP (AG15) documented. All 312 pads re-checked against the R3 netlist. • Ambient operating temperature capped at +75 °C (– 40 °C to +75 °C, set by the Ensemble SoC). • Reference Schematic: 5 V source, protection and hold-up requirements; power button on MODULE_STBY; no capacitor on PORn. SD card: removed the on-module series-resistor claim (not fitted on R3). • R3 power-control update: MODULE_EN / MODULE_STBY now accept 1.8 V, 3.3 V and 5 V logic ($V_{OH} \geq 1.45$ V); released level about 1.2–1.5 V. Standby currents updated (STOP 3.84 µA, STOP with MODULE_STBY low 6.6 µA, self-off 1.14 µA, shutdown 2.94 µA). Module states, control table, electrical rows, reference configurations and carrier sequences updated; power-architecture and carrier-reference figures redrawn. • +S_CAP absolute maximum 5.5 V, charge voltage and backup threshold added to the electrical characteristics. • RTC backup moved to the carrier: +S_CAP (AG15) is connected to the RTC backup input; new RTC Backup section (coin cell, supercapacitor, none) with the trickle-charger warning. The standard module is rated – 40 °C to +75 °C; the – 20 °C to +60 °C supercapacitor rows are removed (room-temperature assembly option only). Reserved pads U3 / V3 described as the private 3.3 V I²C bus. Simulated RF path loss added. • Hardware-damage and data-loss items: R2 modules have no reset or brownout supervisor and the carrier must provide one (Alif ER004), R3 has one on the module; application MRAM partition map added with the Secure Enclave atoc warning (0x80578000, erase ranges stay below it); external memory stated per variant (E1M-AEN803 both fitted, E1M-AEN801 neither, others assembly option); Linux on the A32 stated as not yet buildable; ISP / JPEG software status updated to Alp SDK v0.17.0; Ethernet PHY named DP83825 with MDIO address 0 and PHY identifier 0x2000a140.	
0.12	• External Memory per Variant table: E1M-AEN803 HyperRAM corrected to 512 Mbit (the table said 256 Mbit; the rest of the datasheet already said 512 Mbit).	October 2026

0.13	• Block diagram updated to R3:
	  ▸ Ethernet PHY on RMII (100 Mbps)
	  ▸ Wi-Fi 6 / BLE 5.4 module on SPI + IRQ
	  ▸ EEPROM on I²C0 shared with the E1M I²C0 pads
	  ▸ temperature sensor on the internal I²C, with the RTC and the power controller behind a level shifter on the always-on 3.3 V side
	  ▸ secure element removed (not fitted)
	  ▸ power section (always-on LDOs, power controller, bucks, supervisor) with the MODULE_EN / MODULE_STBY, PORn, RTC_WAKE_N, VIO_OUT, SD_VDD, +V_CAM0/1 and +S_CAP pads
	  ▸ Ethos-U85 on E4 / E6 / E8
	  ▸ assembly options (CAN PHY, OSPI memories) drawn dashed.
	• Power-up timing figure: a released MODULE_EN rises together with VDDIN (module pull-up on the always-on 1.8 V rail).
		October 2026

0.14	• Block diagram layout cleanup: arrowheads unified, stray connection lines removed, I²C bus junction restored, power section aligned with the module blocks.	October 2026

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Revision	Changes	Date
0.15	• New pad-level interface figures drawn from the R3 netlist, with carrier protection and magnetics as schematic symbols (one TVS per line, 1:1 transformer per Ethernet pair, CAN common-mode choke and split termination): Ethernet, USB 2.0, I^2C / I^3C, UART / SPI, CAN, antenna, SD card, MIPI DSI and backlight, MIPI CSI-2 and camera rails, parallel camera, PDM microphones and memory options. The module is shown at block level only. • Block diagram text is plain SVG text. • Block diagram and reference debug-header figures redrawn in the style of the interface figures (same content; the Wi-Fi antenna feed to the Antenna pad drawn solid, with the on-module I-PEX MHF 4L connector drawn as a dashed assembly-option connector inside the module outline, as in the antenna figure). • Pin-out drawing with tighter cells; derating legend moved below the plot. • Pin-out drawing redrawn and split into four quarters at one scale each with the module name, SoC, size, pitch, pad count and a default-function legend inside the module outline, so that every pad name prints at 8 pt; C3, AF3, C32 and AF32 drawn as not fitted. Pad names unchanged, Roboto Mono, no title inside the figure. • Pin Diagram and List: pad-frame statement added. • Land pattern figure redrawn in the E1M specification drawing style with the corner pads marked. All values unchanged; the figure is now placed at the full text width and its caption says top view. • Reflow profile figure redrawn in the house figure style (same measured curve, phases, liquidus, peak, time-above-liquidus and parameter values). • Power architecture, power-up timing, reset timing and minimum reference circuit figures redrawn for readability. • Cover and description: the E1M footprint and pinout are an open standard (E1M-STD-1.0); the module design itself is not open source. • Pin tables: SoC pin or peripheral instance per pad for I^2C0 (SoC I2C2), I^2C1, I^3C, UART0 (SoC UART5), UART1 (SoC UART3), I^2S0 (SoC I2S3), I^2S1 (SoC LPI2S), SPI0 (SPI0_CS1 = SoC SS2), PDM1 (SoC PDM channel 2), analog inputs (ANA_S4–ANA_S7 = SoC ANA_S6 / S8 / S14 / S15), IO0–IO7, parallel camera (CAM_D1–CAM_D8 = SoC CAM D0–D7), JTAG, and the Wi-Fi module SPI1 and GPIO pins (IO15–IO17 do not match their CC3501E GPIO numbers). P3 is pad IO25, carrying RTC_WAKE_N. • Pin tables: ETH0_LED0 is a 3.3 V output and ETH0_LED1 a 1.8 V output (both PHY strap pins); Auto-MDIX can swap the DA / DB pairs; PORn has a 100 kΩ pull-up and 1 nF on the module (no carrier pull-up or capacitor); BL_LED_K is the backlight driver feedback input with R_{FB} on the carrier; CAM_VFB0 / CAM_VFB1 need the divider on the carrier; I^2C and I^3C pads have no module pull-ups; W3 is the identity-EEPROM supply net; S3 is pulled up to the Wi-Fi 3.3 V rail; RTC_CLKOUT source named. • Backlight: LED current corrected to $I_{LED,max}$ = 200 mV / R_{FB} (was 95 mV); BL_LED_A carries the boost output (up to 36 V); BL_PWM is on BL_LED_A only in the assembly variant without the driver. • Ethernet: the DP83825 MDI ESD rating is ± 5 kV HBM (a component rating, not IEC 61000-4-2; other PHY pins ± 1.5 kV HBM), so IEC 61000-4-2 protection is required on the carrier; the LED pads carry the PHY rating; strap rules and LED wiring stated; RMII with an on-module 50 MHz oscillator. • Memories: HyperRAM on OSPI0 SS0 and NOR flash on OSPI0 SS1, on a switched 1.8 V supply; OSPI not on the pads. USB: no ESD or VBUS switch on the module. I^3C: SDA pull-up required, SCL pull-up optional. SPI1: no pull-ups while Wi-Fi is off. SD: SD_RST has no microSD contact. PDM: L/R strapping and 1.8 V microphone I/O. • Electrical characteristics: RTC charge resistance 12.5 / 15.5 / 17.4 kΩ (15 kΩ setting, diode included); backup threshold 1.8 / 2.0 / 2.2 V in Level Switching Mode; backup-time figures state their RTC mode and currents; coin cell needs a 100 Ω–1 kΩ series resistor; unused +S_CAP tied to GND through 10 kΩ; +V_CAM feedback reference, feedback current, minimum divider current (2 µA), feed-forward capacitor (≤ 100 pF) and carrier capacitance (≤ 37 µF) added; brownout supervisor threshold (2.9 V) stated.	October 2026

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Revision	Changes	Date
	• Figure text uses only characters the figure font has: approximate values read “about” (was the approximately-equal sign), limits read >= / <=, resistances read Ohm / kOhm / MOhm, “Pi matching network”, “theta_module”, “PORn falls” / “PORn rises” (values unchanged). • Tables: cell text set ragged-right instead of justified, so narrow cells no longer stretch the gaps between words; the Ensemble MPU Options table is kept on one page with its caption, with a wider MPU column; the part number BDE-BW3501N no longer breaks at its hyphen in the pin list; ranges written with an en dash (for example 0.6–3.3 V, A–AH) no longer print a space after the dash (values unchanged). • Packaging: the tray drawing placeholder removed; the tray drawing is not yet available.	
0.16	• Pad maps, footprints and pad-frame text redrawn: letters down (rows), numbers across (columns), A1 top-left. • Pad assignments unchanged. • Pad frame corrected to the E1M standard (the frame of the E1M specification drawings and of the pinout viewer on alplab.ai): pad letter = row, A–AH top to bottom; pad number = column, 1–34 left to right; A1 top-left at the pin-1 marker, A2 right of A1, B1 below A1, A34 top-right, AH1 bottom-left, AH34 bottom-right. • Pin-out drawing redrawn in that frame as four quarters at one scale (rows A–Q / R–AH, columns 1–17 / 18–34): top and bottom bands two pads deep (rows A, B and AG, AH), left and right bands three pads deep (columns 1–3 and 32–34); every column at the same horizontal position in every row; C3, AF3, C32 and AF32 drawn as not fitted in the side bands. Pad names unchanged; placed at the full text width (pad names print at 8 pt). • Land pattern figure redrawn in that frame: corner pads A1 (top left), A34 (top right), AH1 (bottom left) and AH34 (bottom right) marked, A2 right of A1 and B1 below A1; pad ring three pads deep at the left and right and two pads deep at the top and bottom; keep-out cavity 27.0 mm across and 29.0 mm down; figure note corrected. Pad size, pitch, body and stencil values unchanged (the courtyard is 2.0 mm, see the Courtyard entry below). • Pin Diagram and List: pad-frame statement and band description corrected. • Module outline drawn as a plain 35.0 × 35.0 mm rectangle; A1 is identified by the 0.5 mm triangular pin-1 fiducial, a copper feature like the pads, now drawn in copper in the land pattern (to scale, 0.2 mm in from the edges) and in the pad maps, and the figure note and pad-frame statement say so. • Mounting: the module is not placed directly on the carrier; a spacer PCB (option a) or a carrier through-cutout 27.0 mm across × 29.0 mm down, R1.00 corners, 4.0 mm from the module’s left edge and 3.0 mm from its top edge (option b) is used; the spacer PCB is soldered on both faces (module to spacer, spacer to carrier), and under either option the carrier has no components inside the cavity outline. Keep-Out Zones section renamed Mounting and Keep-Out Zones and rewritten; the no-components rule inside the pad ring now applies with option (a). • Courtyard: 2.0 mm clearance around the module outline, 39.0 × 39.0 mm overall (was 1.0 mm, 37.0 × 37.0 mm); land pattern figure, Recommended PCB Land Pattern text and Land Pattern Parameters table updated. • Land pattern figure: the cavity outline is drawn as the option (b) carrier cutout, with its 4.0 mm and 3.0 mm position dimensions and R1.00 corners.	October 2026
0.17	• Block diagram: ▸ I2C[0:1] (was I2C[0:2]) and SPI0 from the SoC with SPI1 from the Wi-Fi module (was “2x SPI” / SPI[0:2] from the SoC), as in the pin tables ▸ Wi-Fi module GPIOs IO13, IO15–IO24 drawn from the Wi-Fi module ▸ pad labels set to the pad names: ANT_2.4GHZ (was Antenna), ETH0 (was Ethernet), CAN0 (was CAN_BUS), USB0 (was USB2.0), SD0 (was µSDHC), DSI0 (was DSI), CSI0 (was CSI), VDD (was VDD_IN), MODULE_EN and MODULE_STBY (was MODULE_EN/STBY), PWM[0:7], ANA_S[0:7], DAC[0:1] and ENC[0:3] (were 8 x PWM, 8 x ADC, 2 x DAC and 4 x Encoder)	October 2026

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Revision	Changes	Date
	▸ SoC block: A32 count per variant, 1 × on E5 / E6 and 2 × on E7 / E8 (was 2 × A32 for every variant), MRAM 5.5 MB and SRAM 13.5 MB (E3 / E5 / E7) / 9.75 MB (E4 / E6 / E8) added ▸ SD0 drawn through the NVT4858 level translator ▸ +V_CAM0 / +V_CAM1 and CAM_VFB0 / CAM_VFB1 drawn from the camera LDOs (TLV77201) ▸ +S_CAP drawn to the RTC (RV-3028) backup input (was the power section) and RTC_CLKOUT added ▸ CAM_PAR, PDM[0:1], AUDIO_CLK, DBG_TX/DBG_RX (SE-UART) and GPIO IO0, IO2–IO11 added ▸ OSPI0 memories with size and chip select (NOR flash 256 Mbit on SS1, HyperRAM 512 Mbit on SS0) ▸ EEPROM 128 Kbit ▸ part numbers BDE-BW3501N (CC3501E), DP83825, KTD2801 and TCAN1044AVDRBRQ1 ▸ BL_LED_A/K drawn bidirectional (BL_LED_K is the driver feedback input) ▸ legend notes for the OSPI memories per variant, the standard-build CAN pads B18 / B19 and the Wi-Fi module pads ▸ white figure background for dark pages.	
0.18	• Layout: the Block Diagram heading is kept on the same page as its figure.	October 2026
0.19	• Release history: every entry formatted as a bullet list.	October 2026
0.20	• Reflow profile: figure redrawn from the measured JTR1000 run (three thermocouples CH3, CH4, CH5 at their true time and temperature scale, with the 150 °C, 217 °C liquidus and 220 °C lines, the phase spans and a parameter box of the measured ranges); caption “Measured profile of the E1M-AEN (three thermocouples)”. • Reflow parameters (text, figure and table): measured time at or above 220 °C 56.5–60.0 s (was “about 60 s” above 217 °C), peak 240.9–244.3 °C (was 241–244 °C), soak 150–217 °C 70.5–73.5 s (was 70–74 s), preheat 30–150 °C 116.5–122.0 s, cooling slope from 220 °C −1.53 to −1.66 °C/s (was about −1.6 °C/s), over the three thermocouples. • Reflow parameters table: recommended window from the profiler report beside the measured values: preheat 30–150 °C 60–160 s (new), soak 150–217 °C 60–120 s (unchanged), at or above 220 °C 45–90 s (was “time above liquidus (≥217 °C)” 45–90 s), cooling from 220 °C −4 to −0.5 °C/s (was average ramp-down T_P to T_L min −1.6 °C/s), peak 230–250 °C (was 241–244 °C); the ramp-up (max 3 °C/s) and time 25 °C to peak (max 8 min) rows removed (not in the measurement report).	October 2026
0.21	• Reflow profile figure: one measured curve (was three traces), with its phase spans and values (preheat 30–150 °C 116.5 s, soak 150–217 °C 71.5 s, at or above 220 °C 60.0 s, cooling from 220 °C −1.53 °C/s, peak 242.9 °C) and no legend; caption “Measured reflow profile of the E1M-AEN (JTR1000 oven, ALPHA OM338)”. • Reflow parameters table: the measured column is headed “Measured” (the ranges are unchanged).	October 2026
0.22	• Table of Contents: each entry links to its section; the front-matter lists are set tighter. • Page 1: the Applications section is back on the first page (smaller module photos); the Features and Applications headings are unnumbered. • Reflow figure: measured E1M-AEN profile, smoothed, without its zone-boundary kink (was the measured trace with that kink); caption “Recommended reflow profile: measured E1M-AEN profile, smoothed (JTR1000 oven, ALPHA OM338)”. • Reflow parameters: the ramp-down slope (−1.53 to −1.66 °C/s) is the slope at or above 220 °C, from the peak down to 220 °C (was labelled “cooling from 220 °C”).	October 2026
0.23	• Removed the shut-down community forum; support is by email and the documentation site.	November 2026
0.24	• Product name on page 1 links to the product page on alplab.ai.	November 2026

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Revision	Changes	Date
0.25	• Release History: a semicolon after a resistor value in the 0.15 row is printed again.	November 2026
0.26	• Pinout table, SE-UART row: the SE-UART settings are stated (8N1, 57 600 baud on E4 / E6 / E8, 55 000 baud on E3 / E5 / E7).	November 2026

Table 40 Revision History

18 Legal Notices

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