ALP LAB

E1M-AEN HW Design Guide

Document Number: HG-AEN-001 **Revision:** 0.15 **Date:** November 2026 **Status:** Preliminary

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Release History

Revision	Changes	Date
0.1	• Initial draft	April 2026
0.2	• Expanded to carrier-design depth: added Land Pattern & Keep-Out, PCB Layout Guidelines (stack-up + controlled-impedance/skew targets), Module Output Rails, Power-Up & Reset Sequence, Carrier Control Signals, pin-out reference, JTAG/SWD debug header, USB 2.0 and SD/SDIO interfaces, camera-LDO and backlight-driver design, Thermal Design, and a References section. • Fixed status/naming/link consistency. • Interface ESD/EMI protection moved to the carrier board (on-module protection retained only on the SD-card interface). • Stencil spec updated (nano-coated steel mesh, 0.08 mm). • Pin-out figure replaced with the top-view, colour-coded 312-pad drawing.	June 2026
0.3	• SoC Variants table: E4/E6/E8 NPU corrected to 2 × Ethos-U55 + 1 × Ethos-U85 (was 3 × Ethos-U55), per the Alif E4/E6/E8 datasheets.	July 2026
0.4	• Power-Up & Reset Sequence: reworded to separate on-module PMIC rail sequencing (no carrier-side rail sequencing required) from the carrier-side control-signal bring-up order.	July 2026
0.5	• Updated for module hardware revision R3. • Power Architecture rewritten as a carrier design chapter: 5 V input stage (range, ramp, source, hold-up, TVS and inrush), battery-powered carriers, module power domains and states, `MODULE_EN` / `MODULE_STBY` / `PORn` / `VIO_OUT` / `RTC_WAKE_N` carrier circuits with do and don't rules, driving the control pins from a 1.8 V host, reference carrier configurations, power-up / sleep / power-off / wake / reset sequences with timing, back-powering rules, and a power bring-up procedure. • Output rails updated (VIO_OUT 100 mA; +V_CAM 0.6–3.1 V, 170 mA combined; SD_VDD switched). • USB 2.0 moved to the USB0 pads B1 / C1 / C2 / D2. • Wireless corrected to the 2.4 GHz-only BDE-BW3501N. • SD-card path corrected (no on-module series resistors on R3). • Thermal and checklists updated. • Operating temperature − 40 °C to +75 °C. • Added the I^2C0 and identity EEPROM design rules. • Corrected the backlight feedback voltage (200 mV) and the `BL_LED_A` 36 V hazard, CAN pad function per assembly variant, `SD_DET` / `SD_RST` handling, Ethernet LED bootstrap pins, the ADC reference note, and the DSI resolution claim. • Added the debug header pinout. • Final R3 design: ▸ `MODULE_EN` / `MODULE_STBY` now accept 1.8 V, 3.3 V and 5 V logic (circuits, do and don't lists and checklists rewritten; the N-MOSFET buffer is kept only for a host that can be unpowered while the module stays up)	October 2026

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Revision	Changes	Date
	▸ standby currents updated (STOP 3.84 µA, self-off 1.14 µA, carrier-off 2.94 µA) ▸ the on-module RTC backup supercapacitor is no longer fitted, and +S_CAP (AG15) is connected so the carrier provides the RTC backup (new RTC Backup design subsection, with a trickle-charger safety warning) ▸ thermal text without the − 20 °C to +60 °C rating ▸ P0Rn and brownout wording by module revision ▸ MRAM Secure Enclave warning ▸ Ethernet PHY named TI DP83825 ▸ datasheet link made public.	
0.6	• Module block diagram updated to R3 (RMII Ethernet, Wi-Fi on SPI + IRQ, EEPROM on I^2C0, temperature sensor and RTC buses with level shifter, power section and control pads, secure element removed, Ethos-U85 on E4 / E6 / E8, assembly options dashed).	October 2026
0.7	• Module block diagram layout cleanup: arrowheads unified, stray connection lines removed, I^2C bus junction restored, power section aligned with the module blocks.	October 2026
0.8	• Figures redrawn as schematics: eFuse, 5 V buck converter, carrier reference block diagram, Ethernet connection, CAN-BUS interface; RF antenna, MIPI CSI-2 and MIPI DSI routing drawn as routing-guidance diagrams. • Module block diagram replaced by the shared datasheet figure. • Land pattern figure (shared with the datasheet) redrawn in the E1M specification drawing style. Values unchanged; placed at the full text width. • Pin-out drawing (shared with the datasheet) split into four quarters at one scale, each with the module name, SoC, size, pitch, pad count and a default-function legend inside the module outline, so that every pad name prints at 8 pt. • Land Pattern and Interfaces Overview: pad-frame statement added. • Figure text uses only characters the figure font has: approximate values read “about”, limits read >= / <=, resistances read Ohm / kOhm / MOhm, “Pi matching network” (values unchanged); 5 V buck output capacitors moved right so the R25 value label stays clear of C42. • Tables: cell text set ragged-right instead of justified, so narrow cells no longer stretch the gaps between words; the SoC Variants NPU column is wider so “2 × Ethos-U55 + 1 × Ethos-U85” fits on one line; ranges written with an en dash (for example 4.75–5.25 V, A–AH) no longer print a space after the dash (values unchanged).	October 2026
0.9	• Pad maps, footprints and pad-frame text redrawn: letters down (rows), numbers across (columns), A1 top-left. • Pad assignments unchanged. • Pad frame corrected to the E1M standard (the frame of the E1M specification drawings and of the pinout viewer on alplab.ai): pad letter = row, A–AH top to bottom; pad number = column, 1–34 left to right; A1 top-left at the pin-1 marker, A2 right of A1, B1 below A1, A34 top-right, AH1 bottom-left, AH34 bottom-right. • Land pattern figure (shared with the datasheet) redrawn in that frame: corner pads A1, A34, AH1 and AH34 at their corners, A2 right of A1 and B1 below A1; pad ring three pads deep at the left and right and two pads deep at the top and bottom; keep-out cavity 27.0 mm across and 29.0 mm down. Pad size, pitch, body and stencil values unchanged (the courtyard is 2.0 mm, see the Courtyard entry below). • Pin-out drawing (shared with the datasheet) redrawn in that frame as four quarters at one scale (rows A–Q / R–AH, columns 1–17 / 18–34), placed at the full text width. Pad names unchanged. • Land Pattern and Interfaces Overview: pad-frame statement and band description corrected. • Module outline drawn as a plain 35.0 × 35.0 mm rectangle; A1 is identified by the 0.5 mm triangular pin-1 fiducial, a copper feature like the pads, now drawn in copper in the land	October 2026

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Revision	Changes	Date
	pattern (to scale, 0.2 mm in from the edges) and in the pad maps, and the figure note and pad-frame statement say so. • Mounting: the module is not placed directly on the carrier; a spacer PCB (option a) or a carrier through-cutout 27.0 mm across × 29.0 mm down, R1.00 corners, 4.0 mm from the module's left edge and 3.0 mm from its top edge (option b) is used; the spacer PCB is soldered on both faces (module to spacer, spacer to carrier), and under either option the carrier has no components inside the cavity outline. Dimensions mounting line, Keep-Out Zones (renamed Mounting and Keep-Out Zones), Thermal Design copper-area rule and design checklist updated. • Courtyard: 2.0 mm clearance around the module outline, 39.0 × 39.0 mm overall (was 1.0 mm, 37.0 × 37.0 mm); Land Pattern text and Land Pattern Parameters table updated. • Land pattern figure (shared with the datasheet): the cavity outline is drawn as the option (b) carrier cutout, with its 4.0 mm and 3.0 mm position dimensions and R1.00 corners; courtyard redrawn at 2.0 mm.	
0.10	• Module block diagram (shared with the datasheet): ‣ `I2C[0:1]` (was `I2C[0:2]`) and `SPI0` from the SoC with `SPI1` from the Wi-Fi module (was "2x SPI" / `SPI[0:2]` from the SoC), as in the pin tables ‣ Wi-Fi module GPIOs `IO13`, `IO15`–`IO24` drawn from the Wi-Fi module ‣ pad labels set to the pad names: `ANT_2.4GHZ` (was Antenna), `ETH0` (was Ethernet), `CAN0` (was CAN_BUS), `USB0` (was USB2.0), `SD0` (was µSDHC), `DSI0` (was DSI), `CSI0` (was CSI), `VDD` (was VDD_IN), `MODULE_EN` and `MODULE_STBY` (was MODULE_EN/STBY), `PWM[0:7]`, `ANA_S[0:7]`, `DAC[0:1]` and `ENC[0:3]` (were 8 x PWM, 8 x ADC, 2 x DAC and 4 x Encoder) ‣ SoC block: A32 count per variant, 1 × on E5 / E6 and 2 × on E7 / E8 (was 2 × A32 for every variant), MRAM 5.5 MB and SRAM 13.5 MB (E3 / E5 / E7) / 9.75 MB (E4 / E6 / E8) added ‣ `SD0` drawn through the NVT4858 level translator ‣ `+V_CAM0` / `+V_CAM1` and `CAM_VFB0` / `CAM_VFB1` drawn from the camera LDOs (TLV77201) ‣ `+S_CAP` drawn to the RTC (RV-3028) backup input (was the power section) and `RTC_CLKOUT` added ‣ `CAM_PAR`, `PDM[0:1]`, `AUDIO_CLK`, `DBG_TX/DBG_RX` (SE-UART) and GPIO `IO0`, `IO2`–`IO11` added ‣ OSPI0 memories with size and chip select (NOR flash 256 Mbit on SS1, HyperRAM 512 Mbit on SS0) ‣ EEPROM 128 Kbit ‣ part numbers BDE-BW3501N (CC3501E), DP83825, KTD2801 and TCAN1044AVDRBRQ1 ‣ `BL_LED_A/K` drawn bidirectional (`BL_LED_K` is the driver feedback input) ‣ legend notes for the OSPI memories per variant, the standard-build CAN pads B18 / B19 and the Wi-Fi module pads ‣ white figure background for dark pages.	October 2026
0.11	• Release history: every entry formatted as a bullet list.	October 2026
0.12	• Table of Contents: each entry links to its section; the front-matter lists are set tighter.	October 2026
0.13	• Removed the shut-down community forum; support is by email and the documentation site.	November 2026
0.14	• Product name on page 1 links to the product page on alplab.ai.	November 2026
0.15	• SE-UART: the settings are stated (8N1, 57 600 baud on E4 / E6 / E8, 55 000 baud on E3 / E5 / E7).	November 2026

Table 1 Release History

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1 Introduction

1.1 Purpose of This Document

This Hardware Design Guide provides practical guidance for developers and system integrators designing a carrier board for the **E1M-AEN System-on-Module (SoM)**.

It covers:

- Hardware integration and carrier board design
- Power architecture and system bring-up
- Interface usage and pin functional intent
- Common pitfalls during first implementation

This guide complements:

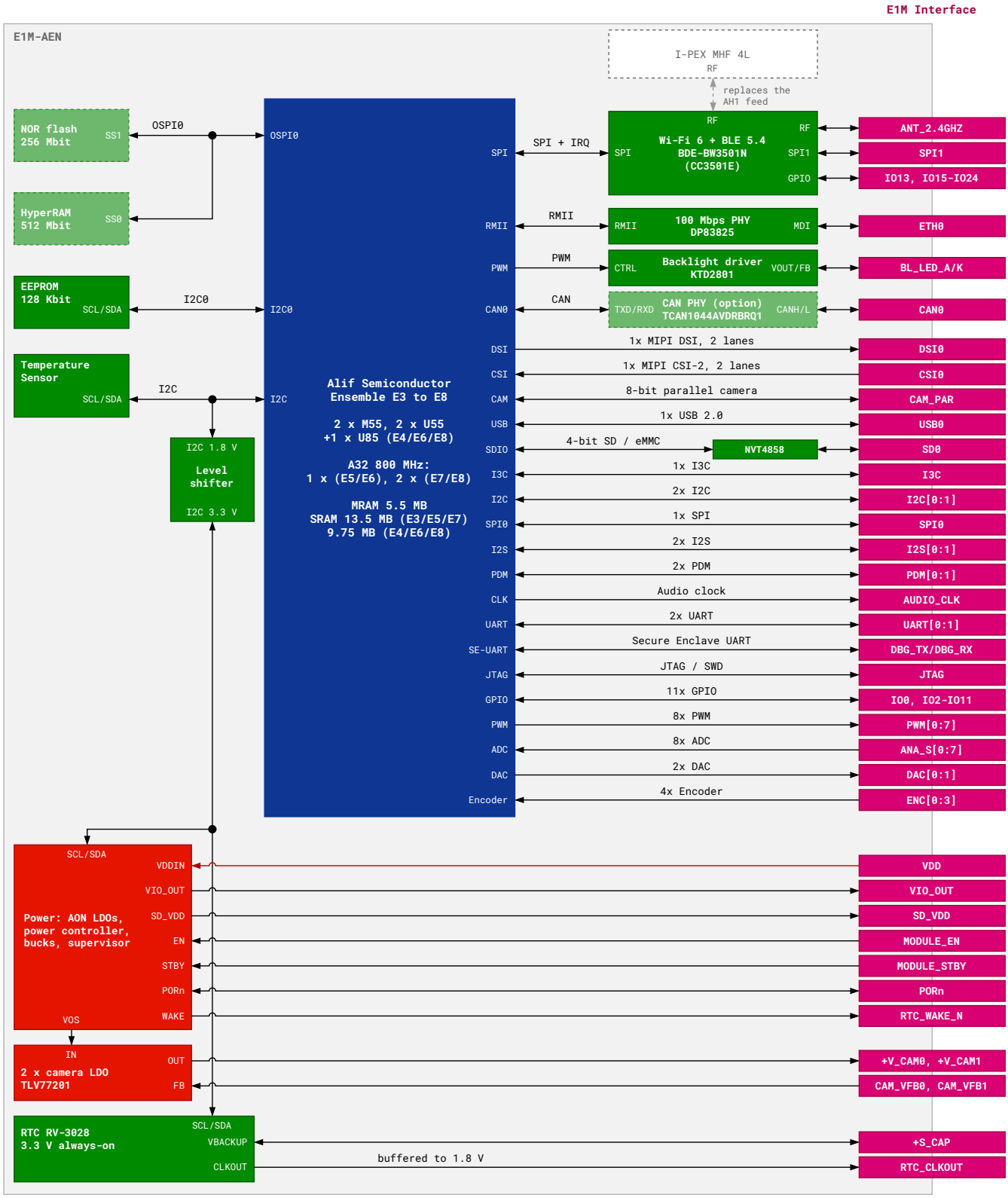
- The E1M-AEN Datasheet
- Alif Semiconductor Ensemble SoC documentation
- Alp SDK™ documentation

1.2 Product Overview

The **E1M-AEN** is a compact **35 × 35 mm Edge-AI System-on-Module**, based on the **Alif Semiconductor Ensemble series**, targeting industrial, IoT, robotics, and low-power AI applications.

The module follows the **E1M™ open-standard pin layout**, enabling drop-in compatibility across the E1M series without redesigning the carrier board.

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Fitted (standard build)

Assembly option (dashed): CAN PHY, I-PEX MHF 4L RF connector, OSPI memories

OSPI memories: fitted on E1M-AEN803, not fitted on E1M-AEN801, build option on E1M-AEN301 / 401 / 501 / 601 / 701

Without the CAN PHY (standard build) B18 / B19 carry the SoC CAN0_TX / CAN0_RX at 1.8 V

SPI1 and IO13, IO15-IO24 belong to the Wi-Fi module: valid only while Wi-Fi is powered

EEPROM shares I2C0 with the E1M I2C0 pads (0x50 / 0x58)

Figure 1 E1M-AEN Block Diagram

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Key characteristics:

- Unified pinout across multiple MCU/MPU variants
- On-module power management with an always-on power controller, real-time clock and self-off; interface EMI/ESD protection is provided on the carrier board (except the SD-card interface, which is protected on-module)
- Single external **5 V supply**; no carrier-side rail sequencing
- Long-term lifecycle orientation

2 Supported SoC Variants

Variant	Application CPU	Real-Time CPU	NPU
E3	—	2 × Cortex-M55	2 × Ethos-U55
E5	1 × Cortex-A32	2 × M55	2 × Ethos-U55
E7	2 × Cortex-A32	2 × M55	2 × Ethos-U55
E4	—	2 × Cortex-M55	2 × Ethos-U55 + 1 × Ethos-U85
E6	1 × Cortex-A32	2 × M55	2 × Ethos-U55 + 1 × Ethos-U85
E8	2 × Cortex-A32	2 × M55	2 × Ethos-U55 + 1 × Ethos-U85

Table 2 SoC Variants

> **Note:** Firmware images must match the installed Ensemble variant.

3 Mechanical Information

3.1 Dimensions

- **Size:** 35 × 35 mm
- **Form factor:** Connectorless, solder-down LGA SoM
- **Mounting:** Land-grid-array (LGA) pads; the module is not placed directly on the carrier board but on a spacer PCB or over a through-cutout in the carrier (see Section 3.3)

The complete mechanical drawing (dimensions, tolerances, height, and mass) is in the **E1M-AEN Datasheet**. The values below are the subset a carrier-board designer needs to lay out the footprint.

3.2 Land Pattern

Design the carrier-board footprint to the recommended land pattern below. The module uses a 1.0 mm pad grid with 0.4 mm round, **non-solder-mask-defined (NSMD)** pads, following IPC-7351 nominal density for LGA packages.

Pad names follow the pad frame of the E1M™ standard (top view, component side up): the pad letter is the row, A to AH from top to bottom, and the pad number is the column, 1 to 34 from left to right. A1 is the top-left pad, next to the 0.5 mm triangular pin-1 fiducial; the module outline is a plain rectangle. A2 is directly to its right and B1 directly below it; A34 is the top-right pad, AH1 the bottom-left pad and AH34 the bottom-right pad. The pad ring is two pads deep along the top and bottom edges (rows A, B and AG, AH) and three pads deep along the left and right edges (columns 1–3 and 32–34), so the pad-free area inside it is 27.0 mm across and 29.0 mm down. The courtyard is 2.0 mm around the module outline (39.0 × 39.0 mm overall); the dashed outline inside the pad ring is the carrier through-cutout of mounting option (b).

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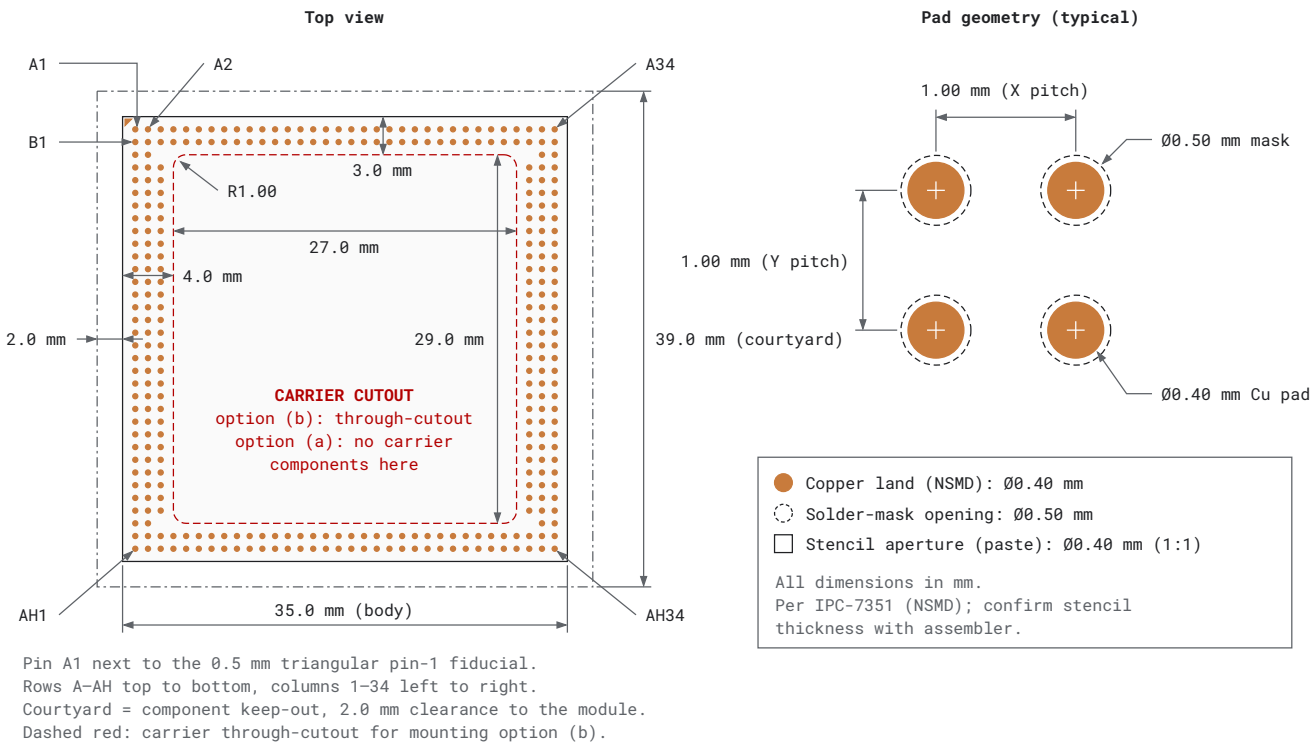


Figure 2 E1M-AEN recommended land pattern (top view)

Parameter	Value	Unit
Pad pitch (signal grid)	1.0	mm
Copper pad diameter	0.40 (dia.)	mm
Pad type	Round, NSMD	—
Solder-mask opening diameter	0.50 (dia.)	mm
Stencil aperture (1:1)	0.40 (dia.)	mm
Stencil material	Nano-coated steel mesh	—
Stencil thickness (recommended)	0.08	mm
Courtyard (2.0 mm clearance to the module outline)	39.0 × 39.0	mm
Carrier through-cutout, mounting option (b) (across × down)	27.0 × 29.0, R1.00 corners	mm
Cutout position from the module left / top edge	4.0 / 3.0	mm

Table 3 Land Pattern Parameters

Tip: A 4-layer (or denser) carrier board is recommended so that signals can be routed out from under the module on inner layers without crowding the top-layer escape routes.

3.3 Mounting and Keep-Out Zones

The module **shall not** be placed directly on the carrier board. Use one of two mounting options:

1. **Spacer PCB** — a spacer PCB between the module and the carrier board. The spacer PCB is soldered on both faces: the module LGA pads to the spacer, and the spacer to the carrier board.
2. **Carrier cutout** — a through-cutout in the carrier board the size of the module's central cavity: 27.0 mm across × 29.0 mm down, R1.00 corners, its left edge 4.0 mm from the module's left edge and its top edge 3.0 mm from the module's top edge (top view), drawn dashed in the land pattern figure.

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The spacer thickness, the module height and the maximum component height on the module bottom side are not specified in this revision (TBD).

Keep-out regions:

- **Courtyard** — keep a 2.0 mm component-free clearance around the module outline (39.0 × 39.0 mm overall) for placement tolerance, inspection, and rework access.
- **Inside the pad ring** — with either option, place no carrier components inside the cutout outline (the cavity outline given above). With a carrier cutout (option b), the area is removed from the carrier; with a spacer PCB (option a), the carrier area under the cavity is kept clear. Signal routing beneath the module is permitted on inner layers and on the top layer between pads, outside the cutout.

Note: Route the RF antenna feed (AH1) away from high-current digital paths, and keep the carrier-board ground pour clear of any on-module or carrier antenna keep-out. See Section 8.2.

3.4 Handling and Assembly

- ESD-sensitive device — use grounded handling equipment
- Avoid mechanical stress after soldering
- Follow standard reflow and PCB flatness rules
- Observe the module's Moisture Sensitivity Level (MSL) and dry-pack floor life; bake before reflow if floor life is exceeded (see the datasheet **MSL & Handling** section)
- The module is supplied in JEDEC matrix trays (no tape & reel)

4 PCB Layout Guidelines

4.1 Layer Stack-Up

The E1M-AEN exposes several controlled-impedance interfaces (100 Ω differential Ethernet and MIPI, 90 Ω differential USB 2.0, and 50 Ω single-ended RF). A **minimum 4-layer** carrier board is recommended; 6 layers eases escape routing and gives cleaner reference planes for high-speed pairs. A typical 4-layer stack-up is:

Layer	Use	Notes
L1 (top)	Signal + components	High-speed escapes, RF trace, module pads
L2	Ground plane	Solid, unbroken reference for L1/L3 high-speed pairs
L3	Power + low-speed signal	Split power pours; keep high-speed off this layer
L4 (bottom)	Signal + ground pour	Slow signals, additional ground stitching

Table 4 Reference 4-Layer Stack-Up

Tip: Reference every high-speed pair to a **continuous** ground plane (L2). Never route a differential pair across a plane split — the return current cannot follow and emissions/cross-talk rise sharply.

4.2 Controlled-Impedance Routing

Set the dielectric heights and trace geometry with your fabricator's impedance calculator to hit the targets below. Match lengths **within** each pair first (intra-pair skew), then across pairs of the same bus (inter-pair skew).

Interface	Impedance	Tolerance	Length matching
Ethernet (10/100)	100 Ω diff	± 10%	Intra-pair ≤ ± 2 ps

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Interface	Impedance	Tolerance	Length matching
MIPI CSI-2 / DSI	100 Ω diff	± 10%	Intra-pair tight; match clock to data lanes in the group
USB 2.0 HS	90 Ω diff	± 10%	Intra-pair ≤ ± 5 ps
RF antenna feed	50 Ω single-ended	± 10%	—

Table 5 Impedance & Skew Targets

- Keep high-speed pairs short and direct; minimize vias (each via is an impedance discontinuity) and avoid stubs.
- Where a pair must change layers, place ground stitching vias adjacent to the signal vias to give the return current a path.
- Keep digital switching noise and high-current paths away from analog, RF, and MIPI routing.

5 Power Architecture & Carrier Power Design

This chapter describes how to design the power and power-control section of a carrier board for an E1M-AEN **R3** module. The carrier supplies one 5 V rail and, optionally, drives two control pins. Everything else (regulators, rail sequencing, brownout handling, reset release, Wi-Fi and SD power) is done on the module. The limits quoted here are the same as in the E1M-AEN Datasheet (DS-AEN-001); the datasheet is authoritative if the two documents ever differ.

Warning: Three rules prevent most carrier power faults: (1) keep `VDDIN` at or below 5.5 V including transients — the module has no input protection; (2) drive `MODULE_EN` and `MODULE_STBY` only with open drain, a switch to GND, or push-pull 1.8 V, 3.3 V or 5 V logic (≤ 5.5 V), and keep their leakage ≤ 0.1 µA; (3) never drive a 1.8 V E1 pad while `VIO_OUT` is low. `MODULE_EN`, `MODULE_STBY` and `RTC_WAKE_N` are exempt from rule (3): they are 5 V tolerant and may be driven or pulled up at any time, also while `VIO_OUT` is low and while `VDDIN` is absent (there is no back-power path; the module boots when 5 V arrives with `MODULE_EN` high). `PORn` may only be pulled low.

5.1 Module Power Domains

Domain	Contents	When it is on
Always-on	Nano-power regulator, real-time clock (backup store on the carrier via +S_CAP), power controller that filters `MODULE_EN` / `MODULE_STBY`, holds the power latch and sequences the rails	Whenever 5 V is present on `VDDIN`
SoC	SoC supplies, 1.8 V I/O rail (`VIO_OUT`), brownout supervisor	Module on (run or STOP). Off in self-off and while `MODULE_EN` is held low
Switched islands	Wi-Fi / BLE module, Ethernet PHY, OSPI memories, SD card supply, camera LDOs	Only when firmware enables them; off by default

Table 6 E1M-AEN Power Domains

The module can switch **itself** off (self-off) while `MODULE_EN` is high, and switch itself on again from an RTC alarm or a `MODULE_STBY` pulse. A carrier therefore must not assume that the module is on because 5 V is present and `MODULE_EN` is high: `VIO_OUT` is the module-on indication.

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5.2 5 V Input Stage

5.2.1 Requirements

Parameter	Min	Typ	Max	Unit
Operating voltage at the VDDIN pads (R1, R2, S1, S2)	4.75	5.0	5.25	V
Absolute maximum, including transients and hot-plug overshoot	–	–	5.5	V
Rise time, 0 V to 4.75 V, monotonic	–	–	40	ms
Source capability, continuous	1.0	–	–	A
Source capability, peak	1.5	–	–	A
Carrier hold-up capacitance at VDDIN (effective, per A of total load on the VDDIN node)	50	–	–	µF/A

Table 7 VDDIN Requirements

The module carries about 50 µF (nominal) of ceramic input capacitance on VDDIN. Include it when you size the carrier inrush limiter or eFuse.

5.2.2 Protection

The module has **no** input protection. Its regulators are rated 6.0 V absolute maximum and its input capacitors 6.3 V. The carrier must provide:

- **Over-voltage protection:** place a TVS at the connector, ahead of an eFuse or load switch with an over-voltage cutoff or clamp, so that VDDIN at the module pads never exceeds 5.5 V, including surges and hot-plug. A TVS alone does not meet this: 5 V TVS diodes clamp well above 6 V at their rated surge current. Size the TVS to protect the eFuse input.
- **Inrush limiting** (eFuse or load switch with a controlled slew), sized for the module input capacitance plus the carrier hold-up capacitance. The ramp must stay monotonic and reach 4.75 V within 40 ms.
- **Reverse-polarity protection** if the 5 V connector can be mis-wired.

The E1M development board uses a **TI TPS25210LRPWR** eFuse for input protection. If you OR redundant supplies, use ideal-diode controllers rather than Schottky diodes, or raise the source voltage to compensate: a Schottky drop from a 5.0 V source (or a 4.75 V USB VBUS) leaves VDDIN below the 4.75 V minimum. Check that ≥ 4.75 V remains at R1 / R2 / S1 / S2 at the 834 mA peak.

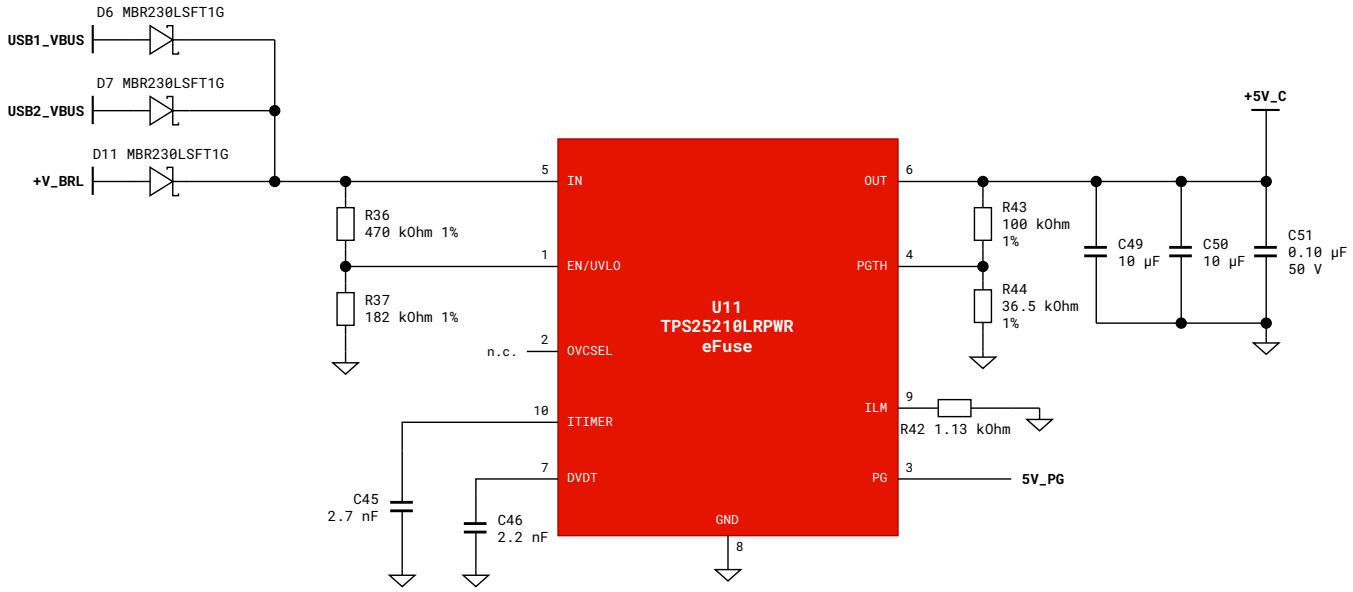


Figure 3 eFuse

5.2.3 Hold-up and Brownout

When 5 V is lost, the on-module supervisor pulls PORn low and switches the SoC off in order. For this to complete before the 1.8 V I/O rail falls below 1.65 V, the 5 V rail must not collapse faster than the module can react. Provide at least 50 µF of effective capacitance per ampere of the **total** current drawn from the VDDIN node: the module load including carrier loads on SD_VDD, VIO_OUT and the camera rails and the on-module backlight driver input current (up to 520 mA), plus any other carrier load connected to the same node after the eFuse (for example ≥ 47 µF effective for the 834 mA module peak alone). Alternatively, isolate the module node from other carrier loads with an ideal diode. Place the capacitors close to the R1/R2/S1/S2 pads after any current-sense shunt or eFuse. Remember that ceramic capacitors lose much of their capacitance at 5 V DC bias; count the effective value.

An unplanned 5 V loss is always handled safely by the module, but writes to MRAM or OSPI flash that are in progress are lost. Products that can lose 5 V during writes (for example a removable supply) should warn the module over an application line before the supply drops, or add enough hold-up to finish the write.

5.2.4 Choosing the 5 V Source

A buck converter can be used to create 5 V for the SoM. Size it for the peak current, not the average: the module draws about 111 mA in full compute, about 372 mA with Wi-Fi transmitting and up to 834 mA when compute and Wi-Fi transmit peaks coincide, plus all carrier loads powered from SD_VDD, VIO_OUT and the camera rails, and the input current of the on-module backlight driver, which runs directly from VDDIN (up to 520 mA input current limit; set by the LED load). The E1M development board generates its rails with **TI TLV62595DMQR** (4 A) and **TI TPS564247DRLR** (6 A) step-down converters.

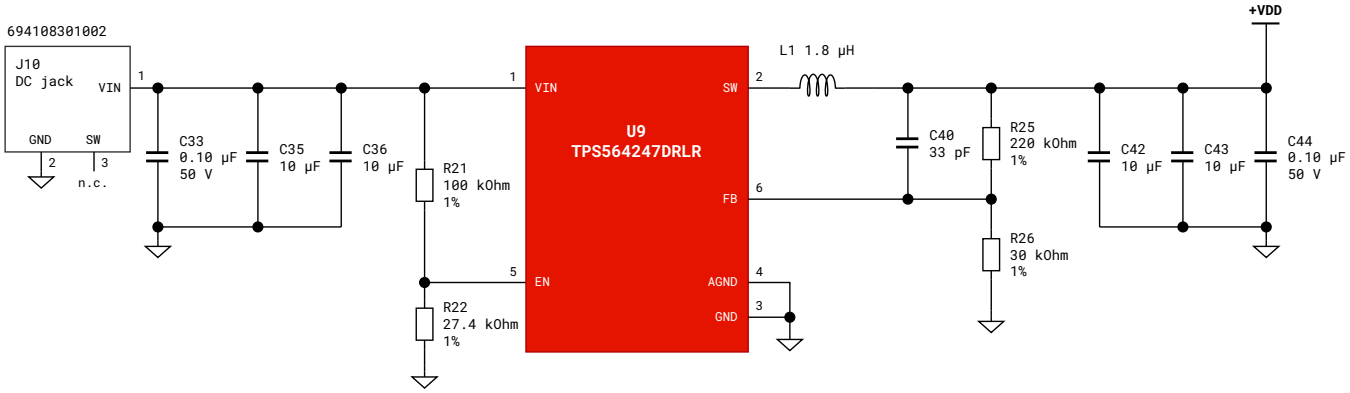


Figure 4 5V Buck Converter

Place a current-sense shunt (if any) so that its drop at the 834 mA peak still leaves ≥ 4.75 V at the module pads. A shunt sized for microampere standby measurements (hundreds of mΩ) drops too much at run current. Use a low-value shunt (≤ 50 mΩ) for normal operation and bypass any high-value measurement shunt automatically (for example a FET that is closed by default, or a Schottky diode in parallel), so that a wake from STOP or self-off never runs through it; switch make-before-break.

5.2.5 Battery-powered Carriers

The module's standby currents are in the microampere range (STOP ≈ 3.84 µA, self-off ≈ 1.14 µA, carrier-off ≈ 2.94 µA, typical, 25 °C, calculated). They rise steeply with temperature (estimated: STOP about 15 µA at 50 °C and about 150 µA at 85 °C; self-off about 3 µA at 50 °C and about 17 µA at 85 °C); size the battery for the warmest storage temperature. In a battery product the carrier's 5 V converter, not the module, usually sets the battery life:

- Use a boost (or buck-boost) converter with sub-microampere quiescent current, or one that can be bypassed in standby.
- Count the converter efficiency at microampere loads, the quiescent current of every always-on carrier part, the leakage of the TVS and ESD diodes, and the battery self-discharge. For multi-year life, a primary lithium cell is usually needed.
- Do not switch 5 V off to save power: the always-on domain (RTC, power controller) needs 5 V to keep time and to wake the module. Use self-off instead. Without 5 V the RTC keeps time only from a backup element that you fit on the carrier at +S_CAP (see Section 5.6); with no backup element, time is lost when 5 V is removed.

5.2.6 Power Layout

- Connect **all** GND pads to a solid, low-impedance ground plane, each with at least one via.

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- Keep the 5 V path from the source to R1/R2/S1/S2 short and wide; place the hold-up capacitors next to the pads.
- Keep the TVS close to the connector and its ground return short.

5.3 Module Output Rails

The module generates these rails **back to the carrier**. They are intended for light carrier loads and camera power, not for powering large external subsystems.

Rail	Pins	Voltage	Max	Notes
VIO_OUT	P1, P2	1.8 V	100 mA	Output only. ≤ 2.5 µF carrier capacitance; ≤ 50 mA in the first 2 ms after it rises. High = module rails up.
+V_CAM0	Z34	0.6 – 3.1 V (adj.)	170 mA combined	TLV77201 LDO, set via CAM_VFB0 (Z33). Switched by firmware, off by default.
+V_CAM1	AB34	0.6 – 3.1 V (adj.)		TLV77201 LDO, set via CAM_VFB1 (AB33). Switched by firmware, off by default.
SD_VDD	AH10	3.4 V	212 mA	SD card supply. Switched by firmware, off by default. No current limit on the module.

Table 8 Module Output Rails

5.3.1 VIO_OUT

`VIO_OUT` is the module 1.8 V I/O rail. Use it in two ways only:

- As the **reference** (VCCA / VREF) of carrier level shifters and as the pull-up rail of 1.8 V signals that connect to the module, so that these go Hi-Z or low together with the module. Choose shifters whose ports are high-impedance when VCCA is off (I_{off} or partial-power-down specified); some pass-gate shifters conduct with VCCA at 0 V.
- As a **status input**: high = module on (run or STOP), low = module off.

Never drive `VIO_OUT` from the carrier and never connect it to another 1.8 V rail. If the carrier needs more than 100 mA or more than 2.5 µF on a 1.8 V rail that must follow the module, generate a carrier 1.8 V rail and switch it with a load switch whose ON input is driven by `VIO_OUT` (for example **TI TPS22916C** or **Diodes AP22916**). Keep any `VIO_OUT` monitor (for example an ADC divider) on `VIO_OUT` itself, not on the switched rail.

> **Warning:** Bulk capacitance on `VIO_OUT` (for example 10 µF plus several 2.2 µF decoupling capacitors on carrier 1.8 V loads) exceeds the 2.5 µF limit and can stop the module 1.8 V rail from starting reliably.

5.3.2 Camera Rails

The camera LDOs run from the module's 3.4 V domain, so each output can be set between 0.6 V and 3.1 V. The two rails together supply at most 170 mA, and at a 3.1 V setting at most 100 mA per rail. At low output voltages the LDO dissipates more: at T_A = 75 °C one rail is limited to about 96 mA at a 1.2 V setting. The rails are off until firmware enables them (Alp SDK™ camera driver).

5.3.3 SD_VDD

SD_VDD has no current limit on the module. A short on SD_VDD overloads the module 3.4 V rail and the module resets repeatedly (no damage). Protect the card socket on the carrier (current-limited switch or fuse) if the card can be hot-plugged or shorted.

5.4 Module States

State	VDDIN	MODULE_EN	VIO_OUT	PORn	I_{VDDIN} typ	Leaves the state on
No 5 V	0 V	–	low	low	0	5 V return; boots if `MODULE_EN` is released. The RTC keeps time only from the carrier backup element
Shutdown	5 V	held low	low	low	2.94 µA	`MODULE_EN` release only

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State	VDDIN	MODULE_EN	VIO_OUT	PORn	I_{VDDIN} typ	Leaves the state on
Self-off	5 V	high or open	low	low	1.14 µA	RTC alarm or timer; MODULE_STBY low ≥ 10 ms (stand-by wake armed by firmware); MODULE_EN low ≥ 2 ms then high
Booting	5 V	high or open	rising	low, then high	mA, firmware dependent	PORn high ≈ 204 ms after the wake event
Run / connected standby	5 V	high or open	high	high	304 µA – 372 mA	firmware, MODULE_STBY, MODULE_EN
STOP	5 V	high or open	high	high	3.84 µA (6.6 µA with MODULE_STBY held low)	MODULE_STBY, RTC, Wi-Fi, IO8 / IO10

Table 9 Module States Seen from the Carrier

Currents are typical at 25 °C, calculated, not yet measured on R3 hardware. The carrier cannot tell run from STOP on these pins; if it needs to know, use an application line on IO8 or IO10.

5.5 Control Pins: Carrier Circuits

The carrier controls the module with MODULE_EN and MODULE_STBY and reads VIO_OUT, PORn and RTC_WAKE_N. All are optional: a carrier that leaves every control pin open gets a module that boots on 5 V insertion.

5.5.1 MODULE_EN (O1)

Function. Low = module forced off and held off (shutdown). A low-to-high transition powers the module on from any state, including self-off. The module filters the pin with a 1.0 ms digital filter on both edges: low pulses shorter than 0.5 ms are always ignored, low pulses of 2 ms or longer always switch the module off.

Module side. The pad is 5 V tolerant (5.5 V maximum). On the module it passes a clamp FET into an always-on 1.8 V rail and has a weak internal pull-up (about 1 MΩ) to the same rail. The module input threshold is 1.25 V. Left open, the carrier-side pad floats to about 1.2–1.5 V, never above 1.8 V. There is nothing to do on the carrier when the pin is unused, and no carrier pull-up is needed.

Do:

- Drive it with an open-drain or open-collector output, a switch, or a button to GND. This is the preferred circuit.
- Push-pull logic from 1.8 V, 3.3 V or 5 V is also allowed: V_{OH} 1.45–5.5 V.
- Drive the low level to ≤ 0.4 V at the E1 pin (at 3.3 µA). The carrier sinks about 1.8 µA from the internal pull-up while the pin is held low.
- Keep the total carrier leakage on the pin ≤ 0.1 µA when it is released, including TVS / ESD diodes and FET leakage. The internal pull-up is weak; a leaky TVS can hold the pin below the module's input threshold.
- If the carrier wants to read the line back, fit its own pull-up: the released level (1.2–1.5 V) exists only on the module side and is too low for most carrier logic.

Don't:

- Don't connect it directly to the GPIO of a host that can be unpowered while the module must stay up. An unpowered host clamps the pin to about 0.5 V through its ESD diodes and turns the module off. Use the N-MOSFET buffer below.
- Don't pull it up to a rail that can be off while VDDIN is present: a pull-up to a rail that is off acts as a pull-down and turns the module off. No pull-up is needed; if you fit one to read the line back, use a rail that is on whenever VDDIN is present.
- Don't use it as a reset button or as the normal way to switch the module off: it is a hard power cut with no notice to firmware (data-loss warning in Section 5.8).

> **Tip: Host that can be unpowered while the module must stay up.** Use a small N-channel MOSFET as an open-drain buffer: gate to the host GPIO with a 100 kΩ pull-down to GND, drain to MODULE_EN, source to GND (the E1M development board

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uses **Diodes DMN31D5UFZ-7B**). Host GPIO high = module off. When the host is in reset or unpowered, the gate pull-down keeps the FET off and the module runs freely. No carrier pull-up is needed on MODULE_EN. The buffer is not needed for voltage-level reasons: a host that is powered whenever the module is powered can drive the pin directly from 1.8 V, 3.3 V or 5 V logic. Choose a FET with $V_{GS(th)}$ max well below the host V_{OH} ($\leq$ 1.0 V for a 1.8 V host) and $I_{DSS} \leq 0.1$ µA at V_{DS} = 1.8 V over the operating temperature range. The 100 kΩ gate pull-down draws 18 µA from a 1.8 V GPIO while it holds the module off; count it in a battery host.

5.5.2 MODULE_STBY (O2)

Function. Active low. Same module circuit, levels and leakage rules as MODULE_EN (5 V tolerant, weak internal pull-up to 1.8 V, 1.0 ms filter, 1.8 V to 5 V push-pull allowed). Firmware selects how the pin is interpreted:

- **Pulse protocol** (button mode): each falling edge is one event — a sleep request while running, a wake while in STOP. A low pulse of $\geq$ 2 ms is recognised; leave $\geq$ 2 ms high between pulses.
- **Level protocol**: low = stay in STOP, high = run. Holding the pin low raises the module standby current (STOP $\approx$ 6.6 µA instead of 3.84 µA).
- **Wake from self-off**: a low pulse of $\geq$ 10 ms. This path goes through the RTC event input, so firmware must arm the stand-by wake before self-off.

The carrier circuit is the same as for MODULE_EN: open drain, a button to GND, a push-pull host output (1.8 V to 5 V) or, for a host that can be unpowered, the N-MOSFET buffer above (host GPIO high = stand-by request). A push-button needs no carrier pull-up and no debounce capacitor; the module filters it and firmware debounces button presses (about 50 ms). Fit only a low-leakage ESD diode on a button line.

5.5.3 PORn (W1)

Function. SoC reset, open drain, wired-AND on the module (100 kΩ pull-up to the module 1.8 V rail, 1 nF on the module). The module releases it about 2 ms after its 1.8 V rail is up, and pulls it low on every power-off and brownout.

Brownout protection: R3 modules (this guide) have an on-module supervisor that holds PORn low while the supply is below 1.65 V, so the carrier needs no brownout circuit and the PORn push-button is optional. R2 modules lack this supervisor; that is a module erratum (E-02, Alif ER004), fixed in R3. Its impact and the R2 workaround are in the E1M-AEN Errata.

Do:

- Read it with a 1.8 V-compatible input: high = SoC out of reset. Use it to decide when the carrier may start driving module pads.
- The input must be high-impedance when its own supply is off (I_{off} rated, or on a rail that is on whenever VDDIN is present). An unpowered input clamps PORn low and holds the SoC in reset.
- To reset only the SoC, pull it low for $\geq$ 2 ms with an open-drain output or a push-button to GND, then release it. The rails, RTC and power latch stay as they are. PORn low stops the SoC with no notice to firmware: a write to MRAM in progress is lost or corrupted. Use it for recovery, not as a normal reset path.

Don't:

- Don't drive it high and don't add a carrier pull-up.
- Don't add capacitance: a 100 nF capacitor on PORn (common on reset buttons) slows the reset release from about 0.1 ms to about 10 ms and delays the reset on a 5 V loss. Fit no capacitor, or $\leq$ 1 nF.

5.5.4 VIO_OUT (P1, P2)

Read it as the module-on signal (see Section 5). Sense it with a high-impedance divider into an ADC, or with a 1.8 V-tolerant GPIO whose supply is on whenever the module can be on. Never use a GPIO of a host that can be unpowered: VIO_OUT then back-powers the host.

5.5.5 RTC_WAKE_N (P3, IO25)

Function. Open-drain output, active low. Goes low on an RTC alarm, timer or stand-by event and stays low until firmware clears the RTC flags. Valid in every power state while 5 V is present; without 5 V the output is off and reads high.

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Carrier circuit. Pull it up to an always-on carrier rail (≤ 5.5 V) with ≥ 10 kΩ and connect it to a host wake input. Use it to wake a carrier host or PMIC on the same RTC event that wakes the module. Size the pull-up for the standby budget (for example 1 MΩ): the pin can stay low indefinitely, for example while MODULE_EN holds the module off with an alarm pending, so use an edge-triggered host wake input. Leave it open if not used.

5.5.6 Reserved Pads Near the Power Pins

- **W3** (RSVD) is the module 1.8 V rail. Never drive, load or jumper it, and never power the module EEPROM through it.
- **U3 / V3** (RSVD) are the 3.3 V programming port (open drain, 4.7 kΩ pull-ups to 3.3 V on the module) of the on-module power controller; the real-time clock sits on the same bus. Only Alp Lab's programming station uses them, with MODULE_EN held low. Leave them open in products; never connect them to a 1.8 V bus.
- **S3** (RSVD) is the Wi-Fi module reset (open drain only); **Q3 / R3 / T3** are its debug port (1.8 V, only while Wi-Fi is powered).
- **BOOT0–BOOT3** (V2, U2, U1, V1) are not connected on E1M-AEN.
- **+S_CAP** (AG15) is the RTC backup input and is connected in the standard build. See Section 5.6. Never leave it floating.
- All other RSVD pads are not connected on R3. Leave them floating for compatibility with later revisions.

5.6 RTC Backup on the Carrier

The module keeps time from 5 V whenever VDDIN is present, including in self-off. The standard module has **no** on-module backup store. To keep time while 5 V is removed, the carrier provides a backup element on +S_CAP (AG15), or none. Choose one of three designs:

Option	Carrier circuit	Firmware setting
Coin cell	BR-type primary lithium cell rated − 40 °C to +85 °C on +S_CAP. Keeps time for years without 5 V.	RTC trickle charger **disabled**
Supercapacitor, up to ≈ 100 mF	Supercapacitor on +S_CAP, rated ≥ 3.3 V. The module charges it from its always-on 3.3 V rail through 15 kΩ, to about 3.05 V. No charging circuit or other source is needed on the carrier: fit only the capacitor. A 47 mF part reaches 2.0 V in about 13 min (time constant about 12 min) and keeps time for about 4.6 days at 25 °C (3.7 days worst case). For room-temperature products: check the capacitor's own temperature range.	RTC trickle charger **enabled**, 15 kΩ (never a lower value)
Supercapacitor, larger than ≈ 100 mF	Carrier charger: 1 kΩ 0402 from the carrier 3.3 V rail (up whenever the carrier has 5 V), then a low-leakage silicon switching diode (for example BAS116, anode on the resistor, cathode on +S_CAP). Do not use a Schottky diode: its reverse leakage at 85 °C reaches the µA range and drains the store. The store charges to about 2.9–3.0 V; 470 mF reaches 2.0 V in about 9 min and keeps time for about 30–40 days at 25 °C. Choose a part rated above the charge voltage.	RTC trickle charger **disabled**, so the module and the carrier never charge at the same time
None	Tie +S_CAP to GND. Do not leave it floating. Time is lost when 5 V is removed.	RTC trickle charger disabled

Table 10 Carrier RTC Backup Options

- The RTC switches to +S_CAP only while the store is above about 2.0 V, and the clock stops when it falls below 2.0 V (2.2 V worst case). That threshold, not the RTC's 1.1 V minimum, ends the backup.
- Size a supercapacitor from the backup time you need: with the RTC load of about 125 nA, allow about 2.3 h per mF between 3.05 V and 2.0 V at 25 °C, and much less at high temperature.

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- The module charger is fixed at 15 kΩ. Never set a lower charge resistance: it drops the RTC supply and puts the RTC's I^2C pins above its supply. Use the carrier charger for stores larger than about 100 mF, or when the backup must be ready within minutes.
- Keep the total leakage on +S_CAP (ESD diode, holder, charger diode, board contamination) ≤ 10 nA. Keep the +S_CAP trace short and away from switching nodes.
- The temperature range of the RTC backup is the range of the element you fit. The module itself is rated − 40 °C to +75 °C.
- The backup type must be configured in firmware to match the hardware: trickle charger off for a primary cell or no store; on, with 15 kΩ, for a supercapacitor.
- A room-temperature assembly option with an on-module backup supercapacitor (− 20 °C to +60 °C) is available on request; contact Alp Lab.

Safety: Never enable the RTC trickle charger, and never fit a carrier charger, when a primary lithium cell is fitted. The charger drives current into the cell, which can then leak, vent or burst. A carrier that can be built with either a coin cell or a supercapacitor must make sure the firmware setting matches the part that is fitted.

5.7 Reference Carrier Configurations

Configuration	MODULE_EN	MODULE_STBY	Deepest state	Notes
A. Always on	open	open	Self-off (≈ 1.14 µA), RTC wake only	Boots on 5 V insertion. After self-off only an RTC alarm or a 5 V cycle wakes it. Firmware that fails to arm a wake leaves the module off until 5 V is cycled: keep VDDIN off for ≥ 1 s for a guaranteed restart (not yet characterised). If the product cannot cycle 5 V, bring MODULE_EN to a test pad or recessed button.
B. One power button	open (optional recessed power-cycle button to GND: a hard power cut)	momentary button to GND	Self-off	Short press while running = sleep, long press = power off (firmware policy); press in STOP = wake; press in self-off = wake if firmware armed the stand-by wake. No carrier pull-up, no debounce capacitor; low-leakage ESD diode only.
C. Host controlled (carrier MCU, PMIC or battery manager)	host open-drain or push-pull output (1.8–5 V)	host open-drain or push-pull output (1.8–5 V)	Shutdown (≈ 2.94 µA) or self-off	Host reads VIO_OUT and PORn for state; RTC_WAKE_N to a host wake input with a pull-up to the host always-on rail. Buffer MODULE_EN with the N-MOSFET circuit if the module must stay up while the host is unpowered.

Table 11 Reference Carrier Configurations

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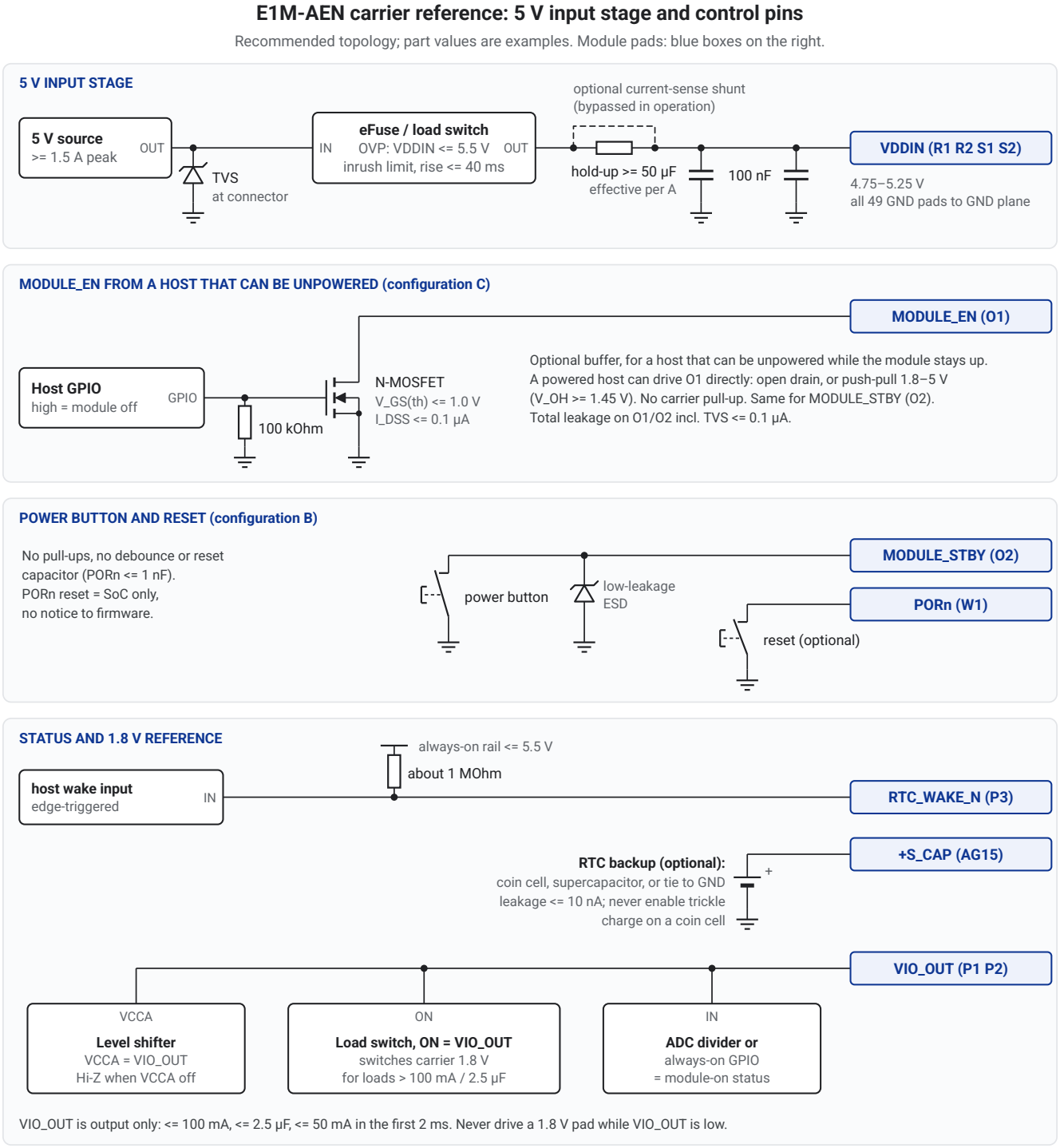


Figure 5 Carrier reference circuit: 5 V input stage and control pins

5.8 Power Sequences

No power-rail sequencing is required; the module sequences its own rails. The carrier only has to respect the order of its **control** and **I/O** signals.

Parameter	Min	Typ	Max	Unit
`VDDIN` rise, 0 V to 4.75 V, monotonic	–	–	40	ms
`MODULE_EN` low pulse that is always ignored	–	–	0.5	ms

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Parameter	Min	Typ	Max	Unit
MODULE_EN low time that always powers the module off	2	—	—	ms
MODULE_EN low time for a full power cycle	25	—	—	ms
MODULE_EN high time after a low that always boots the module	2	—	—	ms
MODULE_STBY low pulse: sleep request, or wake from STOP	2	—	—	ms
MODULE_STBY high time between pulses	2	—	—	ms
MODULE_STBY low pulse: wake from self-off	10	—	—	ms
PORn reset pulse from the carrier	2	—	—	ms
VDDIN reaching 4.75 V, or MODULE_EN released, to PORn high	—	206	290	ms
Wake event (RTC, MODULE_STBY) in self-off to PORn high	—	204	—	ms
Carrier pads Hi-Z after PORn falls (recommended)	—	—	1	ms

Table 12 Carrier Control Timing

A MODULE_EN low pulse of 2 ms to less than 25 ms restarts the SoC with the module 3.4 V rail kept up; use ≥ 25 ms for a full power cycle.

5.8.1 Power-up

1. First, apply 5 V to VDDIN with MODULE_EN released. A carrier that wants the module to stay off holds MODULE_EN low **before** 5 V arrives.
2. Then wait for VIO_OUT high and PORn high (206 ms typical, 290 ms maximum).
3. Only then drive module pads (UART, I^2C, SPI, GPIO, debug). Until then keep every carrier output that connects to the module Hi-Z or low.

5.8.2 Sleep and Wake (STOP)

1. Pull MODULE_STBY low for ≥ 2 ms (pulse protocol) or hold it low (level protocol). The module enters STOP; VIO_OUT and PORn stay high.
2. While the module is in STOP, keep carrier pads in a defined state and stop clocking them.
3. To wake, give a second pulse (pulse protocol) or release the pin (level protocol). An RTC alarm, Wi-Fi traffic or a level change on IO8 / IO10 also wakes the module.

5.8.3 Graceful Power-off (preferred)

1. First, request the power-off over the application link, on IO8 / IO10, or with a long MODULE_STBY press (firmware policy).
2. Firmware finishes its writes, arms its wake sources and switches the module off (self-off).
3. Next, the carrier sees PORn fall and puts its pads Hi-Z within 1 ms.
4. Then VIO_OUT decays. The module is in self-off (≈ 1.14 µA) and keeps time while 5 V is present.
5. If PORn is still high after the firmware's shutdown time (2 s is a sensible host timeout), fall back to the forced power-off.

5.8.4 Wake from Self-off

Give a MODULE_STBY low pulse ≥ 10 ms, or pulse MODULE_EN low ≥ 2 ms and release it, or let the RTC alarm fire. RTC_WAKE_N goes low on RTC and stand-by wakes. PORn rises about 204 ms after the event; then drive pads as in power-up.

5.8.5 Forced Power-off (recovery)

Pull MODULE_EN low for ≥ 2 ms. PORn falls about 1 ms after the falling edge. Hold it low for ≥ 25 ms for a full power cycle, or keep it low to hold the module off (shutdown, ≈ 2.94 µA); release it to cold-boot.

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> **Warning:** MODULE_EN low is a hard power cut with no notice to firmware. A write to MRAM or to the OSPI flash in progress at that moment is lost or corrupted. Use the graceful power-off and keep MODULE_EN for recovery and for holding the module off.

5.8.6 SoC Reset Only

Pull PORn low for ≥ 2 ms with an open-drain output, then release it. The module rails, the RTC and the power latch stay as they are. No notice reaches firmware: an MRAM write in progress is lost or corrupted.

5.8.7 Removing 5 V

First power the module off (graceful, or forced when the data does not matter) and wait for VIO_OUT low. Then remove VDDIN. An unplanned 5 V loss is handled by the module, but writes in progress are lost.

5.9 Back-powering Rules

A carrier signal that is high while the module's rail for that pad is off feeds current into the module through the pad's ESD diodes. This can damage the module, corrupts the power-up order and spoils the standby current.

- Never drive an E1 pad while VIO_OUT is low. Reference carrier level shifters to VIO_OUT and put carrier outputs Hi-Z within 1 ms after PORn falls.
- The Wi-Fi module pads (IO13, IO15–IO24 and SPI1: AG8, AG9, AG10, AH8, AH9) are powered only while Wi-Fi is on, also when the SoC runs. Never drive them while Wi-Fi is off. Pull-downs are fine; avoid pull-ups (a 10 kΩ pull-up to 1.8 V costs about 0.13 mA, against a 3.84 µA STOP budget). If one is unavoidable, use ≥ 100 kΩ to VIO_OUT.
- IO8 / IO9 / IO10 / IO11 are SoC pads: drive them only while VIO_OUT is high.
- PORn: no carrier pull-up, never driven high.
- A debugger connected to the 1.8 V JTAG/SWD pads must use VIO_OUT as its target reference and keep its outputs Hi-Z while VIO_OUT is low. Disable any target-power output of the probe: VTref must be a sense input only.
- Count every carrier pull-up and static load on module pads in the standby budget.

5.10 Power Bring-up on a New Carrier

1. Before the module is fitted, check the 5 V rail at the module pads: level, ramp (monotonic, ≤ 40 ms), overshoot at hot-plug (≤ 5.5 V) and the TVS part number.
2. Fit the module. Hold MODULE_EN low, apply 5 V with a 300 mA current limit and check that VIO_OUT stays below 0.3 V and the current is in the microampere range.
3. Release MODULE_EN. Check VIO_OUT rises to 1.8 V and PORn goes high after about 206 ms (≤ 290 ms). Then raise the current limit to ≥ 1.5 A.
4. Check that no carrier output drives a module pad before PORn is high (scope the busiest lines at power-up).
5. Pulse MODULE_EN low for 25 ms: PORn must fall about 1 ms after the falling edge and the module must cold-boot on release.
6. With firmware that supports it, check STOP (MODULE_STBY pulse) and self-off with an RTC wake, and measure the standby current with a high-value shunt (see Choosing the 5 V Source).
7. Finally, pull 5 V under full load and check that PORn falls before VIO_OUT drops below 1.65 V (hold-up capacitance).

6 Memory and Boot Architecture

6.1 Internal Memory (SoC-Dependent)

- **SRAM:** 128 KB – 13.5 MB
- **MRAM:** 256 KB – 5.5 MB

6.2 On Board Memory (ON SoM)

- OSPI interface supported

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- E1M-AEN803 carries 512 Mbit HyperRAM and 256 Mbit NOR flash on the module
- Other variants: see the datasheet memory information; the configuration depends on the E1M variant

Note: Contact Alp Lab for additional information and configuration.

6.3 BOOT

- BOOT pin functionality is not supported on E1M-AEN. Alif SoCs have no boot-mode strap pins; leave BOOT0–BOOT3 floating.
- The boot ROM loads the application image from internal MRAM. External boot sources (OSPI flash, SD card) are selected in software once the boot ROM is running.
- For MODULE_EN and MODULE_STBY carrier wiring, see Control Pins: Carrier Circuits in Section 5.

6.4 JTAG / SWD Debug

Expose the module's 5-pin JTAG/SWD interface on the carrier for programming and debug. Signals operate at **1.8 V** — add carrier-board level shifters if your debug probe drives 3.3 V.

Also expose the **SE-UART** (DBG_TX AD3, DBG_RX AE3), the Secure Enclave UART of the Ensemble SoC. It is the second programming path (Alif Security Toolkit) and carries the Secure Enclave console. It is a 1.8 V interface on dedicated pins, not GPIO; the module fits 33 Ω in series on TX and 1 kΩ in series plus a 1 MΩ pull-up to 1.8 V on RX. Use a 1.8 V USB-UART referenced to VIO_OUT, and keep its TX Hi-Z while VIO_OUT is low. An unpowered carrier USB-UART loads the RX pull-up by a few µA; count it in the standby budget or isolate it. SE-UART settings: 8N1 at 57 600 baud on the E4, E6 and E8 variants (E1M-AEN401, E1M-AEN601, E1M-AEN801, E1M-AEN803) and at 55 000 baud on the E3, E5 and E7 variants (E1M-AEN301, E1M-AEN501, E1M-AEN701); the Alif Security Toolkit negotiates the rate during its handshake. A wrong rate gives the toolkit error `Target did not respond`.

MRAM and the Secure Enclave: If you program MRAM yourself (Alif Security Toolkit over the SE-UART, or production-test, logging and factory-reset code), stay out of the top of the application MRAM. The Secure Enclave owns the boot table (ATOC) in the 32 KiB band `0x80578000–0x8057FFFF`, directly below the window end at `0x80580000`, and the toolkit places it there at provisioning time. Erasing or writing into that band can leave the module unbootable. Keep every erase range below `0x80578000`; the Alp SDK application `storage` partition (96 KiB at `0x80560000`) ends below it. Firmware built for an earlier SDK may declare a larger `storage` partition that overlaps the boot table: rebuild it first.

Pin	Signal	Description
X1	JTAG_TCK / SWDCLK	Test clock (JTAG) or serial-wire clock (SWD).
X2	JTAG_TDI	Test data in (JTAG only).
Y1	JTAG_TMS / SWDIO	Test mode select (JTAG) or serial-wire I/O (SWD).
Y2	JTAG_TDO	Test data out (JTAG only).
Z1	JTAG_nRST	Active-low system reset request from the probe, open drain. 20 kΩ pull-up to 1.8 V on the module; no carrier pull-up.

Table 13 JTAG / SWD Pinout

Tip: Bring the JTAG/SWD signals out to a standard 10-pin 1.27 mm Cortex debug header (e.g. Samtec FTSH-105). The E1M development board uses this footprint. Use VIO_OUT as the debugger's target-voltage reference, and disable the probe target-power output.

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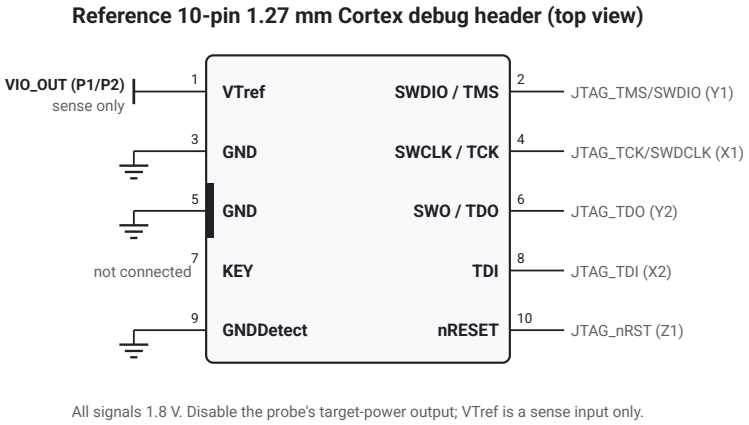


Figure 6 Reference JTAG / SWD Header Pinout

7 Carrier Board Reference Block Diagram

The carrier board has been designed around the **E1M™** open standard to support all E1M variants. Note that E1M-AEN does not implement every peripheral available in the full **E1M™** pinout (e.g. PCIe, the second Ethernet/CSI/DSI, and USB SuperSpeed are not bonded) — see the datasheet **Not-connected Pins** table.

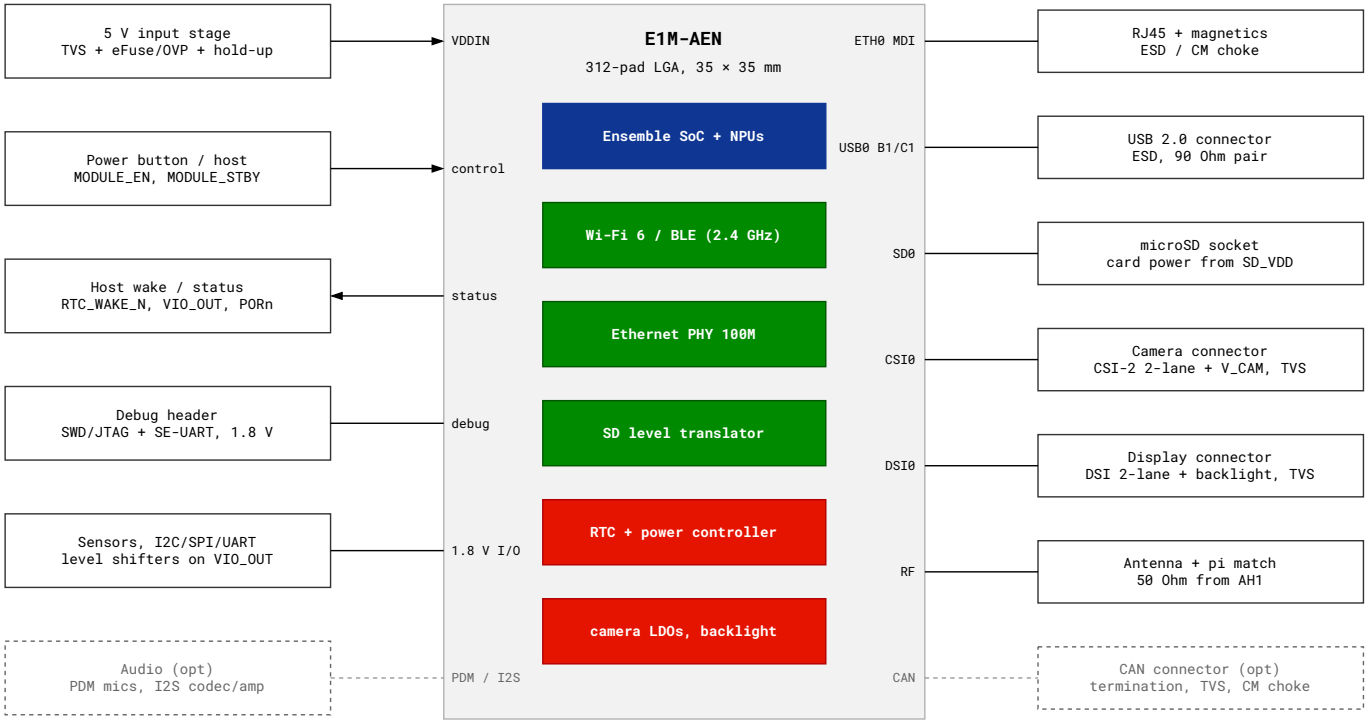


Figure 7 E1M-AEN carrier board reference block diagram

7.1 System-Level Overview

The carrier board provides:

- 5 V power input and protection
- External connectors and signal conditioning
- Application-specific peripherals

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All complex power, RF, EMI, and processing functions are integrated into the E1M-AEN module.

7.2 Design Philosophy

- Keep the carrier board simple and application-specific
- Avoid duplicating functionality already on-module
- Enable reuse across Ensemble variants
- Minimize RF, power, and EMI risk on the carrier board

8 Interfaces Overview

All interfaces are exposed through the standardized **E1M™ pinout**. The pin-out drawings below show the pad locations; the full per-pin tables (Power & Control, Analog, Digital, Not-connected, Reserved) are in the **E1M-AEN Datasheet** and are the authoritative reference for carrier layout. The drawings use the same pad frame as the land pattern: pad letter = row (A–AH, top to bottom), pad number = column (1–34, left to right), A1 at the top-left. The pad band is two pads deep along the top and bottom edges (rows A, B and AG, AH) and three pads deep along the left and right edges (columns 1–3 and 32–34); pads C3, AF3, C32 and AF32 are not fitted. The map is split into four quarters (rows A–Q / R–AH, columns 1–17 / 18–34), drawn at one scale, so that every pad name stays legible.

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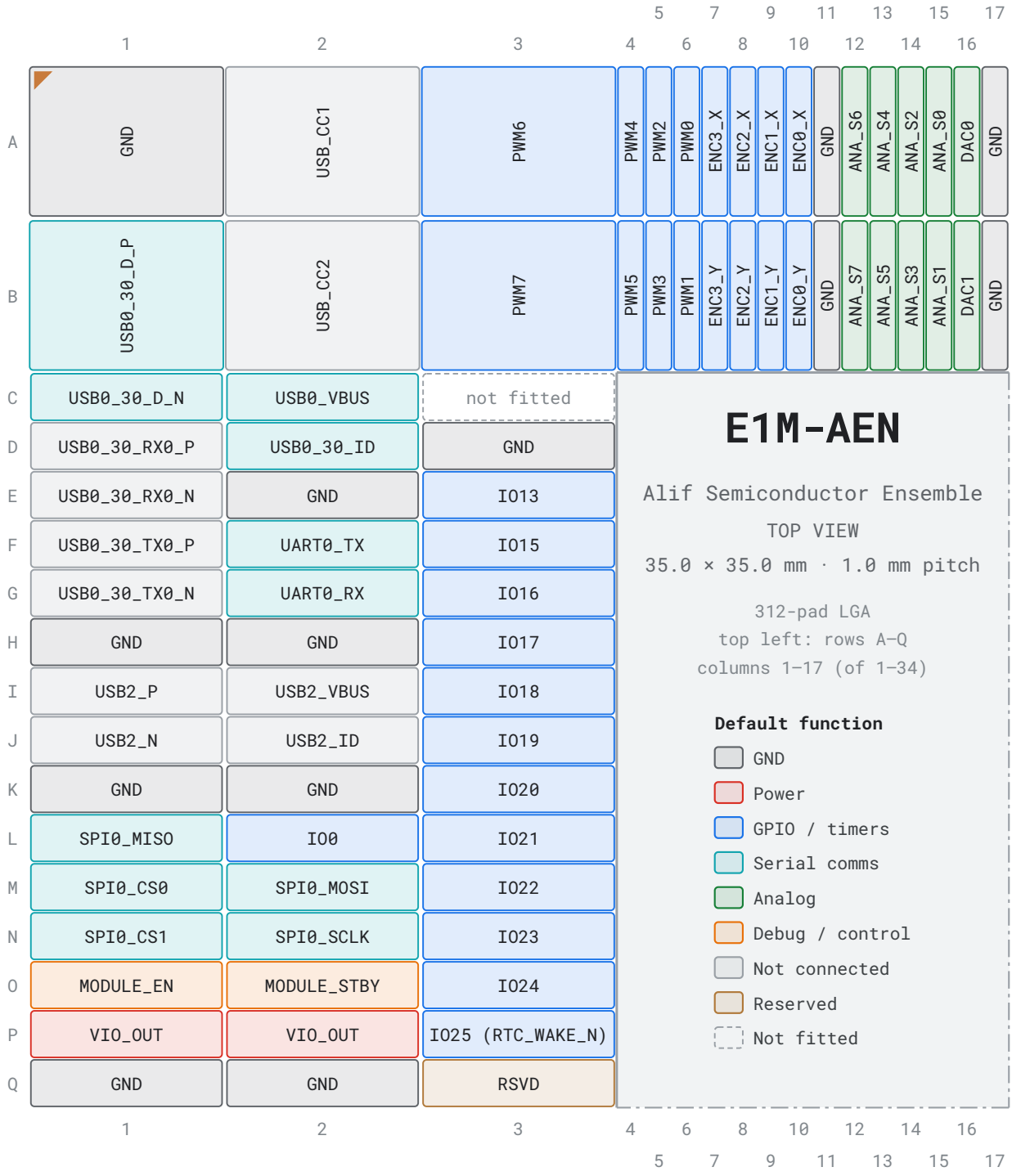


Figure 8 E1M-AEN pin-out (top view, 312-pad LGA), top left: rows A–Q, columns 1–17

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Figure 9 E1M-AEN pin-out (top view, 312-pad LGA), top right: rows A–Q, columns 18–34

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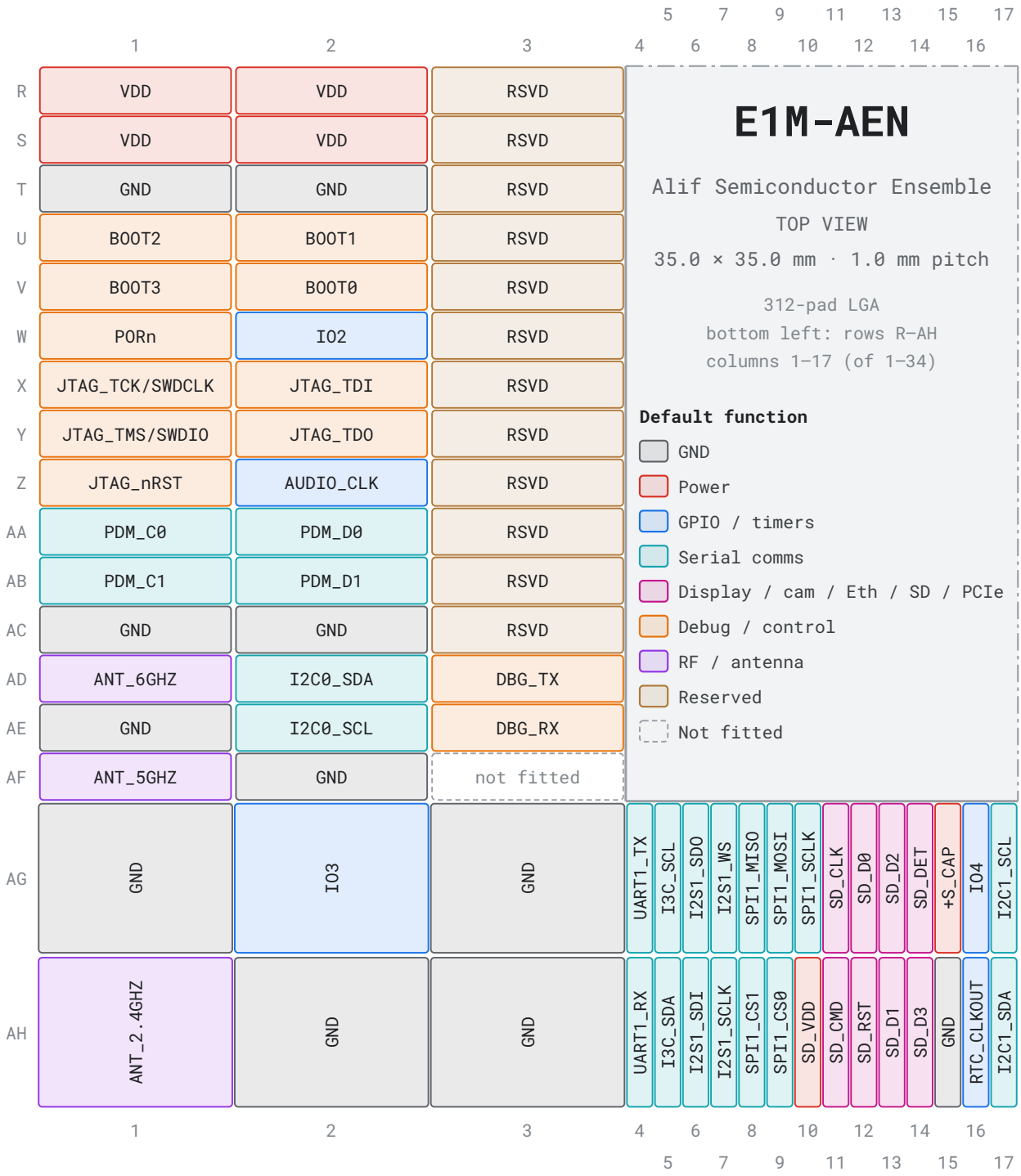


Figure 10 E1M-AEN pin-out (top view, 312-pad LGA), bottom left: rows R–AH, columns 1–17

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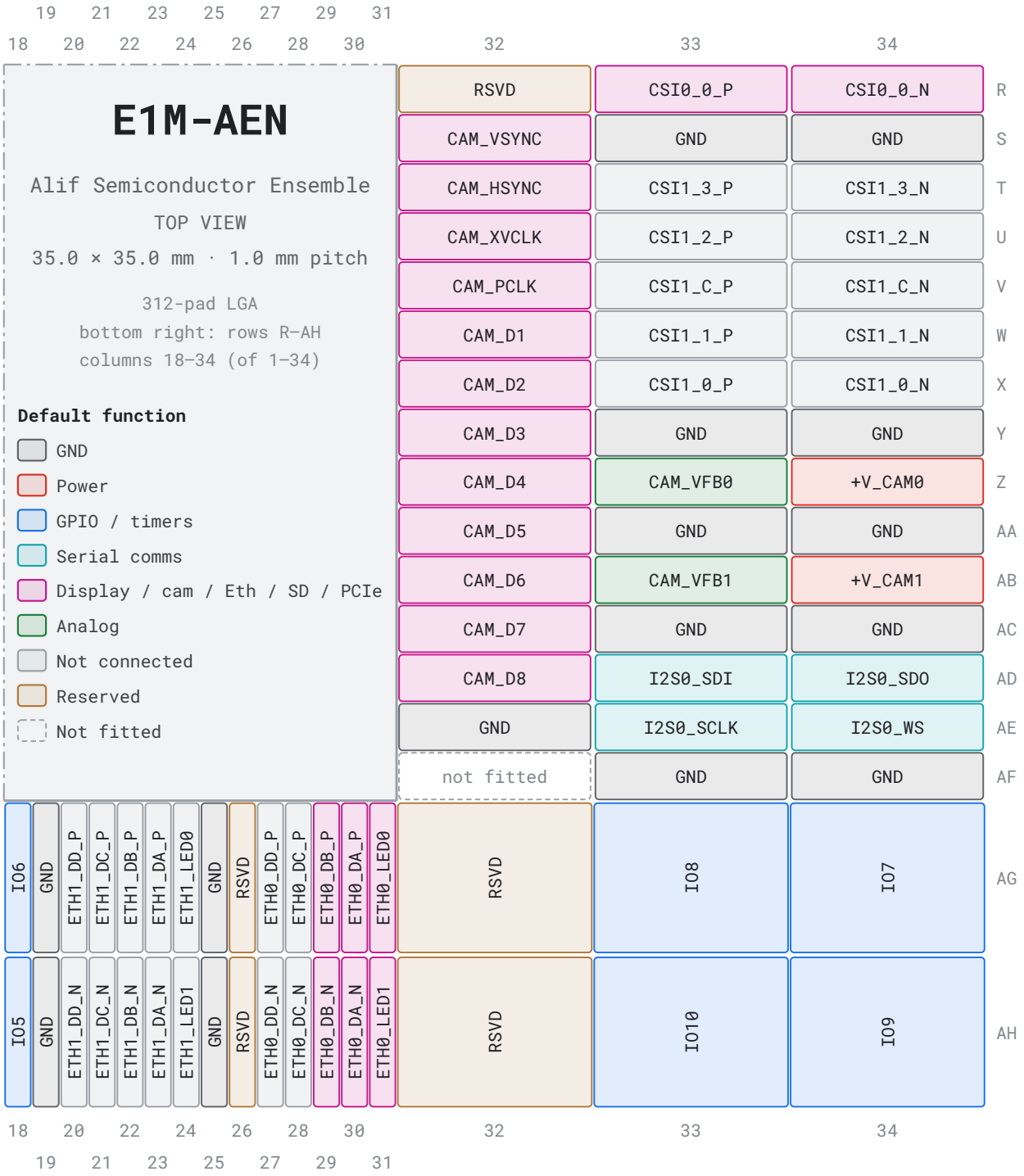


Figure 11 E1M-AEN pin-out (top view, 312-pad LGA), bottom right: rows R–AH, columns 18–34

Note: Check the E1M-AEN datasheet and the E1M™ specification for the authoritative pin map and electrical limits. Pins can be reassigned to alternate functions in software, but hardware compatibility with other E1M variants then no longer holds.

8.1 Ethernet Interface

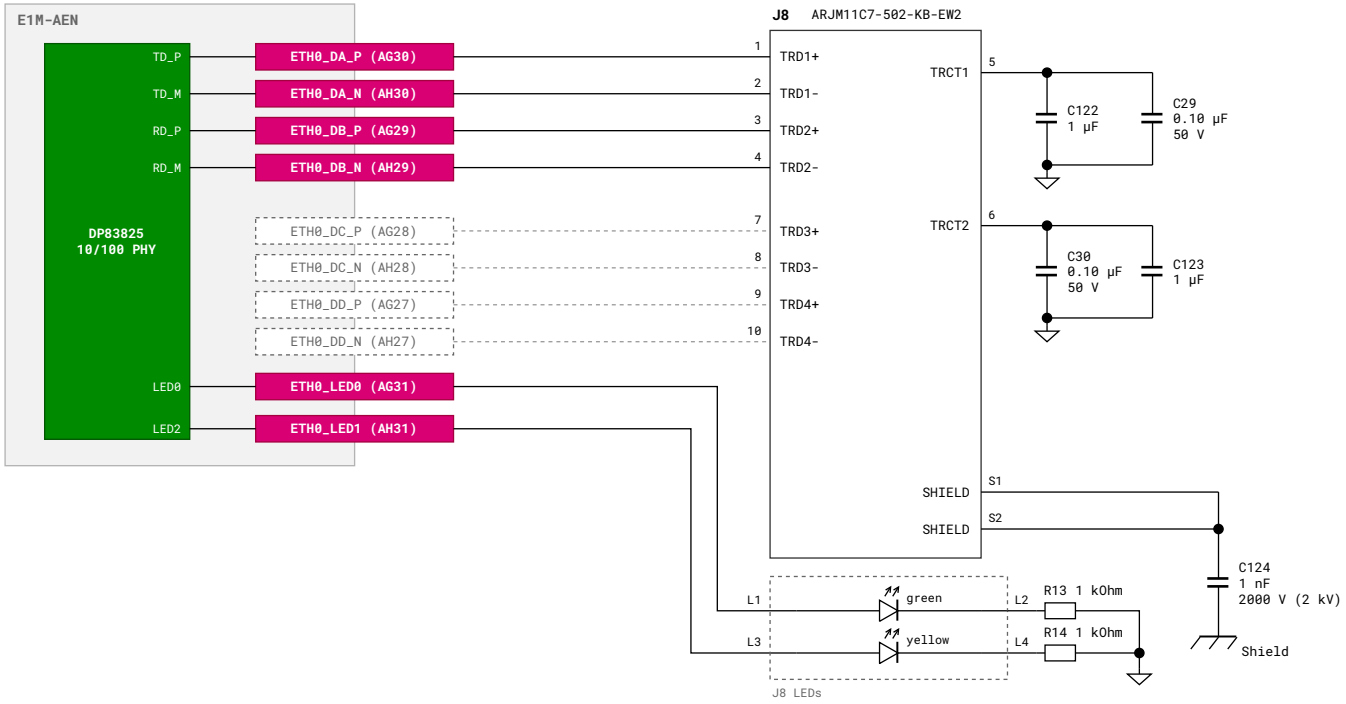
- 100 Mbps Ethernet via on-module PHY (TI DP83825)
- External magnetics and RJ45 required

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- Auto-negotiation enabled by default. ETH0_LED0 (AG31) and ETH0_LED1 (AH31) are also DP83825 bootstrap pins (auto-negotiation disable, RX_DV enable): wire the carrier LEDs so that they do not change the strap levels at reset (see the DP83825 datasheet).
- EMI/ESD protection required on the carrier board

Route ethernet lines with 100Ω in differential pairs. Make sure the match the length within each pair with ±2ps tolerance. The module does not integrate Ethernet ESD/EMI protection — add a low-capacitance ESD/TVS array (and common-mode choke as needed) on the MDI lines between the magnetics and the connector.

The E1M development board uses an **Abracon ARJM11C7-502-KB-EW2** integrated-magnetics RJ45 jack (2 kV isolation); any equivalent 10/100 magnetics jack with the same pinout may be substituted.



MDI pairs ETH0_DA, ETH0_DB: 100 Ohm differential, length matched within each pair (<= ±2 ps). ETH0_DC / ETH0_DD: not connected on E1M-AEN (100 Mbit). ETH0_LED0 / ETH0_LED1 are also DP83825 bootstrap pins: do not pull them up. ETH0_LED0: 3.3 V output (PHY 3.3 V domain). ETH0_LED1: 1.8 V output (PHY VDDIO): for an LED whose forward voltage is near or above 1.8 V, drive it through a transistor or buffer.

Figure 12 Ethernet connection

Note: Ensemble Series supports only **1** ethernet interface. Hence only primary ethernet interface can be used on the SoM.

8.2 Wi-Fi and BLE

- 2.4 GHz Wi-Fi 6 and BLE 5.4 via BDE-BW3501N module (TI CC3501E)
- External antenna required
- Impedance-controlled RF routing
- Keep digital noise away from RF paths

In the standard build the module's antenna feed is brought out on the ANT_2.4GHZ pad (AH1). It can be routed:

1. **Carrier-board PCB / chip antenna** — route AH1 out as a 50 Ω controlled-impedance coplanar trace to an antenna on the carrier. Surround the AH1 landing with GND and place a pi matching network next to the antenna.
2. **Carrier-board RF connector** — extend the 50 Ω trace to a U.FL / IPEX / SMA connector.
3. **On-module I-PEX MHF 4L connector** (assembly option) — the RF output is routed to the on-module connector instead of AH1.

The ANT_5GHZ (AF1) and ANT_6GHZ (AD1) pads are **not used** on E1M-AEN (2.4 GHz only) — leave them floating.

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Route the RF trace with 50 Ω impedance, keep it short and away from noise sources and other components, and add via shielding (a ground fence) along the trace. Follow the antenna vendor's design guidelines.

The E1M development board feeds the RF output through a **Samtec RSP-122811-01** U.FL connector and a 3-element π-matching network (**Murata LQW15AN22NH**, 22 nH) to an **Ignion NN02-201** multiband chip antenna (4.1 dBi, 824 MHz – 7.125 GHz). Populate the matching network footprints and tune per the antenna vendor's guidelines.

Warning: The on-module wireless certifications apply only when the module is used with a certified antenna. Using an unlisted antenna voids the modular grant and requires re-certification on the end product. See the datasheet **Regulatory Information**.

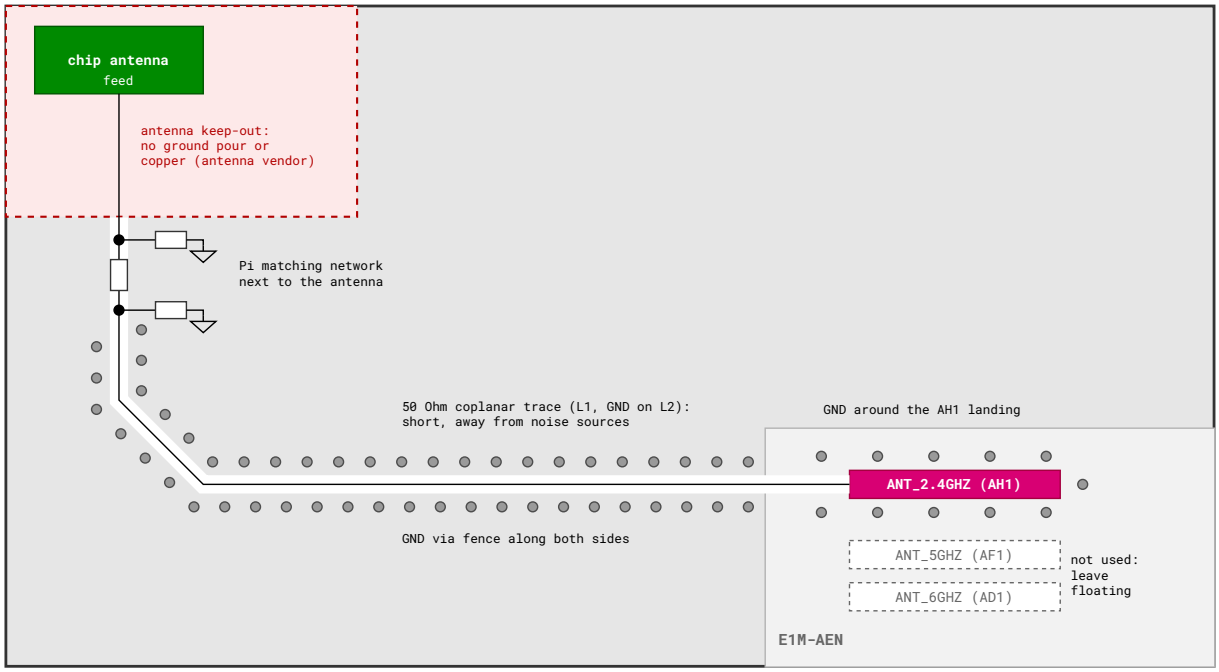


Figure 13 RF antenna routing

8.3 MIPI CSI-2 Camera

- Single-camera support
- 2-lane MIPI CSI-2
- Controlled-impedance differential routing
- Minimize vias and stubs

Ensemble series has one CSI-2 interface for a camera input. The traces must be routed as 100Ω ±10% differential. Make sure the match the lengths within the pairs and the group.

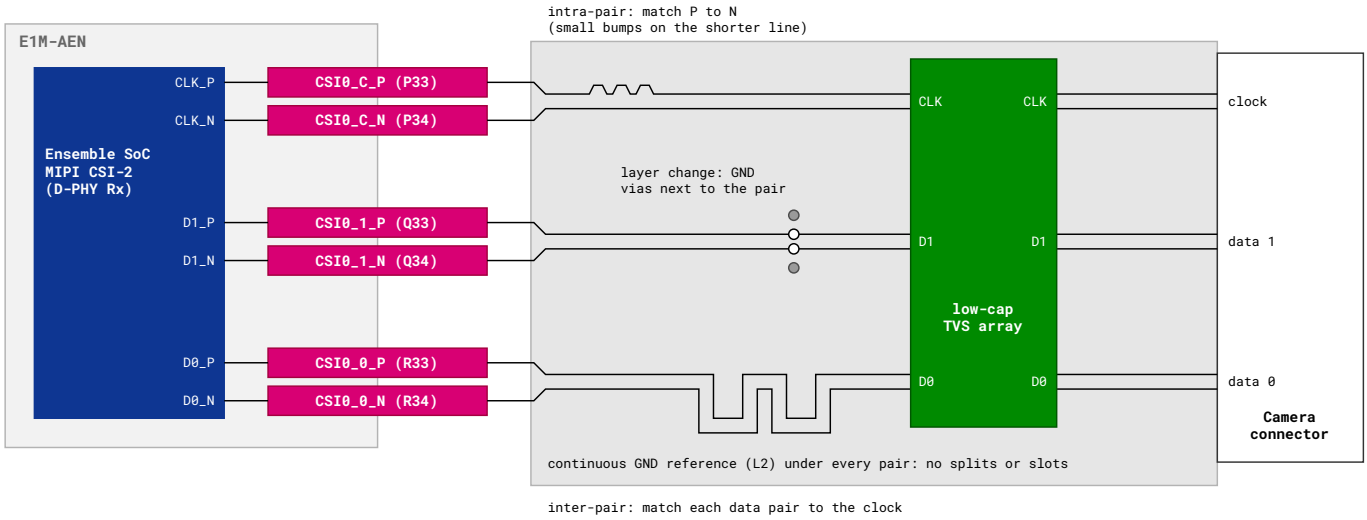
Protect the CSI lanes with a low-capacitance TVS array (the E1M development board uses **Semtech RCLAMP3552T.TNT**). Where a single CSI port is shared between multiple camera connectors, the development board switches the lanes with a **Diodes PI3WVR626XEBEX** MIPI mux.

Camera power. The module's two adjustable LDO rails (`+V_CAM0` / `+V_CAM1`, TLV77201; 0.6–3.1 V, 170 mA combined, off until firmware enables them) can supply the camera directly, avoiding a carrier-side regulator. Set each output with an external divider on the `CAM_VFBx` feedback pin, placed as close to the pin as possible:

$$V_{\mathrm{CAM}} = 0.6\ \mathrm{V} \times \left(1 + \frac{R_1}{R_2}\right)$$

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To keep feedback-pin current error small, size the divider for ~ 100 × the maximum feedback-pin current ($I_{\mathrm{FB,max}} = 100\ \mathrm{nA}$), i.e. $R_1 + R_2 \leq \frac{V_{\mathrm{OUT}}}{I_{\mathrm{FB}} \times 100}$.



All CSI0 pairs: 100 Ohm ±10 % differential. Keep pairs short; minimise vias and avoid stubs. Match within each pair first, then across the pairs (clock to the data lanes). E1M development board TVS array: Semtech RCLAMP3552T.TNT.

Figure 14 MIPI CSI-2 routing example

8.4 MIPI DSI Display

- 2-lane MIPI DSI
- Up to 1.25 Gbps per lane (video mode only); maximum panel resolution set by the pixel clock and link bandwidth (see the datasheet)
- Display power managed externally

Ensemble series has one DSI interface for a display output. The traces must be routed as 100Ω ±10% differential. Make sure the match the lengths within the pairs and the group.

Protect the DSI lanes with a low-capacitance TVS array (the E1M development board uses **Semtech RCLAMP3552T.TNT**). High-speed lane switching to multiple display connectors is handled on the development board by a **Diodes PI3DBS12212AXUAEX** differential mux.

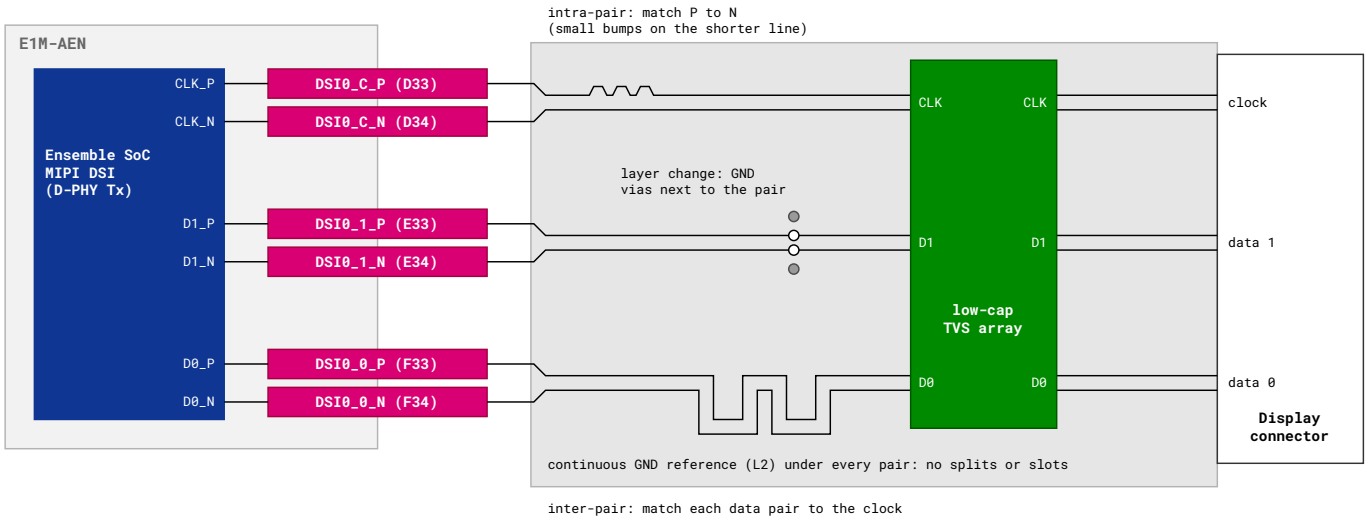
Backlight. The module includes an optional backlight boost driver (up to 10 LEDs in series, or 2P6S; 36 V over-voltage protection), enabled by the Alp SDK™. Connect the LED string anode to BL_LED_A (A31) and its cathode, through R_{FB} to GND, at BL_LED_K (B31). Set the LED current with the feedback resistor, placed on the carrier between BL_LED_K (B31) and GND:

$$I_{\mathrm{LED}} = 200 \frac{\mathrm{mV}}{R_{\mathrm{FB}}}$$

BL_LED_A carries the boost output (up to 36 V): never connect it to a logic input, and rate the carrier traces and connector for it.

On the assembly variant without the on-module driver, BL_LED_A (A31) instead carries the 1.8 V backlight PWM (BL_PWM) from the SoC for an external backlight driver; leave BL_LED_K floating in that case. Contact Alp Lab for this variant.

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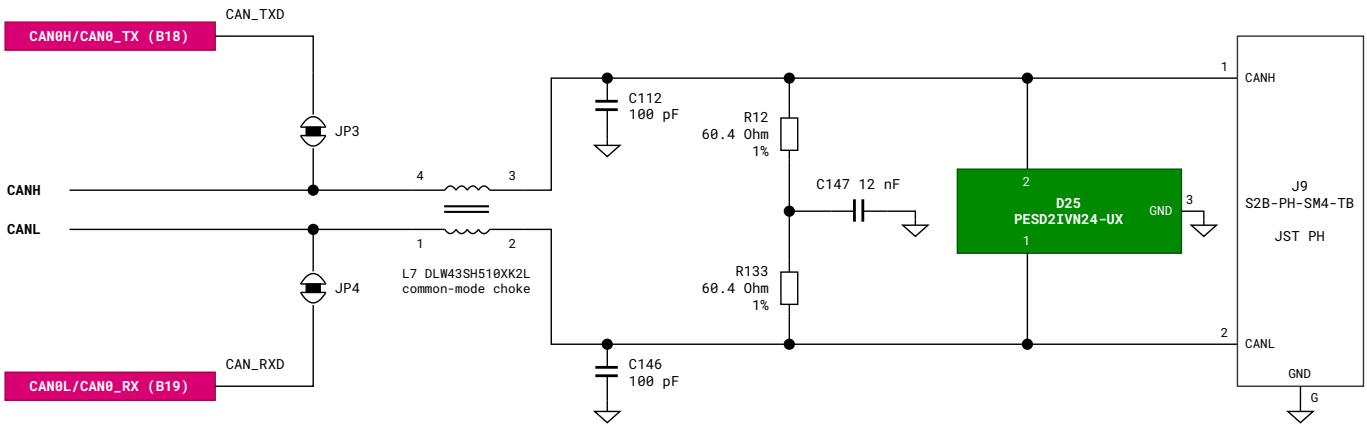
All DSI0 pairs: 100 Ohm ±10 % differential. Keep pairs short; minimise vias and avoid stubs. Match within each pair first, then across the pairs (clock to the data lanes). E1M development board TVS array: Semtech RCLAMP3552T.TNT.

Figure 15 MIPI DSI routing example

8.5 CAN-BUS

- Optional on-module CAN PHY (TI TCAN1044AVDRBRQ1), populated per assembly variant
- When the on-module PHY is fitted: B18 / B19 are CANH / CANL; only termination, ESD and EMI protection are needed on the carrier. Do not pull CAN_STBY (A19) low (low selects the PHY normal mode, several mA).
- When it is not fitted (standard build): B18 = CAN0_TX and B19 = CAN0_RX are 1.8 V SoC logic pins. Add a CAN transceiver on the carrier with its VIO on VIO_OUT (the E1M EVK uses a TI TCAN1044AVDRBRQ1). Never connect a CAN bus directly to B18 / B19 on such a module: bus voltages destroy the SoC pins. Check the assembly variant before you lay out the CAN path.

Add ESD protection and termination resistors. The E1M development board (whose module variant does not populate the on-module CAN PHY) carries its own **TI TCAN1044AVDRBRQ1** transceiver, protected by a **Nexperia PESD2IVN24-UX** TVS diode and a **Murata DLW43SH510XK2L** common-mode choke between the transceiver and the connector.



CANH / CANL: from the carrier CAN transceiver (E1M development board: TCAN1044AVDRBRQ1). JP3 / JP4 drawn as on the E1M development board schematic. Bridged, they tie B18 / B19 to CANH / CANL: only for a module whose CAN PHY is fitted. On a module without it (standard build), B18 / B19 are 1.8 V logic pins: keep JP3 / JP4 open, bus voltages destroy them.

Figure 16 CAN-BUS interface

Note The CAN-BUS transceiver is optional on E1M. If isolation desired, external transceiver must be used.

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8.6 USB 2.0

- One USB 2.0 interface, Full-Speed (12 Mbit/s) and High-Speed (480 Mbit/s)
- Host or device operation
- Brought out on the E1M standard USB0 pads (B1 / C1 / C2 / D2) on R3

Route USB0_30_D_P / USB0_30_D_N (B1/C1) as a **90 Ω differential** pair. Wire the role and power pins as follows:

Pin	Signal	Description
B1 / C1	USB0_30_D_P / USB0_30_D_N	90 Ω differential data pair.
D2	USB0_30_ID	Low: host mode. NC: device mode.
C2	USB0_VBUS	Connect to USB VBUS 5 V.

Table 14 USB 2.0 Connections

Note: On R3 the USB2 pads (I1 / J1 / I2 / J2) and the USB0 SuperSpeed lanes are not connected; leave them floating. R2 modules use the USB2 pads instead. A carrier that must take both revisions can route the connector to both pad groups through 0 Ω option resistors.

8.7 SD Card / eMMC

- One SDIO interface for an external µ SD card or eMMC
- On-module level translator with EMI filter and ESD protection (NXP NVT4858HKZ) on the SDIO lines
- Card power supplied from the module's SD_VDD (AH10) output, switched by firmware

Add only the card connector on the carrier; no additional series termination or ESD is required on SD_CLK, SD_CMD and SD_D0–SD_D3. Do not add carrier pull-ups on these lines. SD_DET (AG14) and SD_RST (AH12) are **not** on the level translator: they are 1.8 V SoC pads without on-module ESD protection. Wire the card-detect switch to GND, use the SoC internal pull-up or a pull-up to VIO_OUT only (never to SD_VDD or 3.3 V, which overdrive the pad), and add a low-capacitance ESD diode if the socket is user-accessible. SD_VDD has no current limit on the module (see Section 5).

8.8 Digital Communication

- UART, SPI, I^2C / I^3C
- Pin-mux configured in software
- I^2C/I^3C require carrier pull-ups to VIO_OUT (1.8 V)
- I^2C0 (AD2 / AE2) also carries the on-module identity EEPROM at 0x50 and 0x58: do not place carrier devices at these addresses (see below)
- SPI chip-selects handled on carrier board

E1M uses a dedicated pin out, the user needs to use the relevant functions in the application.

8.8.1 I^2C0 and the Identity EEPROM

The module carries a 128 Kbit identity EEPROM (onsemi N24S128C4DYT3G) on the I^2C0 pads: I2C0_SDA (AD2) and I2C0_SCL (AE2). It holds the module identity programmed in production (SKU, serial number and hardware revision). Follow these rules on the carrier:

- **Pull-ups.** The module has no pull-ups on I^2C0. Add them on the carrier, to VIO_OUT (1.8 V), for example 4.7 kΩ each. Never pull up to 3.3 V or to an always-on rail. Use a lower value (for example 2.2 kΩ) only if the bus capacitance requires it, and keep the pull-up current within the VIO_OUT budget (100 mA total).
- **Bus capacitance.** Keep the total bus capacitance (traces, connectors and all devices) within the I^2C limit of 400 pF for the speed mode you use. Keep the I^2C0 traces short.

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- **Address map.** The EEPROM uses 7-bit address 0x50 (memory array) and 0x58 (identity objects of the same part: Secure Data Page, 128-bit factory Unique ID, lock status and configuration register). Both respond. Carrier devices on I^2C0 must not use 0x50 or 0x58.
- **Module off.** The EEPROM is powered from the module 1.8 V rail, so it is only powered while `VIO_OUT` is high. A carrier device on I^2C0 that stays powered while the module is off must not hold SDA or SCL low or clamp them: use a device with Ioff-rated pins, or isolate the bus with a switch controlled by `VIO_OUT`.
- **Read-only.** The part has no write-protect pin. Treat the EEPROM as read-only: carrier firmware must not write to it unless Alp Lab documents a user area. Identity data is provisioned by Alp Lab in production, with the module powered on.
- **Never power it through W3.** Reserved pad W3 is the EEPROM supply net. Do not drive, load or jumper it, and never power the EEPROM through it: this back-feeds the whole 1.8 V domain and the unpowered SoC I^2C pads.

8.9 Audio and Sensor Interfaces

- I^2S and PDM
- Digital microphones and codecs
- Keep clocks clean and isolated

8.10 Analog Interfaces

- ADC: 8 channels, 12-bit, up to 5 Msps
- DAC: 2 channels, 12-bit, 1 kHz
- The ADC and DAC are referenced to the module 1.8 V rail; R3 modules have no separate precision reference (R2 modules had an optional 0.1 % 1.8 V reference)
- Keep analog routing short and isolated from digital/RF switching

8.11 PWM and Encoder Interfaces

- 8 × PWM outputs
- 4 × encoder inputs
- Suitable for motor and control use
- Software configuration required

9 Thermal Design

Operating temperature. E1M-AEN is rated − 40 °C to +75 °C ambient (Ensemble SoC limit). The carrier's RTC backup element sets the temperature range of the RTC backup (see Section 5.6). Self-heating reduces the usable ambient further; plan the carrier with the measures below.

The E1M-AEN dissipates heat primarily through the Ensemble SoC into the module PCB and, from there, into the carrier board. The SoC package thermal-resistance figures (θ_{JA} 21.1 °C/W still air, θ_{JC} 17.0 °C/W) are listed in the datasheet; the **realised** thermal performance depends heavily on how the carrier board pulls heat away. Maximum junction temperature is +105 °C operating (+150 °C absolute).

Carrier-board measures that improve thermal performance:

- **Copper area** — provide generous ground/power copper pours on inner and bottom layers beneath and around the module to spread heat (with a carrier cutout, outside the cutout).
- **Via stitching** — stitch the ground pads under the module to inner planes with a dense via array to conduct heat into the board.
- **Airflow** — even modest forced airflow significantly lowers θ_{JA} account for enclosure ventilation early.
- **Ground pads** — solder all 49 GND pads, each with at least one via to a solid GND plane, on a ≥ 4-layer carrier with ≥ 50 × 50 mm of connected GND copper (module-to-ambient ≈ 15 °C/W, estimated).
- **Derating** — derate the AI workload / clock and cap Wi-Fi transmit power and duty at high temperature to stay within $T_{J,max}$. Worst-case dissipation occurs during sustained NPU inference with Wi-Fi TX active. For planning on a 50 × 50 mm carrier in natural convection: with Wi-Fi TX at ≤ 30 % duty plan T_A ≤ 60 °C; with continuous 18 dBm TX plan T_A ≤ 40 °C, or forced air ≥ 1 m/s (estimated). Limit the backlight LED power to ≤ 0.8 W.

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> **Tip:** For sustained full-clock AI workloads in still air, validate junction temperature against your enclosure early — copper area and via stitching under the module are the cheapest and most effective levers.

10 Software Support

10.1 Alp SDK™

- Open-source, CMSIS-compliant
- Unified HAL across E1M variants
- Vendor-agnostic software architecture

10.2 AI Acceleration

- Integrated Arm Ethos-U55 NPUs, plus an Ethos-U85 on E4 / E6 / E8
- Scales with Ensemble variant
- Optimized for low-power edge AI

11 Bring-Up Checklist

11.1 Pre-Power Checks

- Confirm correct SoM variant
- Verify orientation and solder joints
- Ensure only 5 V is connected
- Check ground continuity
- Confirm Ethernet magnetics populated (if used)
- Inspect MIPI routing

11.2 First Power-On

- Follow Power Bring-up on a New Carrier in Section 5
- Monitor current consumption (current-limited supply first)
- Check for abnormal heating
- Confirm `VIO_OUT` and `PORn` high within 290 ms

11.3 Basic Validation

- UART boot/debug output
- Ethernet link up
- GPIO or PWM toggle
- Peripheral enumeration via SDK

11.4 Common Issues

- Missing Ethernet magnetics
- Wrong firmware image
- Poor MIPI routing
- Supplying unintended rails
- Leaky TVS, or a pull-up to a switched rail, on `MODULE_EN` / `MODULE_STBY`; an unpowered host pin on `MODULE_EN`
- `+S_CAP` left floating, or the RTC trickle charger enabled with a primary lithium cell

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- Bulk capacitance on VIO_OUT, or a capacitor on PORn
- Carrier pull-ups or drivers on Wi-Fi module pads while Wi-Fi is off

12 Design Checklist (Summary)

Item	Status
5 V supply 4.75–5.25 V, ≤ 5.5 V with transients; over-voltage protection (TVS ahead of an eFuse with OVP); inrush limited; ramp ≤ 40 ms	OK
Source ≥ 1.0 A continuous / 1.5 A peak; hold-up ≥ 50 µF effective per A at VDDIN	OK
MODULE_EN / MODULE_STBY open drain or push-pull 1.8–5 V, ≤ 0.1 µA leakage, no carrier pull-up; N-MOSFET buffer if the host can be unpowered while the module stays up	OK
+S_CAP (AG15): coin cell (trickle charger off), supercapacitor (charger on) or tied to GND; leakage ≤ 10 nA; never floating	OK
PORn open drain, no pull-up, no capacitor (R2 modules: see errata E-02); RTC_WAKE_N pulled up to an always-on rail if used	OK
VIO_OUT output only, ≤ 100 mA, ≤ 2.5 µF; level shifters referenced to VIO_OUT	OK
No pad driven while VIO_OUT is low; no pull-ups on Wi-Fi module pads	OK
Reserved pads (W3, U3 / V3, S3, Q3 / R3 / T3) left open; other RSVD pads floating	OK
I^2C0 (AD2 / AE2): pull-ups to VIO_OUT, no carrier device at 0x50 / 0x58, no device holding the bus while the module is off, EEPROM not written	OK
All GND pads tied to a low-impedance plane	OK
Output-rail current budget within limits (VIO_OUT / +V_CAM / SD_VDD)	OK
4-layer+ stack-up with continuous ground reference	OK
Controlled impedance: 100 Ω MIPI/Ethernet, 90 Ω USB, 50 Ω RF	OK
Ethernet magnetics + RJ45 populated	OK
RF-clean antenna routing + certified antenna	OK
JTAG/SWD debug header exposed (1V8 level)	OK
Mounting option (spacer PCB or carrier cutout), land pattern, 2.0 mm courtyard and keep-out observed	OK
Thermal: copper area + via stitching under module	OK
Correct firmware per variant	OK

Table 15 Design checklist

13 Ordering Information

E1M-AEN modules are ordered based on:

- Ensemble SoC variant
- Memory configuration
- Assembly options

Refer to the official ordering table for valid MPNs.

14 References & Related Documents

Ref.	Title	Source
[1]	E1M-AEN Datasheet (DS-AEN-001)	Alp Lab
[2]	E1M™ Specification	github.com/alplabai/e1m-spec

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Ref.	Title	Source
[3]	Alif Semiconductor Ensemble Series Datasheet	Alif Semiconductor
[4]	Alif Semiconductor Ensemble Series Reference Manual	Alif Semiconductor
[5]	BDE-BW3501 Wi-Fi 6 / BLE Module Datasheet	BDE Technology
[6]	Alp SDK™ Repository	github.com/alplabai/alp-sdk
[7]	Alp SDK™ Documentation	docs.alplab.ai

Table 16 Related Documents

15 Notices

- Specifications subject to change without notice
- Some features may be preliminary
- Always verify against the latest datasheet

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