ALP LAB

E1M Development Board

User Guide

Document Number: UG-E1M-001 **Revision:** 0.9 **Date:** November 2026 **Status:** Preliminary

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Release History

Revision	Changes	Date
0.1	• Initial draft	April - 2026
0.2	• Documented the 2626-R2 assembly variant: not-populated components for the E1M-AEN (Alif) build (M.2 Key E/M connectors and PCIe AC-coupling, microSD ESD diodes, secondary debug J3, antenna feed, option jumpers). • Added Appendix B and inline notes.	June - 2026
0.3	• E1M-AEN R3 module alignment: ▸ +S_CAP (AG15) is now the RTC backup input on R3 modules and the carrier provides the backup store ▸ the 2641-R3 EVK fits a 47 mF supercapacitor C38 on +S_CAP via P16, charged by the module (backup options, trickle-charger rule and primary-cell safety warning added) ▸ MODULE_EN / MODULE_STBY pad levels and drive options added ▸ the RK055HDMIPI4MA0 panel is identified without the dead vendor link.	October - 2026
0.4	• Hardware sections rewritten to the 2641-R3 netlist (E1M-AEN build). • Power: input eFuses, power tree, and +VIO_SW generated from VIO_OUT. • Current measurement: six INA236 and two INA228 monitors. • RP2040 debug probe and GPIO map: module enable, standby and reset control, RTC_WAKE_N. • Each jumper, switch, button and multiplexer described in its own subsection, with positions, control line, default and recommended setting. • I2C bus map, four PDM microphones, on-board speakers, camera and display connectors. • Antenna: the two antenna options, the rework steps for J1, and the unconnected 5 GHz and 6 GHz pads. • Block diagram redrawn for the 2641-R3 carrier (module-independent). • New simplified schematics drawn from the netlist: power tree and inputs, current auto-ranging, power-good LEDs, RTC backup, module control, debug and console routing, I2C, USB and USB-A host, SDIO / I2S muxes, microSD, antenna, Ethernet, CAN, camera, display, audio, Arduino / mikroBUS, DAC, encoder and UART headers, user LEDs, and every jumper and switch. Transistors and passives are drawn as schematic symbols. Placeholders mark the figures still to come from the 2641-R3 CAD. • Connector pinouts for J4 and J7; Ethernet link-LED table; cautions for P1 / P9 double shunts, P2 with pad D2 driven high, and current-range switching on the module supply. • E1M-AEN notes: ETH0 only (one 100 Mbit PHY) and two DSI lanes. • Module mounting: the module sits on a spacer PCB on the EVK (E1M-STD 1.5 section 5.2, option (a)). • +S_CAP floats with P16 open (R223 not fitted); mux control lines rely on weak internal pull-downs; J2 pin 7 is the key; CAM_EN_# polarity; caution for modules with an on-module CAN PHY. • Datasheet-checked values: TAS2563 addresses 0x4D / 0x4E, the USB-PD requirement (3 A at 9 V to 20 V, 27 W or more), eFuse thresholds and fault flag, mux and transceiver	October - 2026

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Revision	Changes	Date
	defaults, monitor addresses and the LSF I/O-level rule (new cautions for P1 / P9 with a 3.3 V module, CAN termination faults and the SDA hold time). • Sizing formulas for the external RTC charger (R126, D11) for a rechargeable cell or a large supercapacitor. • Figures redrawn in one style: block diagram with the schematic symbols of the other figures; ESD diodes drawn as TVS symbols on each line (Ethernet, CAN, USB-A, microSD), the same TVS symbol for D46 and D7 on the power inputs, and the CAN choke L7 as a common-mode choke symbol; the current-range comparator U36 (TLV7021) drawn as a triangle symbol, like the OPA189 DAC buffers U23 and U24, with the designator and part number beside each symbol; the barrel-jack board render removed (the barrel input schematic covers it). • Removed the sensor, 74LVC157 and M.2 content. Appendix B replaced with the 2641-R3 not-populated list.	
0.5	• Document status: the title page now reads Preliminary, matching the running header (it read Draft).	October - 2026
0.6	• RP2040 boot line named RP_USB_BOOT_n (active low) in the JP7 text, caption and figure (it was printed with a stray backslash and without the _n suffix). • RP2040 Debug Probe: states that the RP2040 is the EVK's USB-to-UART console bridge on J5 (with S7 on the RP2040 side); only a separate bridge chip is absent.	October - 2026
0.7	• Release history: every entry formatted as a bullet list.	October - 2026
0.8	• Table of Contents: each entry links to its section; the front-matter lists are set tighter.	October - 2026
0.9	• Product name on page 1 links to the product page on alplab.ai.	November - 2026

Table 1 Release History

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1 Purpose and Scope

The *E1M Development Board (EVK)* accelerates evaluation and development on the E1M System-on-Module (SoM) platform by providing a carrier board with common peripherals: USB, Ethernet, CAN, display and camera, audio, expansion headers, an on-board RP2040 debug probe, and on-board current measurement. This guide describes what each interface is, how it is wired on the EVK, and how to use it safely during bring-up.

> **Warning:** This guide describes the **E1M-EVK 2641-R3** carrier as assembled for the **E1M-AEN** module (the "Alif" build). On this board the RP2040 can switch `MODULE_EN`, `MODULE_STBY` and `PORn` of the module (see Module Control Pins). Fitting a jumper on P11 or P12 holds the module off or in standby. Some footprints (M.2, IO expander, speaker connectors, secondary debug headers) are not fitted on this build; see Appendix B.

The EVK aligns with the E1M platform's unified-pinout approach across module variants described in the internal E1M Standard.

2 Safety, Handling, and ESD

> **Warning:** Handle the EVK and any attached camera or display modules under proper ESD controls: grounded wrist strap and ESD mat. Do not hot-plug peripherals unless the interface is explicitly designed for it. USB is generally OK; display and camera connectors are not.

1. **ESD precautions:** grounded wrist strap and ESD mat for every handle.
2. **Power precautions:** no hot-plug on display or camera connectors.
3. **Avoid shorts:** many signals are routed to exposed headers; an accidental short can damage the SoM or the peripheral.
4. **Input voltage:** the barrel jack input is specified for 7 V to 15 V. The input eFuse divider is set so that the eFuse only turns on at a higher voltage (see Power Inputs); use a supply of 9 V or higher.
5. **Rail domains:** the board uses `+5V`, `+3V3`, `+1V8`, and `+VIO_SW` (1.8 V with an E1M-AEN module). Several level shifters connect the module and expansion headers to these rails.
6. **Level-select headers:** set P1 (display I/O level) and P9 (Arduino and mikroBUS I/O level) before you attach a display, shield or click board. Do not leave these at an unknown position.

3 Functional Overview

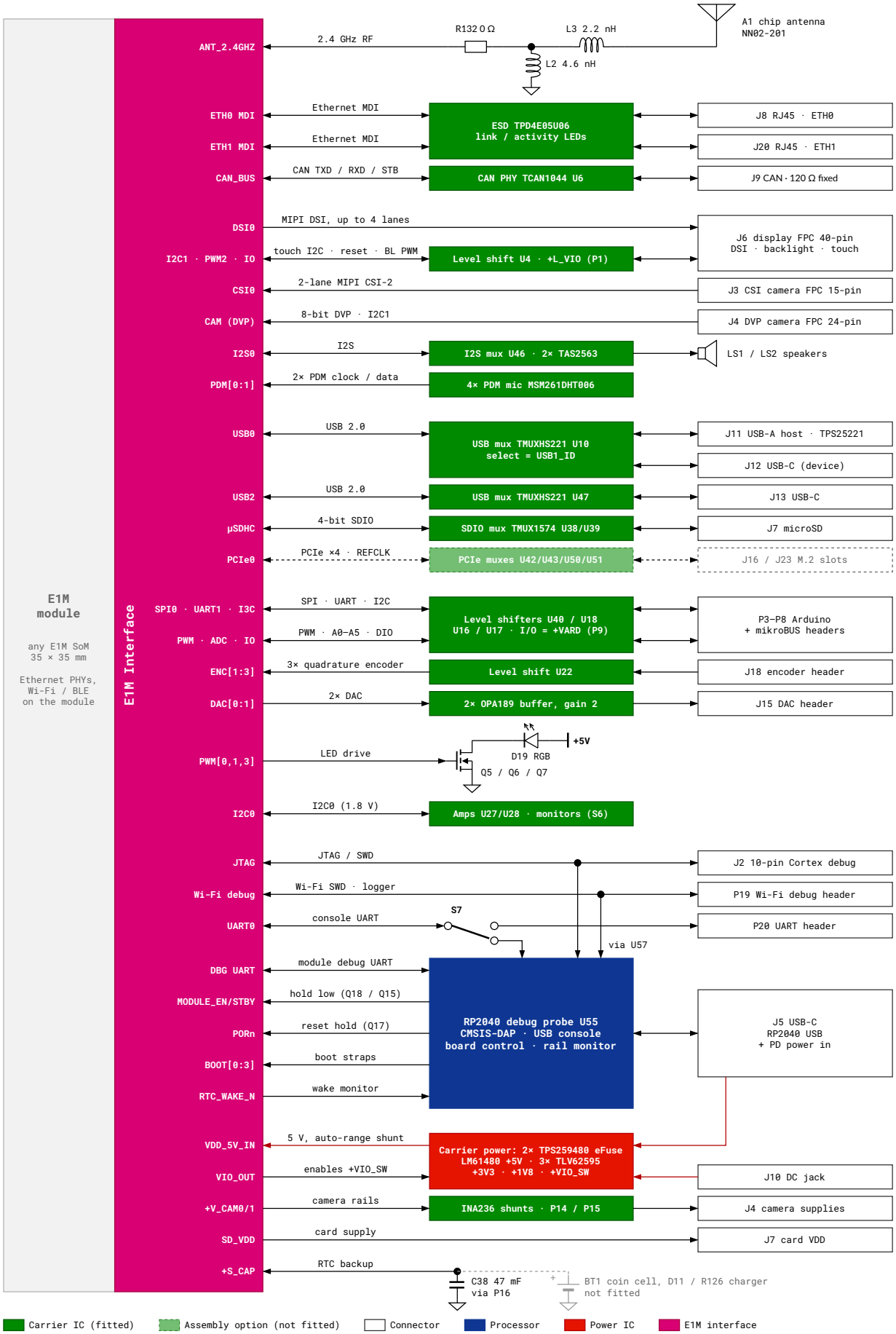
The EVK includes the following blocks:

- **Power input and tree:** barrel jack `J10`, USB-C power-delivery input `J5`, two input eFuses, a 5 V buck, `+3V3`, `+1V8` and `+VIO_SW` bucks, power-good LEDs on each rail.
- **Current measurement:** six `INA236` and two `INA228` I2C monitors.
- **Debug probe:** on-board RP2040 (`U55`) with USB on J5, module enable, standby and reset control, and a JTAG/SWD path to J2.
- **Compute module interface:** E1M 35 by 35 module footprint with USB, Ethernet, SDIO/SD, CAN, MIPI DSI/CSI, I2S, PDM, UART, ADC/DAC, GPIO, boot pins, JTAG/SWD. The module is mounted on a spacer PCB that sits on the EVK carrier (mounting option (a) of E1M-STD 1.5 section 5.2); it is not placed directly on the carrier.
- **Networking:** two RJ45 MagJacks J8 (`ETH0`) and `J20` (`ETH1`). E1M-AEN has one 100 Mbit PHY on `ETH0`, so only J8 is live; `J20` is unused.
- **CAN bus:** `TCAN1044AV` transceiver `U6` and a 2-pin connector J9.
- **USB:** USB-C J12 and J13, USB-A host J11, two `TMUXHS221` data muxes (`U10`, `U47`).
- **Storage:** microSD socket J7 with `TMUX1574` SDIO muxes (`U38`, `U39`).
- **Display:** 40-pin MIPI DSI connector J6 for the `RK055HDMIPI4MA0` 720p panel.
- **Camera:** 15-pin MIPI CSI connector J3 and 24-pin parallel (DVP) connector J4; camera rails `+1V2_CAM` / `+2V6_CAM`.
- **Audio:** two `TAS2563` Class-D amplifiers (`U27`, `U28`) driving two on-board speakers, four `MSM261DHT006` PDM microphones, an I2S source mux (`U46`).

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- **Expansion:** Arduino and mikroBUS headers behind level shifters, DAC output header J15, encoder header J18, UART header P20.
- **User interface:** RGB LED, status LEDs and the reset and boot buttons.
- **M.2:** the M.2 connectors and PCIe path are **not fitted** in the E1M-AEN build.

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Carrier I/O rail +VIO_SW follows module VIO_OUT (1.8 V or 3.3 V). Monitors: 6× INA236 + 2× INA228 on I2C0 or the RP2040 bus (S6).
Interfaces that a module does not implement stay unused (E1M-AEN: ETH0 only, two DSI lanes). J5 carries both the RP2040 USB and USB-C PD power.
RTC backup: C38 47 mF on +S_CAP via P16, charged by the module. BT1 coin cell and the D11 / R126 charger are unfitted options; fit exactly one store.

Figure 1 E1M-EVK 2641-R3 block diagram. The carrier accepts any E1M module; interfaces a module does not implement stay unused.

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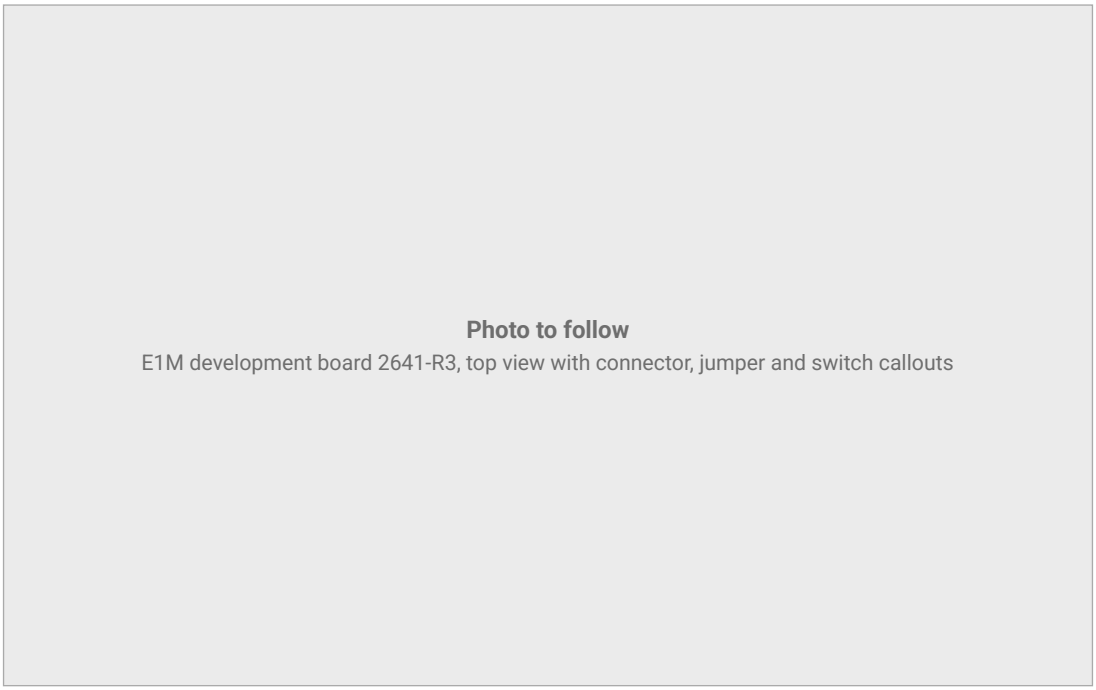


Figure 2 E1M development board 2641-R3, top view with connector, jumper and switch callouts

4 Power System

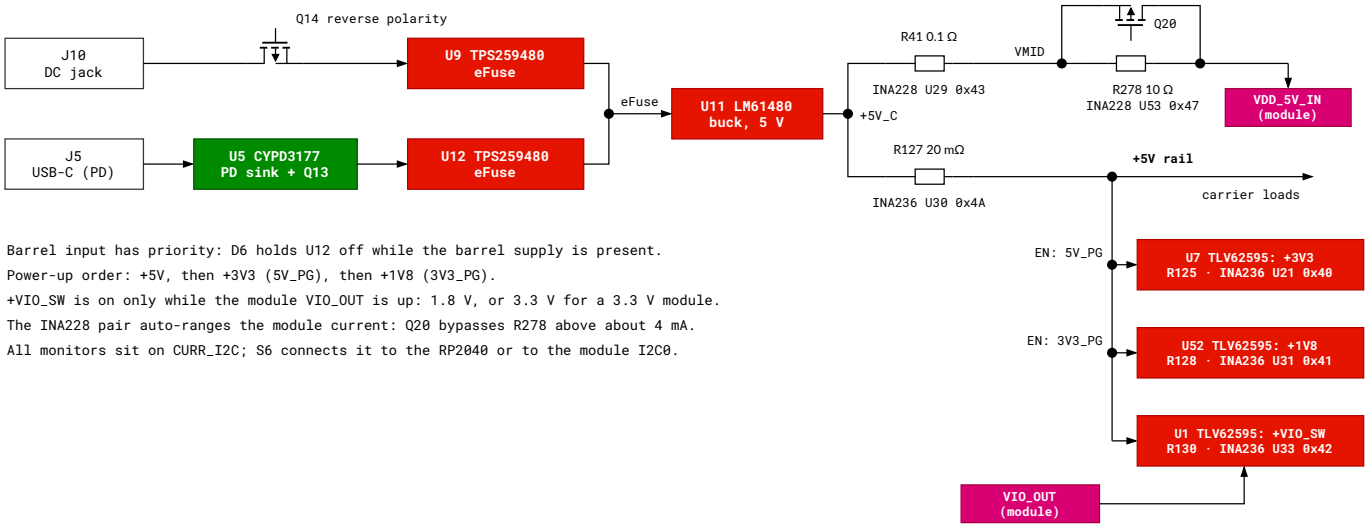


Figure 3 Power tree: inputs, eFuses, regulators and current monitors (simplified from the 2641-R3 netlist)

4.1 Power Inputs

The EVK has two power inputs. Both feed a shared net eFuse through their own input eFuse.

4.1.1 Barrel Jack

J10 is a DC jack (5 A, 24 V rated connector). Pin 1 is +V_BRL and pin 2 is 0V. The P-channel pair Q14 (DMP3036SSD-13, both halves in parallel) protects against reverse polarity. Its drains are on +V_BRL and its sources on BRL_IN. R240 (100 kΩ) pulls its gates to 0V, so Q14 conducts only when the polarity is correct. Zener D56 (SZ1SMA5925BT3G, 10 V) between the gates and BRL_IN limits the gate-source voltage to about 10 V, inside the 25 V rating of Q14. TVS D46 (TVS2200DRVR) and C198 (1 µF) sit on BRL_IN. eFuse U9 (TPS259480A) switches BRL_IN onto eFuse, which feeds the buck U11.

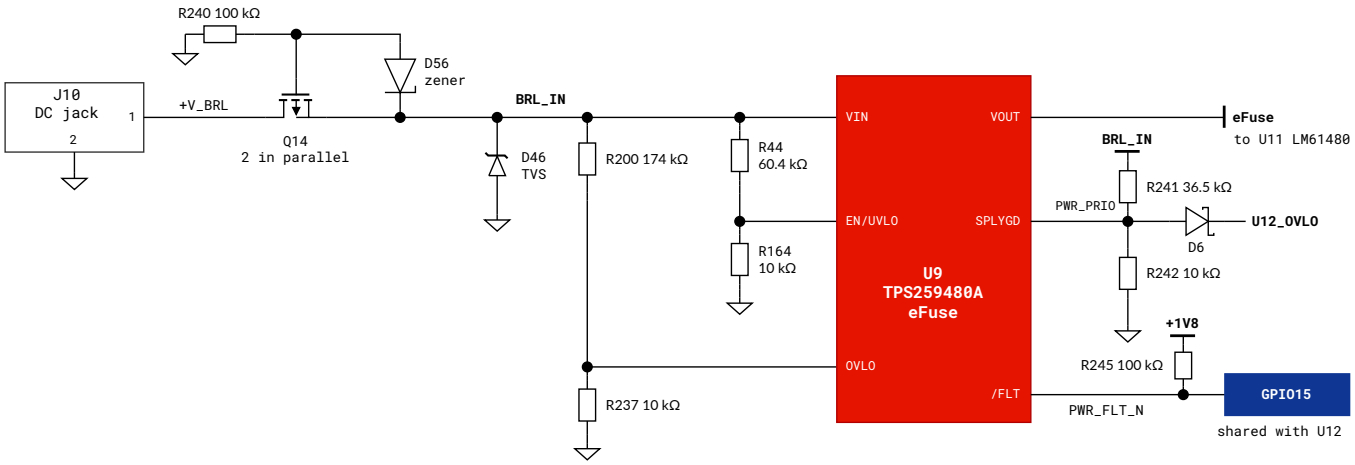


Figure 4 Barrel input: Q14 reverse-polarity FET, D46 TVS, eFuse U9 with its UVLO and OVLO dividers, and the PWR_PRIO priority link to U12 (simplified)

The schematic labels the barrel input 7 V to 15 V. From the dividers R44/R164 (EN/UVLO) and R200/R237 (OVLO), U9 turns on at about 8.5 V and cuts off above about 22 V. These values are calculated from the 1.2 V threshold of the TPS25948x family, not measured. A supply between 7 V and 8.5 V does not start the board through J10. Use 9 V to 15 V.

4.1.2 USB-C Power Delivery (J5)

J5 is a USB-C connector with a CYPD3177 USB-PD sink controller (U5) on CC1/CC2. Strap resistors set the contract it requests: VBUS_MIN (R46 5.1 kΩ up, R47 1 kΩ down), VBUS_MAX (R48 0 Ω up), ISNK_COARSE (R92 / R104 5.1 kΩ) and ISNK_FINE (R137 0 Ω down). The straps are referenced to UPD_3V3, the U5 VDDD pin. U5 switches USBPD_VBUS through Q13, a back-to-back P-channel pair. Its gates are pulled up to USBPD_VBUS by R45 (10 kΩ) and driven by U5 VBUS_FET_EN through R140 (1 kΩ). The switched node USBPD_V feeds eFuse U12 (TPS259480A), which feeds the same eFuse net. TVS D7 (TVS2200DRVR) clamps USBPD_VBUS. The straps request a contract between 9 V (VBUS_MIN) and 20 V (VBUS_MAX) at 3 A (ISNK_COARSE 3 A + ISNK_FINE 0 A). If the source offers no voltage in that range with at least 3 A, U5 keeps Q13 off and J5 does not power the board. This covers every 5 V-only source and PD chargers that offer less than 3 A at 9 V or higher (for example 9 V/2 A or 9 V/2.22 A). Use a charger that offers 3 A at 9 V, 12 V, 15 V or 20 V (27 W or more). Separately, from R165/R199, U12 turns on only at about 7.2 V (calculated).

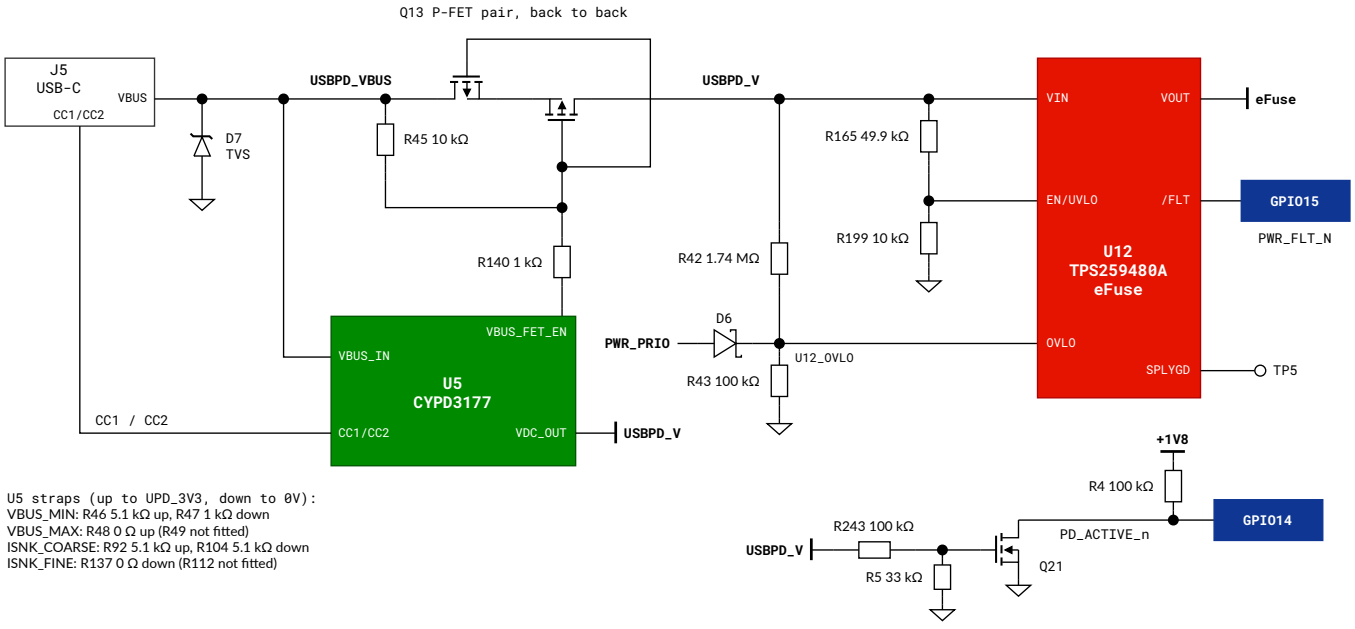


Figure 5 USB-C PD input: sink U5, pass FETs Q13, eFuse U12 and the PD_ACTIVE_n flag (simplified)

U5 SAFE_PWR_EN (the 5 V fallback gate drive) is not connected, so a source that cannot meet the request gives no power. U5 FAULT (high on a mismatch, or when USBPD_VBUS is more than 20 % below 9 V or above 20 V) has only R141 (100 kΩ) to 0 V and is not read by software. PD_ACTIVE_n is the only PD status the RP2040 sees.

J5 also carries the USB connection of the on-board RP2040 (see Debug Probe). PD_ACTIVE_n is the drain of Q21 (BSS138PW), whose gate sees USBPD_V through the divider R243 (100 kΩ) / R5 (33 kΩ). It is read by RP2040 GPIO14 (pull-up R4 100 kΩ to +1V8). With a 9 V or higher contract the gate sees about 2.2 V or more and PD_ACTIVE_n is reliably low. With a 5 V-only source, or any source that cannot meet the request, U5 leaves Q13 off, USBPD_V stays near 0 V and PD_ACTIVE_n reads high. The /FLT outputs of U9 and U12 are wired together as PWR_FLT_N (open drain, R245 100 kΩ to +1V8) and read by RP2040 GPIO15. Low means overtemperature, a persistent overcurrent (longer than the ITIMER blanking time, about 5 ms with 6.8 nF) or a shorted ILM pin in either eFuse. Input undervoltage or overvoltage, and the priority hold-off of U12, do not pull it low. The TPS259480A retries about 103 ms after a fault, so the flag can pulse.

J12 and J13 are USB 2.0 data ports; they are **not** power inputs (see USB Subsystem).

> **Tip:** Use one primary power source at a time during early bring-up (barrel or J5). When both are connected the barrel input takes priority. While U9 reports a good input on SPLYGD, the divider R241/R242 (PWR_PRIO) drives the U12 OVLO pin high through D6 and holds the USB-PD eFuse off.

4.2 Main 5 V Generation

- Both eFuses feed eFuse, which feeds a LM61480 buck regulator (U11) that generates +5V_C.
- +5V_C is split into two branches. The carrier branch passes through the 20 mΩ shunt R127 to give the +5V carrier rail. The module branch passes through the 0.1 Ω shunt R41 and a 10 Ω resistor R278 (bypassed by Q20) to give VDD_5V_IN, which supplies the module on pads R1, R2, S1, S2.
- The two branches meet only at +5V_C. Each branch is measured by its own current monitors (see Current Measurement).
- The USB-A host port is powered from +5V through switch U8 (TPS25221).

> **Warning:** VDD_5V_IN has only about 0.1 µF of local capacitance. Do not add long unfiltered leads between the board and the module supply.

4.3 Secondary Rails

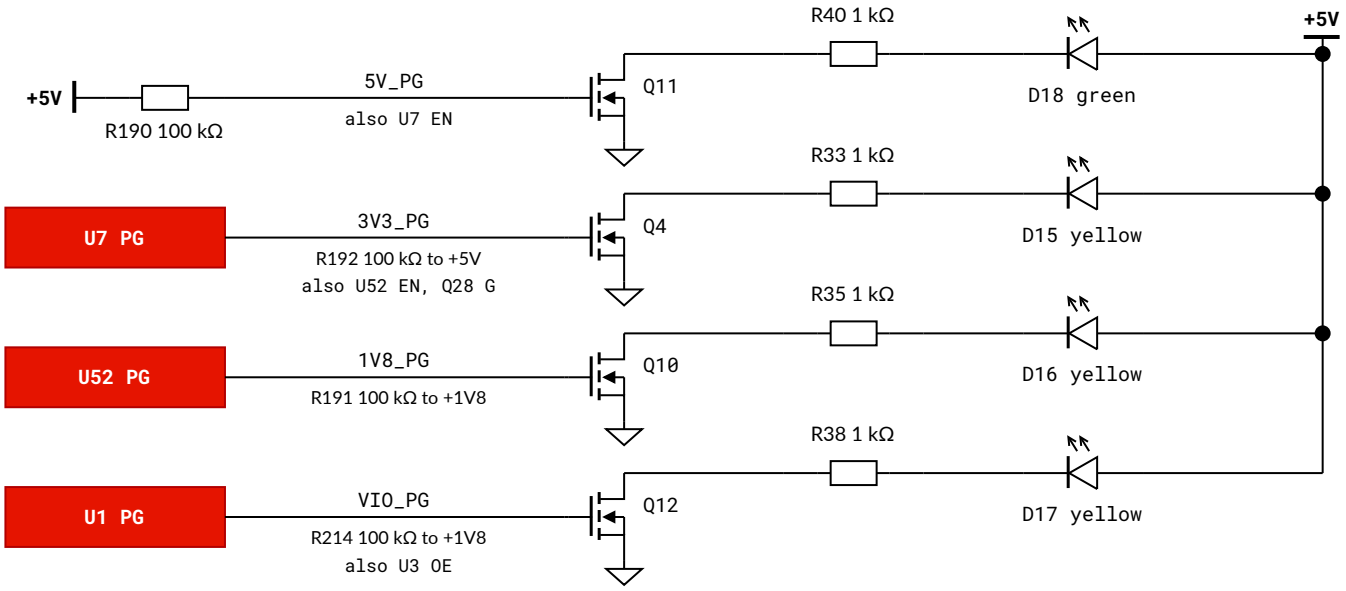
All three secondary rails are TLV62595 buck regulators from +5V. They start in sequence: +5V, then +3V3, then +1V8.

Regulator	Output	Notes	Power-good LED
U7	+3V3	Enabled by 5V_PG. Rail current shunt R125.	D15 (yellow)
U52	+1V8	Enabled by 3V3_PG. Rail current shunt R128.	D16 (yellow)
U1	+VIO_SW	Carrier I/O rail, enabled by the module VIO_OUT. Rail current shunt R130.	D17 (yellow)

Table 2 Secondary rails

D18 (green) shows 5V_PG. 5V_PG is +5V through R190 (100 kΩ), not a regulator power-good output, so D18 lights whenever +5V is present. The RESET (power-good) output of U11 is only pulled up (R25 100 kΩ to +5V_C) and is not used. Each LED is switched by a low-side N-FET and sinks from +5V through 1 kΩ. The power-good lines also sequence the rails: 5V_PG enables U7, 3V3_PG enables U52 and drives the Q28 gate, and VIO_PG drives the U3 OE pin.

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Each LED is on while its power-good line is high. 5V_PG is +5V through R190, so D18 shows that +5V is present. U7, U52 and U1 drive 3V3_PG, 1V8_PG and VIO_PG from their PG outputs. The same lines sequence the rails: 5V_PG enables U7, 3V3_PG enables U52, VIO_PG enables U3 (OE).

Figure 6 Power-good LEDs D18, D15, D16, D17 and their drivers (simplified)

4.4 Carrier I/O rail +VIO_SW and VIO_OUT

+VIO_SW is the carrier's I/O rail (1.8 V with an E1M-AEN module). It is **not** connected to the module VIO_OUT pads (P1, P2). Buck U1 generates it from +5V, and the module VIO_OUT only **enables** U1 through R284. VIO_OUT carries a very small load (about 18 µA and 0.1 µF). The RP2040 reads VIO_OUT through a divider on GPIO29 (ADC3 sees VIO_OUT / 2).

Consequently +VIO_SW is off whenever the module's VIO_OUT is off. Comparator U13 (TLV7031) raises U1 to about 3.3 V (calculated) if a module presents VIO_OUT above about 2.5 V; with an E1M-AEN module (1.8 V VIO_OUT) +VIO_SW stays at 1.8 V.

4.5 SuperCap Rail and RTC Backup (+S_CAP)

The E1M interface pin +S_CAP (pad AG15) is the net +SCAP on the carrier. It is available on the 3-pin header P16 and the 2-pin header P21.

What the module does with +S_CAP. On the **E1M-AEN R3** module, the +S_CAP pad (AG15) is connected to the module's RTC backup input. The standard R3 module has no backup supercapacitor of its own, so the carrier provides the RTC backup store, or none. Choose one:

- **Coin cell.** A BR-type primary lithium cell rated −40 to +85 °C keeps time for years without 5 V. Firmware must keep the RTC trickle charger **disabled**.
- **Supercapacitor** (room-temperature products). Firmware enables the RTC trickle charger; the module charges the capacitor from its 3.3 V always-on rail through 15 kΩ, to about 3.0– 3.25 V. No charging circuit or other source is needed on the carrier: fit only the capacitor. Choose a part rated for at least 3.3 V.
- **None.** Tie +S_CAP to GND (do not leave it floating). Time is lost when 5 V is removed.

Keep the total leakage on +S_CAP (ESD diode, holder) at 10 nA or less. The backup type must be configured in your firmware to match what is fitted. The temperature range of the RTC backup is set by the backup element you choose, not by the module.

> **Warning:** **Never enable the RTC trickle charger while a primary lithium cell is fitted.** The cell can leak, vent or burst. Enable it only when the element on +S_CAP is a supercapacitor.

E1M-AEN R2 modules keep the RTC backup supercapacitor on the module and do not connect the +S_CAP pad.

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On the EVK. The **2641-R3** carrier fits a 47 mF supercapacitor, C38 (rated ≥ 3.3 V), as the RTC backup store for an R3 module, connected to +S_CAP through jumper P16. The module charges it: no other source is needed. With P16 closed on pins 1-2 the backup type is a supercapacitor, so firmware must enable the RTC trickle charger (15 kΩ). With P16 open, +S_CAP floats, because the 0 Ω tie to 0 V (R223) is not fitted; avoid this, or fit R223 when no store is wanted. The carrier also has three unfitted options. Fit exactly one backup store:

Option	Parts and jumpers	State
Supercapacitor	C38 47 mF, ≥ 3.3 V, through P16 pins 1-2	Fitted
Coin cell	Holder BT1 (S8411-45R) through P16 pins 2-3	Not fitted
External charger	R126 1 kΩ and D11 (BAS116GWX), connected to +S_CAP by P21	Not fitted
None	R223 0 Ω ties +S_CAP to 0 V	Not fitted

Table 3 +S_CAP backup options on the 2641-R3

The module charges C38 itself (trickle charger on, 15 kΩ).
`Fit exactly one store; keep P21 open.`

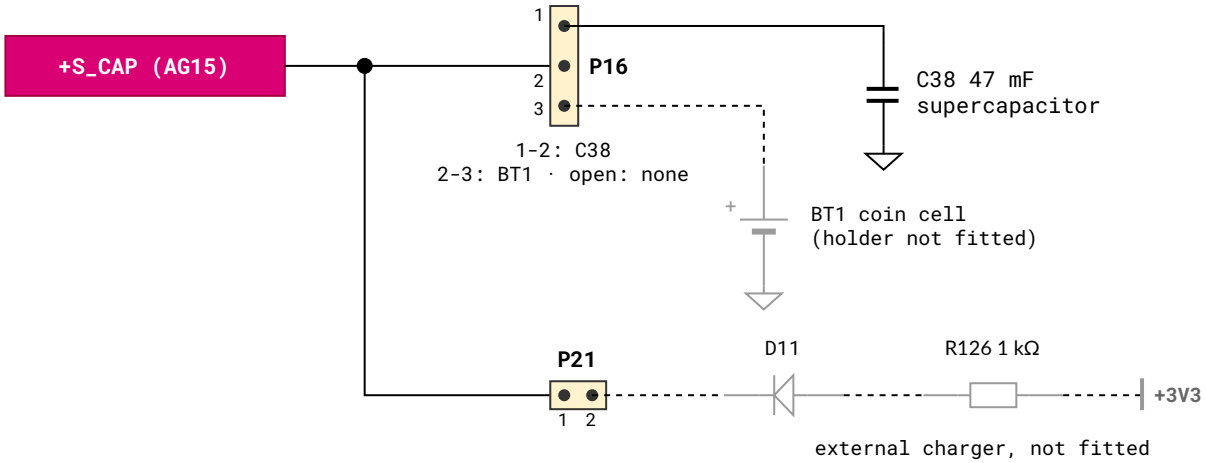


Figure 7 +S_CAP RTC backup: store select P16 and charger link P21 (simplified)

The EVK backup is a supercapacitor, so it is meant for room-temperature evaluation; a product that needs RTC backup over − 40 °C to +85 °C uses a coin cell instead (see above).

Warning: If you fit a primary (non-rechargeable) coin cell in BT1, do not fit the charger parts (R126, D11) and do not close P21, and keep the module RTC trickle charger disabled. A primary lithium cell that is charged can leak, vent or burst. Do not fit the coin cell and C38 as backup stores at the same time.

Note: Charge and hold time of C38. Through 15 kΩ the time constant is about 12 minutes: an empty C38 reaches the RTC's 2.0 V switchover level in about 13 minutes and charges to about 3.05 V. Fully charged, it keeps the RTC running for about 4.6 days at 25 °C (3.7 days worst case) after 5 V is removed; the clock stops when C38 falls below about 2.0 V. Leave a new EVK powered for at least 15 minutes, with firmware that enables the trickle charger, before you test timekeeping without 5 V. Hold time is much shorter at high temperature.

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4.5.1 Sizing the external charger (R126, D11)

A customer who fits a **rechargeable** coin cell in BT1 (12 mm holder), or a supercapacitor larger than about 100 mF, charges it from the carrier instead of from the module. The charge path is +3V3 through R126 and diode D11 (anode on R126), then P21 to +S_CAP, then P16 to the store. Both parts are not fitted in this assembly; their footprints are on the board.

The charge current with the store at voltage V_{store} is

$$I_{\text{chg}} = \frac{V_{3\text{V3}} - V_F - V_{\text{store}}}{R_{126}}$$

where $V_{3\text{V3}}$ is the carrier +3V3 rail (3.32 V from the U7 divider) and V_F is the forward voltage of D11 at that current, from the D11 datasheet. The current is highest when the store is empty. To keep it within the cell's maximum charge current I_{max} (from the cell datasheet), choose

$$R_{126} \geq \frac{V_{3\text{V3}} - V_F - V_{\text{store,min}}}{I_{\text{max}}}$$

The store charges towards the float voltage

$$V_{\text{float}} \approx V_{3\text{V3}} - V_F$$

with V_F taken at the cell's self-discharge current, which is close to 0 V across R126. Check three limits:

- V_{float} must not exceed the cell's maximum charge voltage. A cell rated for less needs a lower supply or a different diode.
- V_{float} must stay below 5.5 V, the absolute maximum on +S_CAP, and above about 2.2 V so that the RTC runs from the store.
- The power in R126 is at most $I_{\text{chg}}^2 R_{126}$ with the store empty; the fitted footprint is a 0603 (0.1 W) part.

For a supercapacitor C the charge follows $V(t) = V_{\text{float}}\left(1 - e^{-t/(R_{126}C)}\right)$: it reaches about 95 % of V_{float} after $3R_{126}C$.

Example (assumed values; take the real ones from the datasheets). With $V_F = 0.6$ V, a cell that may be charged at up to 0.5 mA and an empty store at 2.0 V: $R_{126} \geq (3.32 - 0.6 - 2.0)\ \text{V}\ /0.5\ \text{mA} = 1.44\ \text{k}\Omega$, so fit 1.5 kΩ. The cell then floats at about 2.7 V; confirm this against the cell's charge voltage.

To use the external charger: fit R126 and D11, set P16 to the store (2-3 for BT1), close P21, and keep the module RTC trickle charger disabled so that the two chargers do not work against each other.

> **Warning:** Treat the supercap rail as an energy storage node. After power-down it may remain charged. Confirm discharge behavior before handling or probing.

5 Current Measurement (Power Profiling)

> **Note:** U33 (0x42) and U30 (0x4A) have their A0 pin strapped to SDA. TI requires at least 100 ns of SDA hold time after SCL falls for these addresses: configure the RP2040 or module I2C master accordingly, or these two monitors can mis-decode their address.

The EVK has eight I2C power monitors on the bus CURR_I2C. Six are INA236 (variants INA236A and INA236B) and two are INA228. All are powered from +5V.

Ref	Part	I2C address	Rail measured and shunt	Alert
U21	INA236A	0x40	+3V3, R125 20 mΩ	none
U31	INA236A	0x41	+1V8, R128 20 mΩ	none
U33	INA236A	0x42	+VIO_SW, R130 50 mΩ	none
U29	INA228	0x43	Module 5 V supply, high range: R41 0.1 Ω	5V_CURR_ALERT
U53	INA228	0x47	Module 5 V supply, low range: R278 10 Ω (valid only while Q20 is off)	5V_CURR_ALERT

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Ref	Part	I2C address	Rail measured and shunt	Alert
U34	INA236B	0x49	+V_CAM1 (+2V6_CAM), R131 50 mΩ	none
U30	INA236B	0x4A	+5V carrier rail (all loads except the module), R127 20 mΩ	none
U32	INA236B	0x4B	+V_CAM0 (+1V2_CAM), R129 50 mΩ	none

Table 4 Current monitors

- Max-current relation for the INA236 monitors (ADCRANGE = 0, the reset default; with ADCRANGE = 1 the full scale is 20.48 mV):

$$I_{\max} = 81.92\,\frac{\mathrm{mV}}{R}$$

  For the two INA228 monitors the full scale is 163.84 mV (ADCRANGE = 0): 1.6384 A on U29 (R41 0.1 Ω) and 16.384 mA on U53 (R278 10 Ω), calculated.
- The two INA228 alert pins are wired together as 5V_CURR_ALERT (open drain, pulled up to +1V8) and read by RP2040 GPIO28.
- **Module current range (auto-ranging).** U29 measures across R41 (0.1 Ω) at all times. U53 measures across R278 (10 Ω), which is in series with the module (VDD_5V_IN, E2 pads R1, R2, S1, S2) only while P-FET Q20 is off. Comparator U36 (TLV7021) compares VDD_5V_IN with VMID × 124/125 (divider R293 1 kΩ / R294 124 kΩ). When the drop across R278 passes about 40 mV (about 4 mA at 5 V, calculated), its open-drain output (R39 100 kΩ to +5V_C, C5 0.10 µF) clears flip-flop U35 (SN74LVC1G74). Q goes low and turns Q20 on, which bypasses R278.
- The bypass latches. While Q20 is on, U36 sees only the small drop across Q20, so /CLR is high. To return to the 10 Ω range, drive GPIO6 (RP_CURR_SEL) high and then low. Q19 inverts the pulse, so the falling edge on GPIO6 clocks D (tied to +5V_C) into U35. Q goes high and Q20 turns off, whatever the module draws. If the module then draws more than the trip current, the drop across R278 trips U36 again, U35 is cleared and Q20 turns back on. Until that happens the module supply dips by up to the module current × 10 Ω (about 1 V at 100 mA). Read GPIO26 after the pulse to check which range is active.
- The RP2040 reads the range on GPIO26/ADC0 (RP_CURR_STATUS): /Q through R295 100 kΩ / R296 47 kΩ. This gives about 1.6 V with the bypass on and about 0 V in the 10 Ω range (calculated). At power-up C5 holds /CLR low, so the board starts with the bypass on (inferred from the circuit).

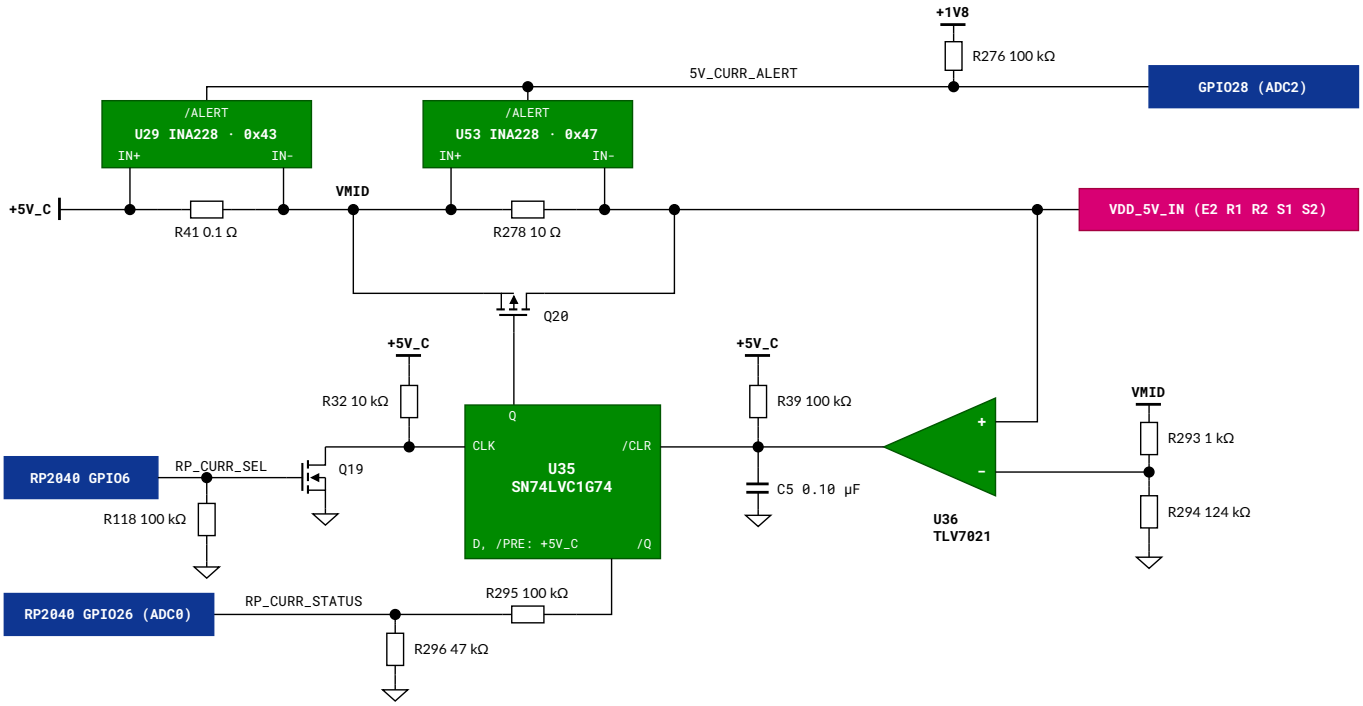


Figure 8 Module 5 V current auto-ranging: R41/R278 shunts, Q20 bypass, comparator U36, flip-flop U35 and the RP2040 control lines (simplified)

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Warning: In the 10 Ω range the module supply drops by up to about 40 mV before U36 trips. A fast load step is limited by R278 until Q20 turns on, and VDD_5V_IN has only C204 (0.10 µ F) on the board. Switching back to the 10 Ω range with GPIO6 while the module draws more than a few milliamps causes a short supply dip of up to the module current × 10 Ω (about 1 V at 100 mA) until Q20 turns on again. This can brown out the module. Select the 10 Ω range only while the module is already in sleep or another low-current state.

- The camera rail monitors U32 and U34 sit behind the jumpers P14 and P15 (see Camera Interfaces).
- Which bus the monitors are on depends on slide switch S6 (see I2C Bus Map).

Tip: Use the monitors to log rail consumption during boot, radio activity, display usage, and camera streaming: especially useful for comparing firmware power states or module variants side-by-side.

6 Boot, Reset, and Debug

6.1 RP2040 Debug Probe

The EVK carries an RP2040 microcontroller (U55) that acts as the debug probe and provisioning controller. It is powered from +1V8 (I/O) and +3V3 (USB and regulator input), runs from the 12 MHz crystal Y1, and has a 16 Mbit QSPI flash U54. Its USB port is on J5 (the same connector that carries USB-PD power). The RP2040 is also the EVK's USB-to-UART console bridge: with S7 on the RP2040 side, the module UART0 is a USB serial port on J5. There is no separate USB-UART bridge chip.

The RP2040 SWD header P18 is **not fitted**. To put the RP2040 in USB boot mode use button S2 (BOOTSEL) or the open solder jumper JP7; S3 resets the RP2040.

All 30 RP2040 GPIOs are used:

GPIO	Net	Function
GPIO0	R_RP_UART0.TX	UART0 TX to module console (E1 UART0_RX, through U3 and switch S7)
GPIO1	R_RP_UART0.RX	UART0 RX from module console
GPIO2	RP_GPIO2	I2C1 SDA to module pad V3 (RSVD6) through U14
GPIO3	RP_GPIO3	I2C1 SCL to module pad U3 (RSVD5) through U14
GPIO4	RP_UART1_TX	UART1 TX to module debug RX (DBG_RX, AE3)
GPIO5	RP_UART1_RX	UART1 RX from module debug TX (DBG_TX, AD3), through U56
GPIO6	RP_CURR_SEL	Module current range select (pulses Q19)
GPIO7	RTC_WAKE_N_RP	Monitor of RTC_WAKE_N (module pad P3)
GPIO8	MCU_RST_RP	PORn hold: drives Q17, which pulls module PORn low
GPIO9	I2C0_LINK_N_RP	I2C0 link enable (Q29, U58); the link is disabled by default
GPIO10	R215	BOOT3 to module pad V1
GPIO11	R207	BOOT2 to module pad U1
GPIO12	R216	BOOT1 to module pad U2
GPIO13	R208	BOOT0 to module pad V2
GPIO14	PD_ACTIVE_n	USB-PD power present (low = live)
GPIO15	PWR_FLT_N	Input eFuse fault (low = fault)
GPIO16	TMS/SWDIO_RP	SWDIO through mux U57
GPIO17	TCK/SWDCLK_RP	SWCLK through mux U57
GPIO18	TDO_RP	TDO through mux U57

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GPIO	Net	Function
GPIO19	MARKER_RP	MARKER line to module pad AG6
GPIO20	JTAG_RST_RP	JTAG reset (open drain through Q16) through mux U57
GPIO21	LED	Status LED D53 (green) through Q27
GPIO22	MODULE_STBY_RP	MODULE_STBY pull-down: drives Q15
GPIO23	MODULE_EN_RP	MODULE_EN pull-down: drives Q18
GPIO24	RP_I2C.SDA	RP2040 I2C0 SDA (to S6 and U58)
GPIO25	RP_I2C.SCL	RP2040 I2C0 SCL
GPIO26	RP_CURR_STATUS	Module current range bypass state (ADC0)
GPIO27	SWD_SEL	Debug target select (ADC1): 0 = module, 1 = Wi-Fi coprocessor debug pads
GPIO28	5V_CURR_ALERT	INA228 alert (ADC2)
GPIO29	VIO_OUT / 2	VIO_OUT sense (ADC3)

Table 5 RP2040 GPIO map

6.1.1 SWD target select

Mux U57 (TMUX1574) routes GPIO16, GPIO17, GPIO18 and GPIO20 to one of two targets, selected by SWD_SEL (GPIO27, default 0):

- **0 (default):** the module debug pads and header J2.
- **1:** the Wi-Fi coprocessor debug pads on header P19.

P19 (6-pin): pin 1 WIFI_RST, pin 2 0 V, pin 3 WIFI_LOGGER, pin 4 WIFI_SWDIO, pin 5 WIFI_SWCLK, pin 6 +1V8.

> **Warning:** P19 pin 6 is the **carrier** +1V8 rail, not a module supply. Do not connect it to a module supply or to another probe's target-voltage input unless that probe expects to be driven by this rail. Do not select SWD_SEL = 1 unless the Wi-Fi coprocessor is powered: the RP2040 drives its debug pads directly.

6.2 Debug Connectors

- **J2:** 10-pin debug header (FTSH-105): pin 1 +VIO_SW (target reference), pin 2 TMS/SWDIO, pin 4 TCK/SWDCLK, pin 6 TDO, pin 8 TDI, pin 10 JTAG_RST, pins 3, 5 and 9 0 V, pin 7 is the key (no pin). The header and the on-board RP2040 share the same lines through U57.
- **P19:** Wi-Fi coprocessor debug header (see above).
- **P18** (RP2040 SWD) and **P13** (module debug UART) are **not fitted**.

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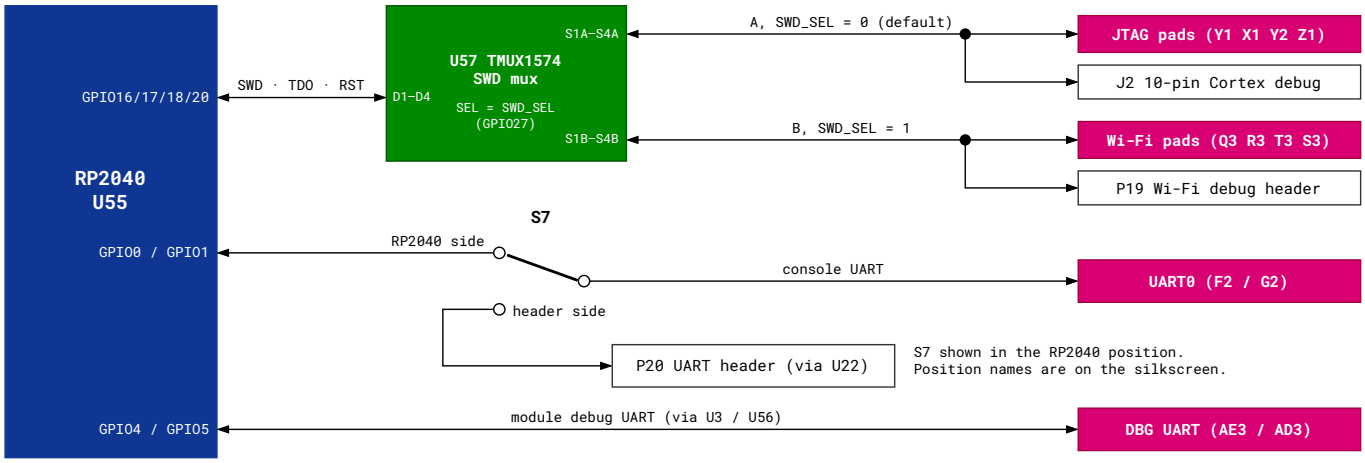


Figure 9 Debug and console routing: SWD target mux U57 and console switch S7 (simplified)

6.3 Reset

S1 is the module reset switch (PORn of the module, net MCU_RST). Capacitor C1 is 1 nF. The RP2040 can also hold the module in reset through Q17, driven by GPIO8.

No reset readback The RP2040 can **hold** PORn low but cannot read it back. Any procedure that waits for PORn to rise cannot be done in hardware. Only VIO_OUT (GPIO29) can be observed.

Module-side pulls Reset pin has an internal pull-up. The carrier adds no pull-up to PORn.

6.4 Boot Mode Selection

The BOOT0 to BOOT3 module pads (V2, U2, U1, V1) are connected through 10 kΩ resistors to RP2040 GPIO13 to GPIO10. The BOOT DIP switch SW1 and its related parts (S4, S5, R93, R94, R105, R106) are **not fitted** on the E1M-AEN build, so there is no switch and no pull on the carrier.

Module-side pulls Pull-up or pull-down for the boot pins must be provided inside the module. On E1M-AEN the BOOT pads are not connected.

6.5 Module Control Pins

Signal	E1 pad	Carrier wiring
MODULE_EN	O1	Header P11 (jumper to 0 V). N-FET Q18, gate = RP2040 GPIO23 (10 kΩ to 0 V). GPIO23 high or P11 fitted = module off. No pull-up on the carrier.
MODULE_STBY	O2	Header P12 (jumper to 0 V). N-FET Q15, gate = RP2040 GPIO22 (10 kΩ to 0 V). GPIO22 high or P12 fitted = standby request. No pull-up on the carrier.
PORn	W1	Button S1, C1 1 nF, N-FET Q17, gate = GPIO8 (hold only, see Reset).
RTC_WAKE_N	P3	R256 100 kΩ to +VIO_SW; through U3 to RP2040 GPIO7.
VIO_OUT	P1, P2	Enables U1; sensed on GPIO29 (see Carrier I/O rail).

Table 6 Module control pins

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- **P11** header: “Short to disable module” (MODULE_EN control). On E1M-AEN this is a hard power cut with no notice to firmware: an MRAM or OSPI flash write in progress is lost or corrupted. Use it for recovery only. The RP2040 does the same when GPIO23 is driven high.
- **P12** header: MODULE_STBY control. On E1M-AEN the standby behaviour is set by firmware (pulse protocol: each short is one sleep/wake event; level protocol: shorted = stay in STOP). A short of ≥ 10 ms wakes the module from self-off if firmware armed that wake. The RP2040 does the same when GPIO22 is driven high.

Pad levels on E1M-AEN R3 modules. MODULE_EN (pad O1) and MODULE_STBY (pad O2) accept 1.8 V logic. With nothing driving them the pads sit at about 1.2 to 1.5 V, never above 1.8 V; the module input threshold is 1.25 V. No carrier pull-up is needed. A carrier may drive a pad with an open-drain or open-collector output or a switch to 0 V (preferred, and what the EVK N-FETs and headers do), or push-pull from 1.8 V, 3.3 V or 5 V logic with a high level (V_{OH}) of 1.45 to 5.5 V. The low level must be 0.4 V or less at the pad, and the pad sinks about 1.8 µA while held low. Off-state leakage on the carrier (including any TVS) must be 0.1 µA or less. Both pads stay 5 V tolerant (5.5 V maximum). Because the released level exists only on the module, a carrier that wants to read the line back must fit its own pull-up.

> **Warning:** A host pin that can be unpowered while the module must stay on clamps the line to about 0.5 V through its ESD diodes, which turns the module off. Buffer such a pin with an N-MOSFET or use an open-drain output that is high-impedance when unpowered.

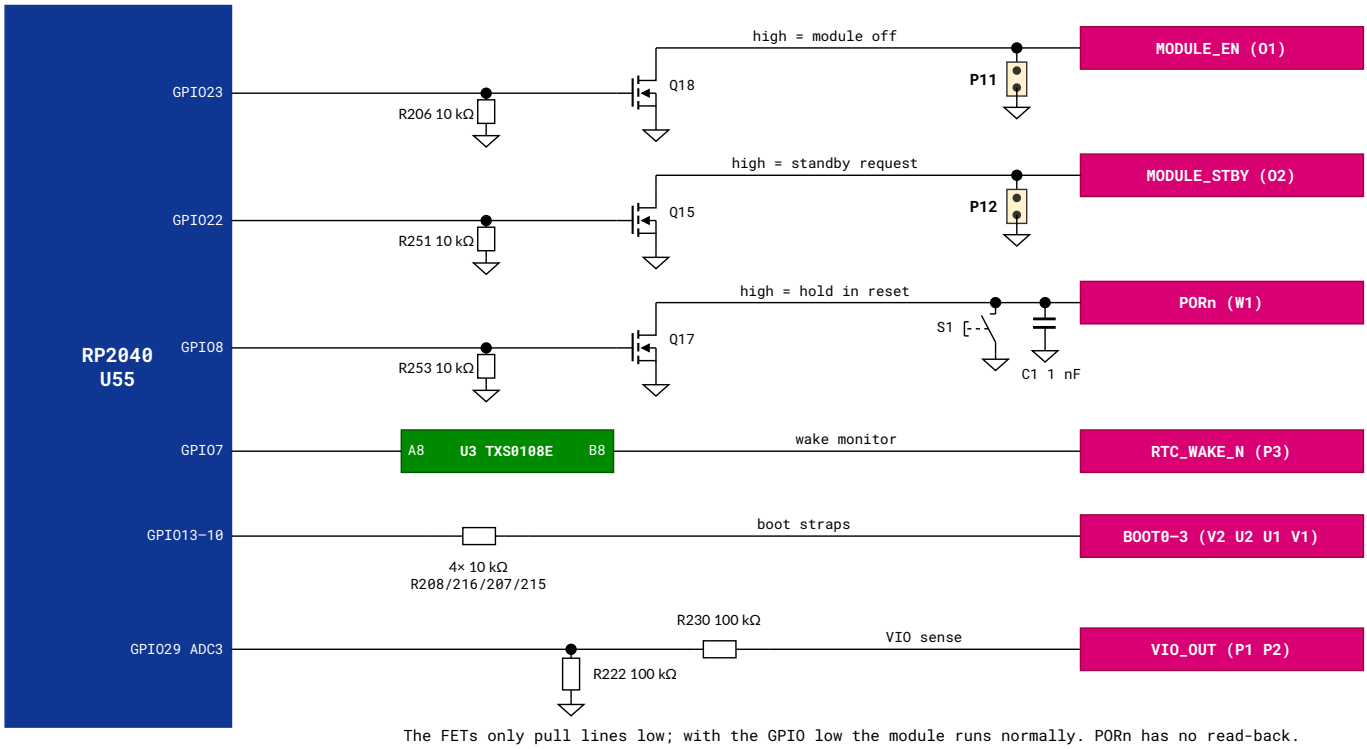


Figure 10 Module control from the RP2040: enable, standby, reset, wake, boot straps and VIO sense (simplified)

6.6 Antenna

The carrier routes the module 2.4 GHz antenna pad (ANT_2.4GHZ, pad AH1) to one of two antenna options. The choice is made with 0 Ω resistors, not with a jumper.

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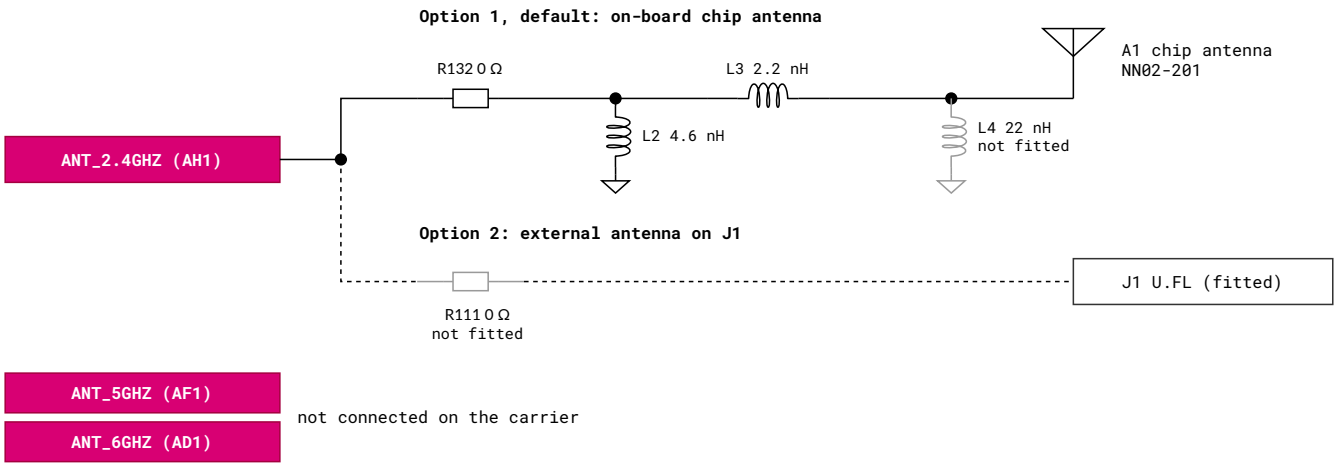


Figure 11 Antenna options on the 2.4 GHz pad (simplified)

6.6.1 Option 1: on-board chip antenna (default)

R132 (0 Ω) connects the pad to the Ignion NN02-201 chip antenna A1 through a matching network: L2 (4.6 nH, shunt to 0 V) and L3 (2.2 nH, series). A second shunt position at the antenna feed, L4 (22 nH), is not fitted. This is the assembled state.

6.6.2 Option 2: external antenna on J1

J1 is a U.FL connector. It is fitted but not connected: its link resistor R111 is not fitted. To use an external antenna:

1. Remove R132.
2. Fit a 0 Ω resistor at R111.
3. Connect the antenna to J1 before the radio is switched on.

Warning: Fit only one of R111 and R132. With both fitted the pad drives the chip antenna and the J1 path in parallel, which detunes the match. Using a different antenna can affect the radio's regulatory approval: check the module's regulatory notes first.

6.6.3 5 GHz and 6 GHz antenna pads

The module pads ANT_5GHZ (AF1) and ANT_6GHZ (AD1) are not connected on the carrier. A module that uses these pads for its radio has no antenna path on this EVK.



Figure 12 2641-R3 antenna area photo: chip antenna A1, U.FL J1, R111 / R132 positions

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6.7 Jumpers, Switches and Buttons

Each jumper and switch is described below with its positions and the recommended position for a first power-up. The recommendation is not necessarily how the board ships: check every position before you connect power.

6.7.1 P1: display I/O level (+L_VIO)

> **Warning:** With a 3.3 V module (VIO_OUT and +VIO_SW at 3.3 V) do not set P1 to 1.8 V: the level shifter U4 needs +L_VIO at or above +VIO_SW, and a 1.8 V panel would see 3.3 V from the module and can be damaged.

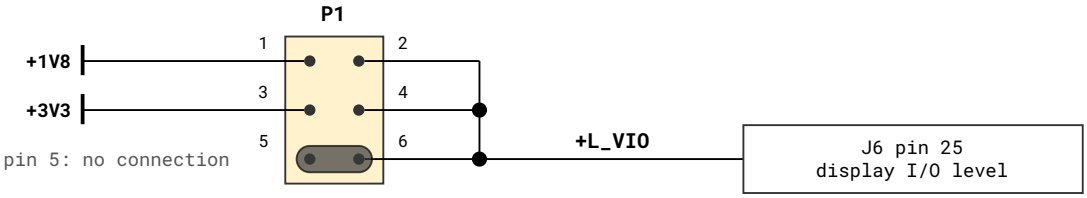
Sets the I/O voltage of the display connector J6: J6 pin 25 and the panel-side pull-ups of U4 (panel power enable, panel reset, touch interrupt and reset, touch I2C and the backlight PWM). Pin 5 is not connected, so in position 5-6 +L_VIO is not supplied (it floats): J6 pin 25 and the panel-side pull-ups are then unpowered.

- **1-2:** 1.8 V.
- **3-4:** 3.3 V.
- **5-6:** unpowered.

Pins 1 and 3 carry +1V8 and +3V3; pin 5 is not connected. Pins 2, 4 and 6 are all +L_VIO.

Recommended: the I/O level of your panel; 5-6 when no panel is attached.

> **Warning:** Fit only one shunt on P1: shunts on 1-2 and 3-4 together short +1V8 to +3V3.

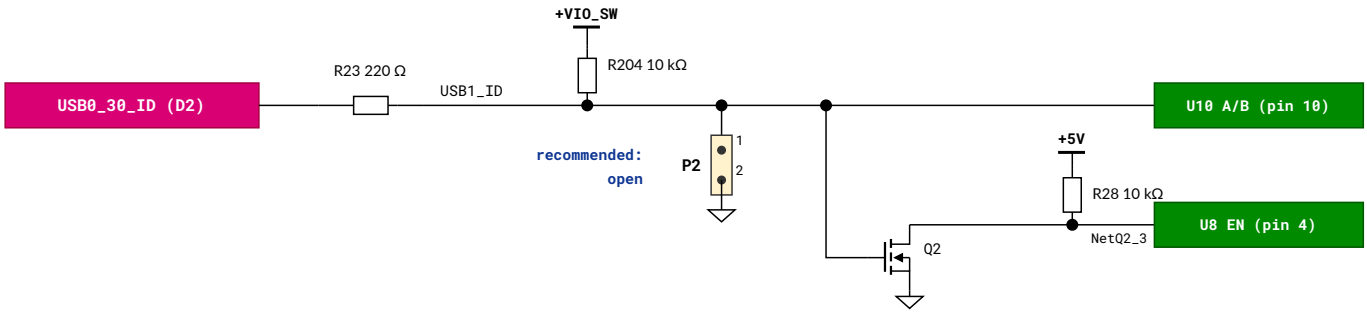


Shunt shown on 5-6: recommended with no panel attached (+L_VIO unpowered).
With a panel: 1-2 for 1.8 V, 3-4 for 3.3 V, the level your panel needs.
Fit one shunt only: two shunts short +1V8 and +3V3 together.

Figure 13 P1 display I/O level select

6.7.2 P2: USB0 host select (USB1_ID)

Ties USB1_ID to 0 V. USB1_ID comes from module pad D2 (USB0_30_ID) through R23 (220 Ω) and is pulled up to +VIO_SW by R204 (10 kΩ). It drives the U10 select pin (where module USB0 goes, see U10 below) and the gate of N-FET Q2. The Q2 drain is the U8 enable, pulled up to +5V by R28 (10 kΩ): with P2 open and +VIO_SW up, Q2 holds U8 off, and with P2 fitted U8 switches the USB-A VBUS on. R204 is supplied from +VIO_SW and USB1_ID has no pull-down: while +VIO_SW is off (module VIO_OUT off or not yet up), Q2 has no gate drive and R28 holds U8 on, so USB-A VBUS is on whenever +5V is present.



Open: USB1_ID high (R204), USB0 to J12 USB-C; Q2 on pulls U8 EN low, USB-A VBUS off.
Fitted: USB1_ID low, USB0 to J11 USB-A host; Q2 off, R28 pulls U8 EN high, USB-A VBUS on.

Figure 14 P2 USB0 host select

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- **Fitted:** USB0 goes to the USB-A host port J11, and USB-A VBUS is switched on.
- **Open:** USB0 goes to the USB-C port J12; USB-A VBUS stays off.

Recommended: open, unless you need the USB-A host port.

6.7.3 P9: Arduino / mikroBUS I/O level (+VARD)

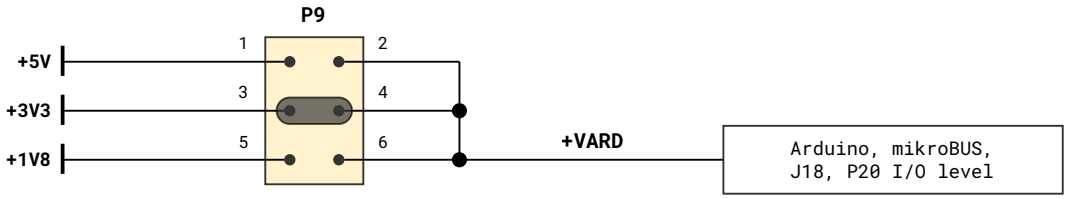
> **Warning:** With a 3.3 V module (VIO_OUT and +VIO_SW at 3.3 V) do not set P9 to 1.8 V (5-6): the LSF level shifters need +VARD at or above +VIO_SW, and a 1.8 V shield would see 3.3 V from the module and can be damaged.

Sets +VARD, the I/O voltage of the Arduino headers P3 to P6, the mikroBUS headers P7 and P8, the encoder header J18 and the UART header P20. +VARD feeds the header-side pull-ups of the translators, P3 pin 2 (IOREF), J18 pin 1 and P20 pin 1. It does not change the fixed supply pins (+3V3 on P3 pin 4 and P7 pin 7, +5V on P3 pin 5 and P8 pin 7) or the analog inputs on P4.

- **1-2:** 5 V.
- **3-4:** 3.3 V.
- **5-6:** 1.8 V.

Recommended: 3-4 (3.3 V), or the level your shield or click board needs.

> **Important:** Set P9 before you attach a shield or click board: a level that is too high can damage it. Fit only one shunt: two shunts short two of +5V, +3V3 and +1V8 together.



Shunt shown on 3-4: recommended, +VARD = 3.3 V.

1-2: 5 V; 5-6: 1.8 V. Set it before you attach a shield or click board.
Fit one shunt only: two shunts short two supply rails together.

Figure 15 P9 Arduino / mikroBUS I/O level select

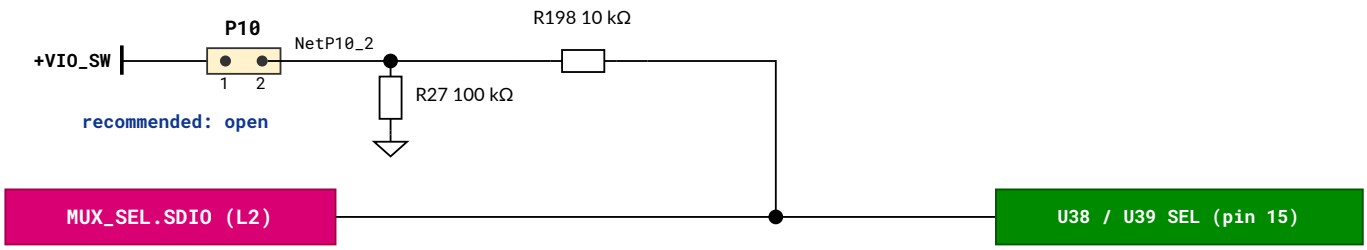
6.7.4 P10: SDIO mux select

Pulls the SDIO mux select line MUX_SEL.SDIO up to +VIO_SW through R198 (10 kΩ) (see U38 / U39 below). With P10 open, R27 (100 kΩ) pulls the line low through R198. Module pad L2 (IO0) is on the same line, so module firmware can also drive it.

- **Fitted:** SDIO goes to the M.2 Key E slot.
- **Open:** SDIO goes to the microSD socket J7.

Recommended: open. The M.2 slot is not fitted in this assembly, so fitting P10 disconnects the microSD card.

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Open: R27 pulls SEL low through R198 (module IO0 may also drive it): SDIO to microSD J7.
Fitted: SEL high through R198: SDIO to the M.2 Key E side (not fitted).

Figure 16 P10 SDIO mux select: +VIO_SW through P10 and R198 10 kΩ to MUX_SEL.SDIO (module L2, U38 / U39 SEL). R27 100 kΩ pulls it low when open. Recommended: open.

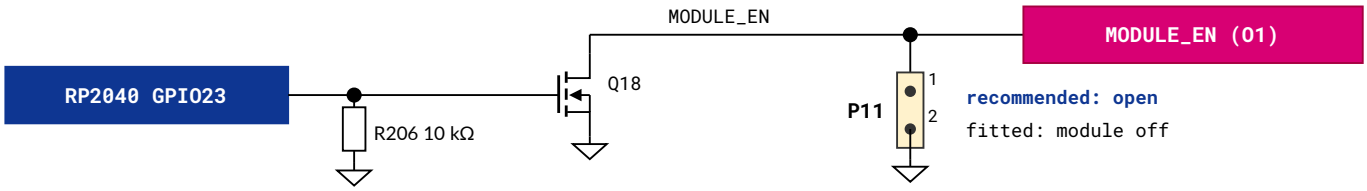
6.7.5 P11: module enable (MODULE_EN)

Ties MODULE_EN (module pad 01) to 0 V, in parallel with N-FET Q18, which the RP2040 switches on with GPIO23 (R206 10 kΩ pull-down on the gate).

- **Fitted:** the module is switched off (hard power cut).
- **Open:** the module runs (the RP2040 can still switch it off).

Recommended: open. Use it only for recovery.

> **Warning:** Fitting P11 cuts module power with no notice to firmware: a flash or MRAM write in progress is lost or corrupted.



GPIO23 high or a shunt on P11 pulls MODULE_EN low: hard power cut, no notice to firmware.

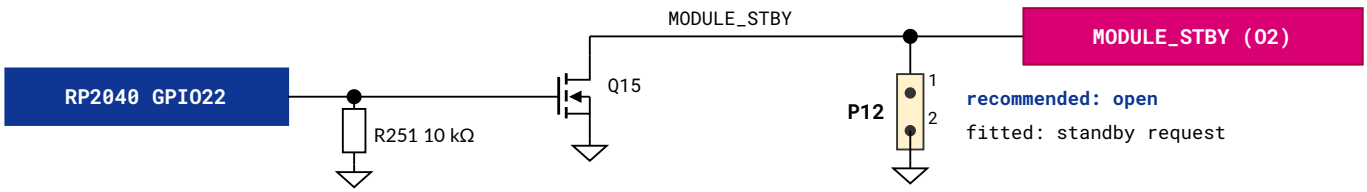
Figure 17 P11 module enable: MODULE_EN (01) to 0 V, in parallel with N-FET Q18 driven by RP2040 GPIO23 (R206 10 kΩ pull-down). Recommended: open.

6.7.6 P12: module standby (MODULE_STBY)

Ties MODULE_STBY (module pad 02) to 0 V, in parallel with N-FET Q15, which the RP2040 switches on with GPIO22 (R251 10 kΩ pull-down on the gate).

- **Fitted:** the module is asked to enter standby.
- **Open:** normal operation.

Recommended: open.



GPIO22 high or a shunt on P12 pulls MODULE_STBY low: the module is asked to enter standby.

Figure 18 P12 module standby: MODULE_STBY (02) to 0 V, in parallel with N-FET Q15 driven by RP2040 GPIO22 (R251 10 kΩ pull-down). Recommended: open.

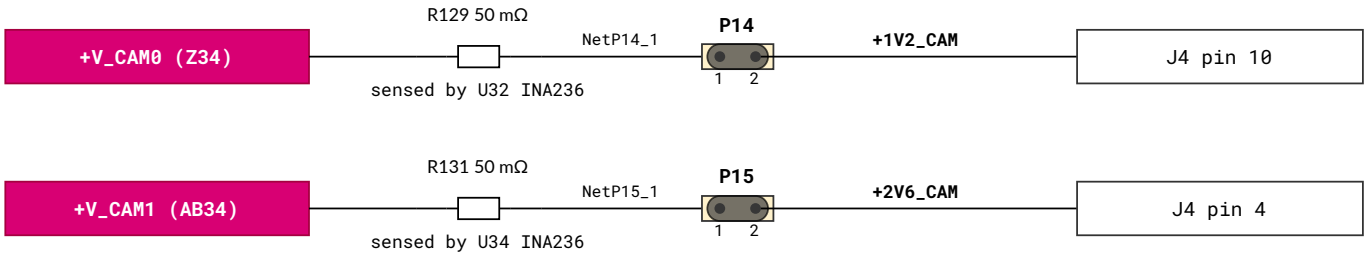
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6.7.7 P14 and P15: camera supplies to J4

Connect the module camera rails to the parallel camera connector J4, through the current-sense resistors R129 and R131.

- **P14 fitted:** +1V2_CAM (from module +V_CAM0, pad Z34, through R129, measured by U32) reaches J4 pin 10.
- **P15 fitted:** +2V6_CAM (from module +V_CAM1, pad AB34, through R131, measured by U34) reaches J4 pin 4.
- **Open:** J4 gets no camera supply.

Recommended: fit both when a DVP camera is on J4; leave them open otherwise.



Shunts shown: recommended when a DVP camera is on J4.
Without a camera leave both open: J4 then gets no camera supply.

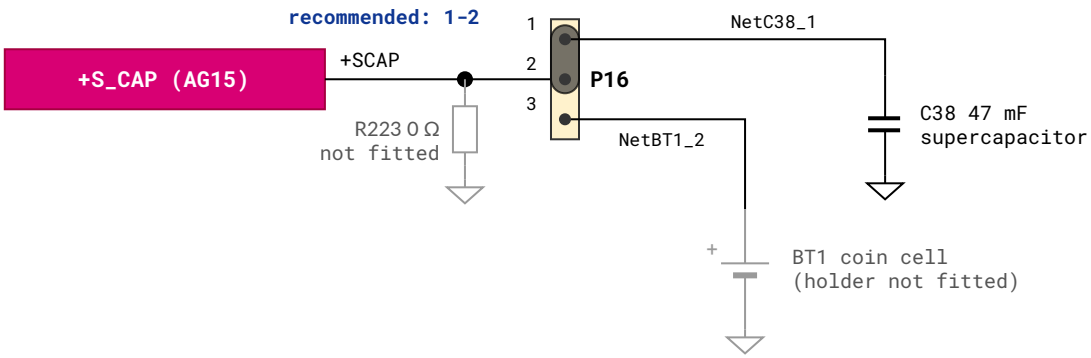
Figure 19 P14 / P15 camera supplies: module +V_CAM0 (Z34) through R129 50 mΩ (U32) and P14 to +1V2_CAM (J4 pin 10). Module +V_CAM1 (AB34) through R131 50 mΩ (U34) and P15 to +2V6_CAM (J4 pin 4). Shunts = recommended with a DVP camera on J4.

6.7.8 P16: RTC backup store (+S_CAP)

Selects what backs up the module RTC on +S_CAP (module pad AG15).

- **1-2:** supercapacitor C38 (47 mF), charged by the module.
- **2-3:** coin cell BT1 (holder not fitted in this assembly).
- **Open:** no backup store, and +S_CAP floats (the 0 V tie R223 is not fitted). Avoid this.

Recommended: 1-2.



1-2: C38, charged by the module. 2-3: BT1. Open: +S_CAP floats (R223 not fitted).

Figure 20 P16 RTC backup store: pin 2 = +SCAP (module +S_CAP, AG15), pin 1 = C38 47 mF, pin 3 = BT1 anode (holder not fitted). R223 0 Ω to 0 V not fitted. Shunt on 1-2 = recommended.

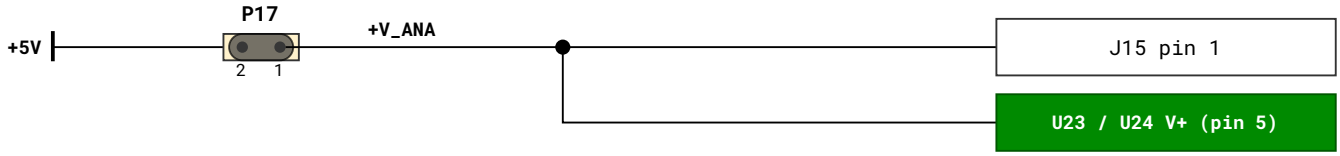
6.7.9 P17: analog supply (+V_ANA)

Connects +5V (pin 2) to +V_ANA (pin 1), the supply of the two DAC buffer op-amps U23 and U24 (OPA189IDBVR) and of J15 pin 1.

- **Fitted:** the DAC header J15 works.
- **Open:** the DAC buffers are unpowered.

Recommended: fit it when you use J15.

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Shunt shown: recommended when you use the DAC header J15.
Open: the DAC buffers U23 / U24 (OPA189IDBVR) are unpowered and J15 pin 1 has no supply.

Figure 21 P17 analog supply: pin 2 = +5V, pin 1 = +V_ANA (J15 pin 1, U23 / U24 V+). Shunt = recommended when J15 is used.

6.7.10 P19: Wi-Fi coprocessor debug header

Not a jumper: a 6-pin header for an external debugger on the Wi-Fi coprocessor debug pads. The on-board RP2040 can reach the same pads (see U57 below).

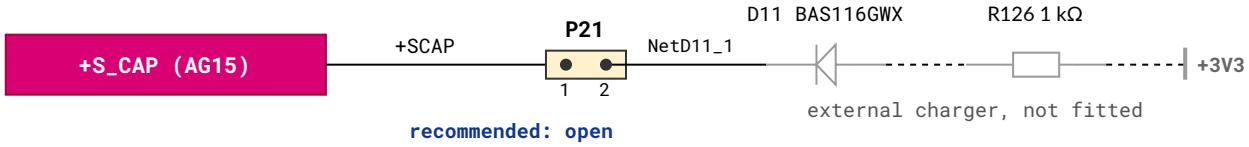
6.7.11 P21: external RTC charger

Connects the external charger to +S_CAP: +3V3 through R126 (1 kΩ) and diode D11 (BAS116GWX), both not fitted in this assembly. P21 pin 1 is +S_CAP, pin 2 is the D11 cathode.

- **Fitted:** the charger is connected.
- **Open:** the module charges C38 by itself.

Recommended: open.

> **Warning:** Never fit P21 while a primary (non-rechargeable) coin cell is selected on P16 pins 2-3: the charger would charge the cell.

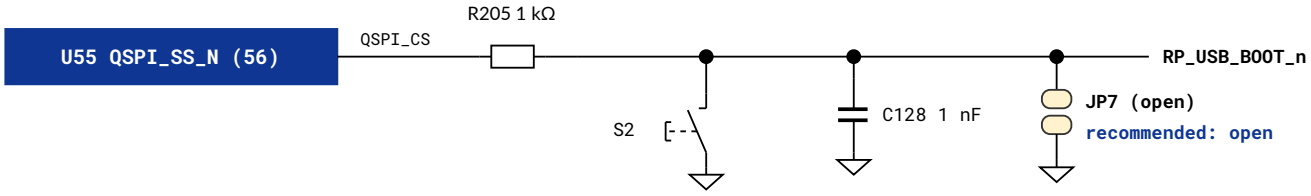


Never fit P21 while a primary coin cell is selected on P16 2-3: the charger would charge it.

Figure 22 P21 external RTC charger: pin 1 = +SCAP, pin 2 = D11 cathode. D11 BAS116GWX and R126 1 kΩ from +3V3 not fitted. Recommended: open.

6.7.12 JP7: RP2040 boot (solder jumper)

An open solder jumper from the RP2040 boot line RP_USB_BOOT_n to 0 V, in parallel with button S2. The line reaches the RP2040 flash chip-select QSPI_SS_N (U55 pin 56) through R205 (1 kΩ). Bridging it forces the RP2040 into its USB bootloader at every reset. **Recommended:** leave it open; use the S2 button instead.



Bridging JP7, or holding S2, pulls RP_USB_BOOT_n low: the RP2040 starts its USB bootloader at the next reset (S3). Use S2 instead of bridging JP7.

Figure 23 JP7 open solder jumper from RP_USB_BOOT_n to 0 V, in parallel with S2 and C128 1 nF. R205 1 kΩ to RP2040 QSPI_SS_N (U55 pin 56). Recommended: open.

6.7.13 S6: current-monitor bus switch

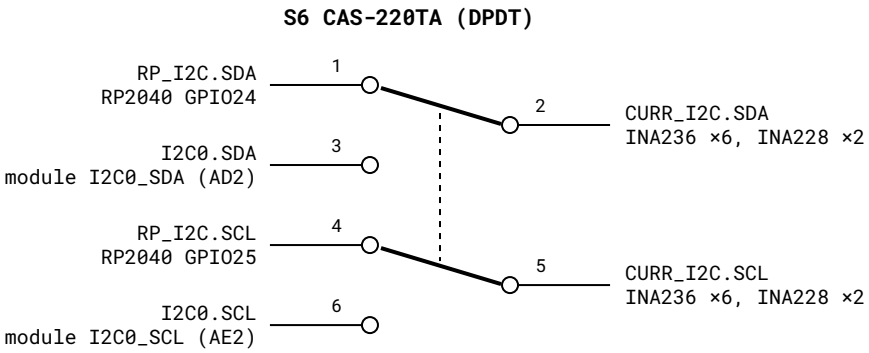
A slide switch that connects the eight current monitors (CURR_I2C) to one of two I2C masters.

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- **RP2040 side (pins 1-2 and 4-5):** CURR_I2C joins RP_I2C (GPIO24 / GPIO25); the RP2040 debug probe reads the monitors.
- **Module side (pins 2-3 and 5-6):** the monitors join the module I2C0 bus (pads AD2 / AE2), and your firmware reads them.

S6 keeps the two hosts apart only while the U58 link (see U58 below) is off, which is its default. If the RP2040 drives GPIO9 low, U58 joins RP_I2C to I2C0, and the RP2040 and the module share one bus in either S6 position.

Recommended: RP2040 side. The position names are on the silkscreen.



Shown in the recommended position: 1-2 and 4-5 closed, the RP2040 reads the monitors.
Other position: 2-3 and 5-6 closed, the monitors join the module I2C0 bus.
Keep U58 (RP_I2C to I2C0 link) off, its default (GPIO9 high), or the RP2040 and the module share one bus in either position.

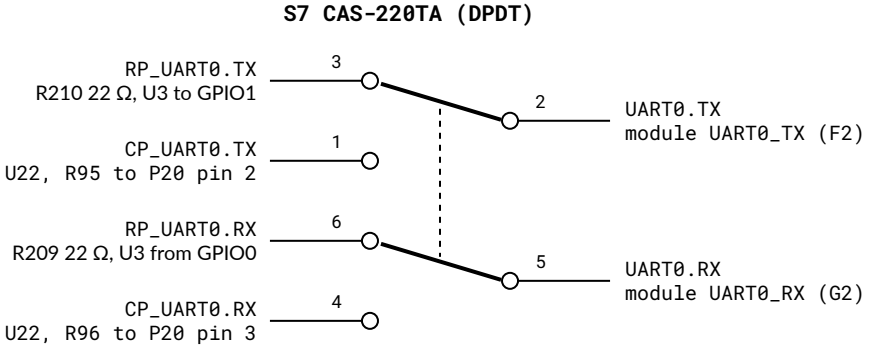
Figure 24 S6 CAS-220TA DPDT: commons 2 / 5 = CURR_I2C.SDA / CURR_I2C.SCL. Throws 1 / 4 = RP_I2C (RP2040 GPIO24 / GPIO25), 3 / 6 = I2C0 (module AD2 / AE2). Shown in the recommended RP2040 position. The positions keep the two hosts apart only while the U58 link stays off (default).

6.7.14 S7: console switch (UART0)

A slide switch that connects module UART0 (pads F2 / G2) to one of two places.

- **RP2040 side (pins 2-3 and 5-6):** UART0 goes through R210 / R209 (22 Ω) and level shifter U3 to RP2040 GPIO1 / GPIO0; the console is a USB serial port on J5.
- **Header side (pins 1-2 and 4-5):** UART0 goes through level shifter U22 to the 4-pin header P20 (pin 2 TX, pin 3 RX), for an external USB-to-UART adapter. The header I/O level is +VARD, set by P9.

Recommended: RP2040 side. The position names are on the silkscreen.



Shown in the recommended position: 2-3 and 5-6 closed, console on the RP2040 (USB on J5).
Other position: 1-2 and 4-5 closed, console on header P20 through level shifter U22.

Figure 25 S7 CAS-220TA DPDT: commons 2 / 5 = UART0.TX (F2) / UART0.RX (G2). Throws 3 / 6 = RP_UART0 (R210 / R209 22 Ω, U3, RP2040 GPIO1 / GPIO0), 1 / 4 = CP_UART0 (U22 to P20). Shown in the recommended RP2040 position.

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6.7.15 Buttons

- **S1:** module reset (PORn).
- **S2:** RP2040 BOOTSEL. Hold it while pressing S3 to start the RP2040 USB bootloader.
- **S3:** RP2040 reset (RUN).

There are no user push buttons and no standby button on the EVK.

6.8 Multiplexers and Selectors

Several carrier switches route one module interface to one of two places. Each is controlled by a module pad (driven by your firmware) or by an RP2040 GPIO (driven by the debug-probe firmware). The default is the state when nothing drives the control line.

6.8.1 U10: USB0 port select

TMUXHS221. Routes module USB0 data (pads B1 / C1).

- **Control:** USB1_ID, module pad D2, with a 10 kΩ pull-up to +VIO_SW. Jumper P2 pulls it low.
- **Low:** USB-A host port J11; USB-A VBUS is switched on.
- **High (default while +VIO_SW is up):** USB-C port J12. While +VIO_SW is off the line is low: USB0 goes to J11 and USB-A VBUS is on.

6.8.2 U47: USB2 port select

TMUXHS221. Routes module USB2 data (pads I1 / J1).

- **Control:** USB2_SELECT, module pad A18, with a 100 kΩ pull-down.
- **Low (default):** USB-C port J13.
- **High:** M.2 Key E slot (not fitted).

Keep USB2_SELECT low.

6.8.3 U38 and U39: SDIO select

Two TMUX1574. Route the module SDIO lines (pads AG11 to AH14).

- **Select:** MUX_SEL.SDIO, module pad L2, with a 100 kΩ pull-down. Jumper P10 pulls it up.
- **Enable:** MUX_EN, module pad AG34, active low. No resistor on the carrier; only the multiplexer's weak internal pull-down.
- **Select low (default):** microSD socket J7.
- **Select high:** M.2 Key E SDIO (not fitted).

Drive MUX_EN low in board init rather than relying on the weak internal pull-down.

6.8.4 U46: I2S select

TMUX1574. Routes module I2S0 (pads AD33 to AE34).

- **Select:** I2S_SELECT, module pad AH34. No resistor on the carrier; only the multiplexer's weak internal pull-down.
- **Enable:** I2S_EN, module pad AG33, active low. No resistor on the carrier; only the weak internal pull-down.
- **Select low:** the amplifiers U27 / U28.
- **Select high:** M.2 Key E I2S (not fitted).

The weak internal pull-downs select the amplifiers and enable the mux. Drive both lines low before starting audio rather than relying on them.

6.8.5 U57: debug target select

TMUX1574. Routes the RP2040 SWD / JTAG lines (GPIO16, GPIO17, GPIO18, GPIO20).

- **Control:** SWD_SEL, RP2040 GPIO27, with a 100 kΩ pull-down.
- **0 (default):** module JTAG pads, shared with the J2 debug header.
- **1:** Wi-Fi coprocessor debug pads, shared with the P19 header.

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6.8.6 U58: RP2040 link to module I2C0

LSF0102 level shifter between the RP2040 I2C0 bus and the module I2C0 bus.

- **Control:** RP2040 GPIO9, through Q29.
- **GPIO9 low:** the link is on.
- **GPIO9 high (default):** the link is off.

6.8.7 U18: Arduino digital bank

LSF0108 level shifter for Arduino DIO1 to DIO4 and PWM1 to PWM4.

- **Control:** ARD_DIO_CNTRL, module pad W2, with a 10 kΩ pull-up to +VIO_SW (R263). It drives the gate of Q3, which pulls the U18 enable (200 kΩ R177 to +5V) low.
- **Low:** the bank is enabled.
- **High (default):** the bank is disabled. The default needs +VIO_SW: while +VIO_SW is off, Q3 is off and R177 enables U18.

6.8.8 U3: RP2040 to module signals

TXS0108E level shifter for the RP2040 control and debug lines to the module. It is enabled by VIO_PG, the power-good of +VIO_SW. It is on only while the module I/O rail is good, so the RP2040 cannot drive an unpowered module.

> **Important:** MUX_EN, I2S_SELECT and I2S_EN have no pull resistor on the carrier: only the multiplexers' weak internal pull-downs hold them low. Drive them low early in board init, or microSD and audio may be unreliable.

7 USB Subsystem

7.1 USB-C Ports

J12 and J13 are USB-C connectors, USB 2.0 only. Each has 5.1 kΩ pull-downs on CC1 and CC2 (sink only). Their VBUS goes to module pads (C2 for J12, I2 for J13) and to a red LED (D8, D9).

> **Warning:** A host connected to J12 or J13 drives 5 V into the module VBUS pads whether or not the module is powered.

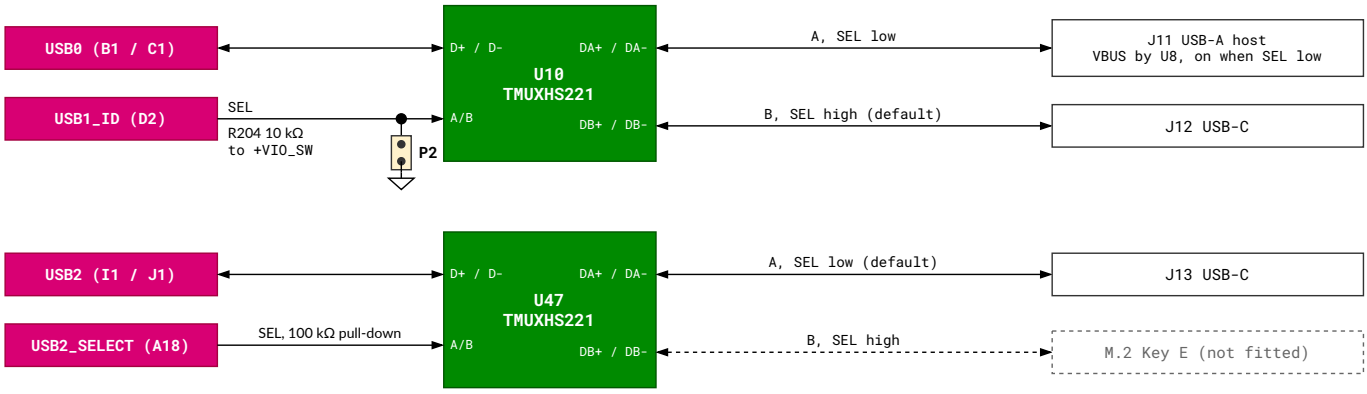


Figure 26 USB data routing: muxes U10 and U47 (simplified)

7.2 USB-A Host Port

J11 (61400416021) is a USB-A connector. Host VBUS is switched from +5V by U8 (TPS25221DRVR); the current limit is set by R16 (90.9 kΩ on ILIM). The output net USB_HOST_VBUS has C34 0.1 µF, C37 2.2 µF, bulk C206 120 µF (35SVPF120M) and the red LED D10 (R31 1 kΩ).

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- **Enable:** U8 EN (pin 4) has R28 10 kΩ to +5V. Q2 pulls it low while USB1_ID is high, so VBUS is on only while USB1_ID is low (P2 fitted, or the module drives pad D2 low) or while +VIO_SW is off (USB1_ID then has no pull-up and Q2 is off). USB1_ID reaches pad D2 (USB0_30_ID) through R23 220 Ω.
- **Fault:** FAULT_N (open drain, low = over-current or over-temperature) is net HOST_VBUS_FAULT on module pad N1 (SPI0_CS1), with R261 10 kΩ to +VIO_SW.
- **Data:** USBH_D_P / USBH_D_N (J11 pins 3 / 2) go to U10 side A (DA+ pin 5, DA− pin 4), with ESD D24 (D+) and D1 (D-). Pin 4 is on 0 V; the shell goes to 0 V through ferrite FB1.

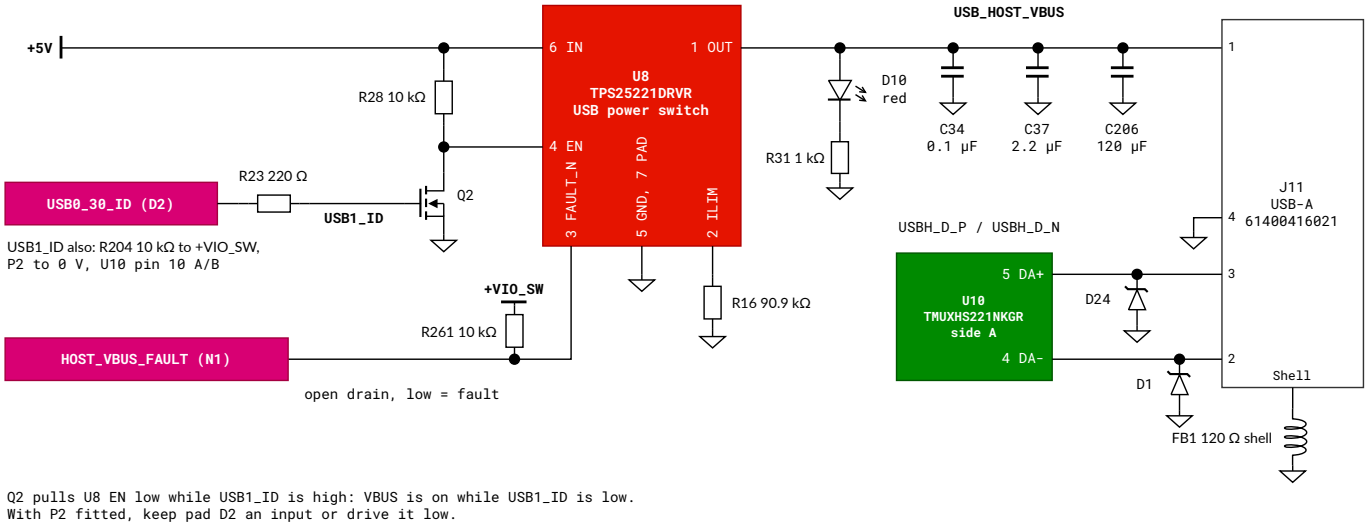


Figure 27 USB-A host port J11 with VBUS switch U8 and Q2 enable (simplified)

Warning: Fitting P2 shorts USB1_ID to 0 V. Pad D2 then sees 0 V through only R23 220 Ω: with P2 fitted, keep D2 an input or drive it low. Driving it high pushes about 15 mA into the short at 3.3 V.

Note: Pad N1 is the module SPI0_CS1 pad. With HOST_VBUS_FAULT on it, configure N1 as an input and do not use SPI0_CS1 for an SPI device.

7.3 Data Muxes and Host ID

- **U10 (TMUXHS221)** on module USB0 data pads B1 / C1: side A goes to the USB-A host J11, side B goes to USB-C J12. The select line is USB1_ID, connected to module pad D2 (USB0_30_ID) through R23 220 Ω and pulled up to +VIO_SW by R204 10 kΩ: USB0 is on J12 by default and on J11 when USB1_ID is low.
- **U47 (TMUXHS221)** on module USB2 data pads I1 / J1: side A goes to USB-C J13 (default). Side B goes to the M.2 slot, not fitted. The select line is USB2_SELECT (module pad A18), pulled down by 100 kΩ; keep it low.
- **P2** header ties USB1_ID to 0 V (host). USB-A VBUS is on only when USB1_ID is low.

Tip: If your software expects OTG / role selection via the ID pin, use P2 to force the intended role (host).

8 Ethernet

- **J8:** ETH0, HR851178A RJ45 with integrated magnetics.
- **J20:** ETH1, same connector and circuit. E1M-AEN has one 100 Mbit PHY (TI DP83825) on ETH0 and leaves the ETH1 pads unconnected, so with E1M-AEN only J8 is live.
- There is no PHY on the carrier: the module provides the PHYs. The four pairs ETHx_DA to ETHx_DD run straight from the module pads to the connector (ETH0: AG30/AH30 to AG27/AH27; ETH1: AG23/AH23 to AG20/AH20, P/N).

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- ESD: one TPD4E05U06DQAR array per two pairs, D35 (DA, DB) and D39 (DC, DD) on J8, D40 and D41 on J20.
- Centre tap TRCT1 (pin 1) is tied to 0 V; TRCT2 (pin 2) is not connected.
- Shield: S1 / S2 go to 0 V through 1 nF in parallel with 1 MΩ (C124 / R117 on J8, C129 / R119 on J20).

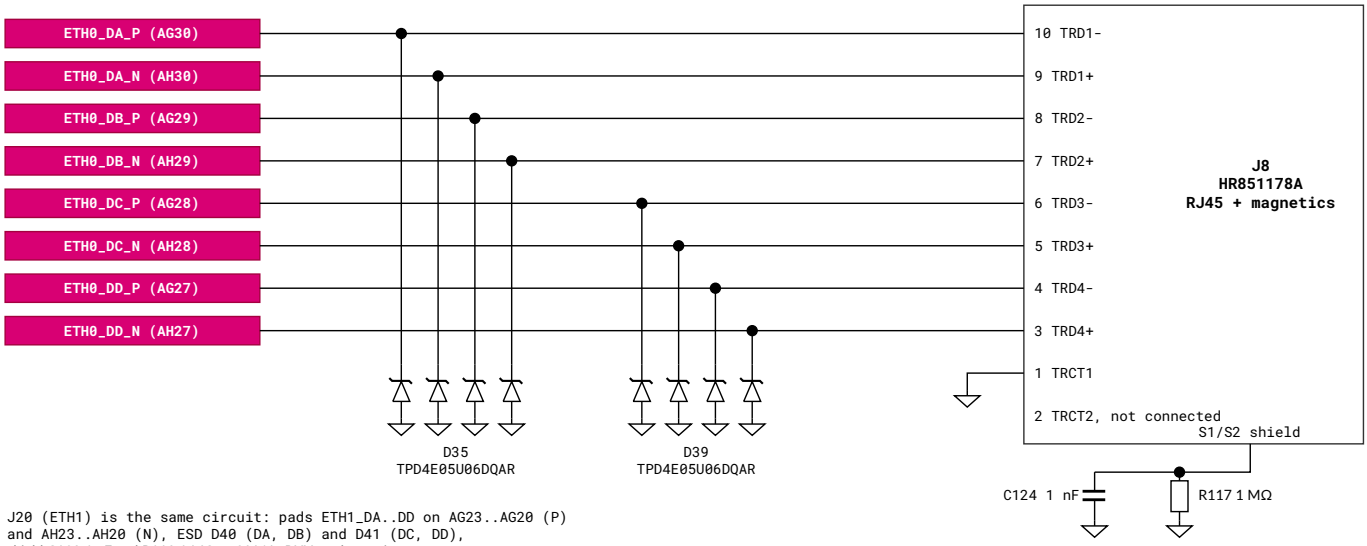


Figure 28 Ethernet port J8 (ETH0): pairs, ESD, centre taps and shield. J20 is the same circuit (simplified)

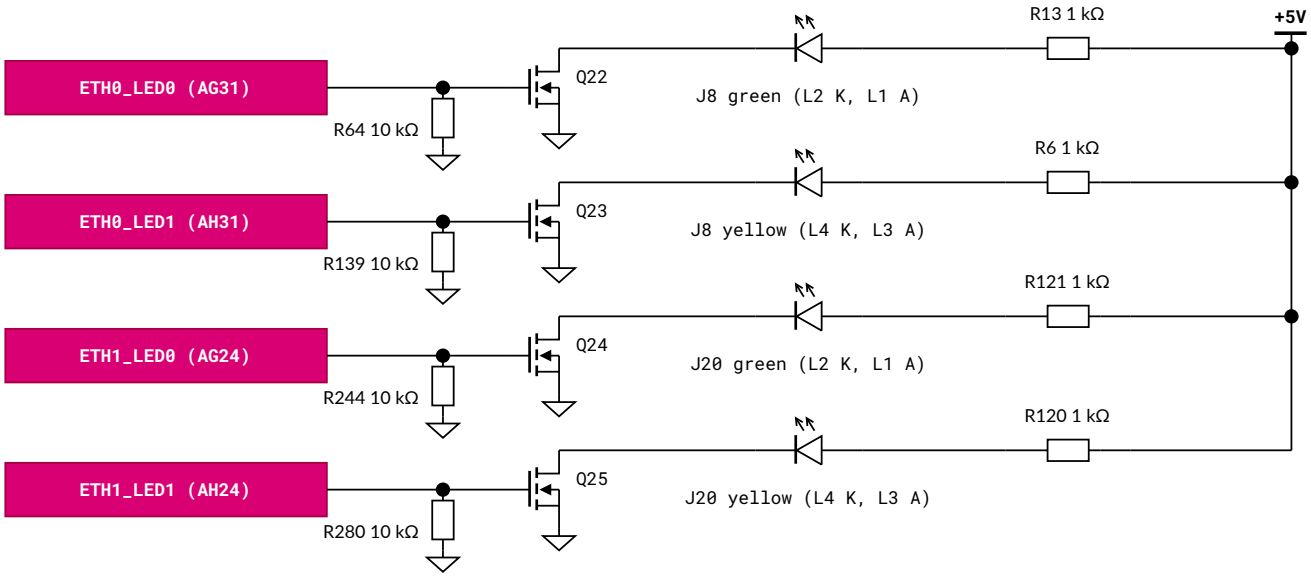
8.1 Link LEDs

Each connector has a green and a yellow LED. The module ETHx_LED0 / ETHx_LED1 pads drive the gates of N-FETs Q22 to Q25 (DMN31D5UFZ-7B, 10 kΩ gate pull-down to 0 V); each FET pulls the LED cathode low, and the anode is fed from +5V through 1 kΩ. A high level on the pad lights the LED.

Pad	FET	Gate pull-down	LED	Anode resistor
ETH0_LED0 (AG31)	Q22	R64	J8 green (L1 A, L2 K)	R13 1 kΩ
ETH0_LED1 (AH31)	Q23	R139	J8 yellow (L3 A, L4 K)	R6 1 kΩ
ETH1_LED0 (AG24)	Q24	R244	J20 green (L1 A, L2 K)	R121 1 kΩ
ETH1_LED1 (AH24)	Q25	R280	J20 yellow (L3 A, L4 K)	R120 1 kΩ

Table 7 Ethernet link LED drivers

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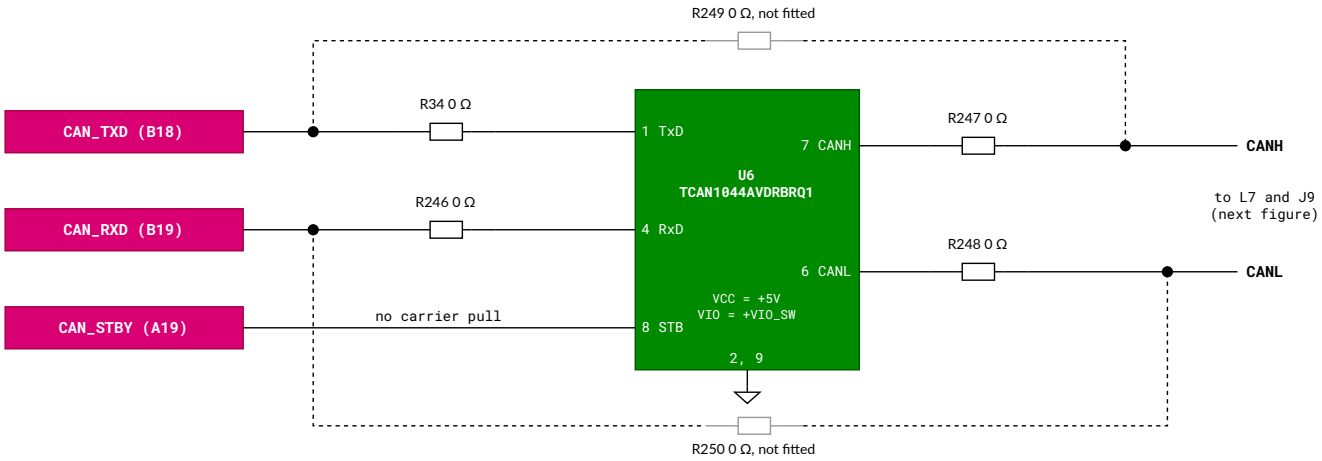
A high level on the LED pad turns the N-FET (DMN31D5UFZ-7B) on and lights the LED.

Figure 29 Ethernet LED drivers Q22 to Q25 (simplified)

9 CAN Bus

9.1 Transceiver

U6 TCAN1044AVDRBRQ1: VCC (pin 3) from +5V, VIO (pin 5) from +VIO_SW. TxD (pin 1) comes from CAN_TXD (module pad B18) through R34 0 Ω; RxD (pin 4) goes to CAN_RXD (B19) through R246 0 Ω. STB (pin 8) is CAN_STBY (A19) with no carrier pull resistor. U6 has a weak internal pull-up on STB, so while A19 is not driven (reset, boot, pin not configured) the transceiver stays in low-power standby: driver off, RXD high until a bus wake-up pattern. Drive CAN_STBY low from firmware for normal mode; do not rely on the internal pull-up. CANH (pin 7) and CANL (pin 6) leave through R247 / R248 0 Ω.



Module with its own CAN PHY: remove R34, R246, R247 and R248, then fit R249 and R250.

Figure 30 CAN transceiver U6 and the not-fitted PHY bypass R249 / R250 (simplified)

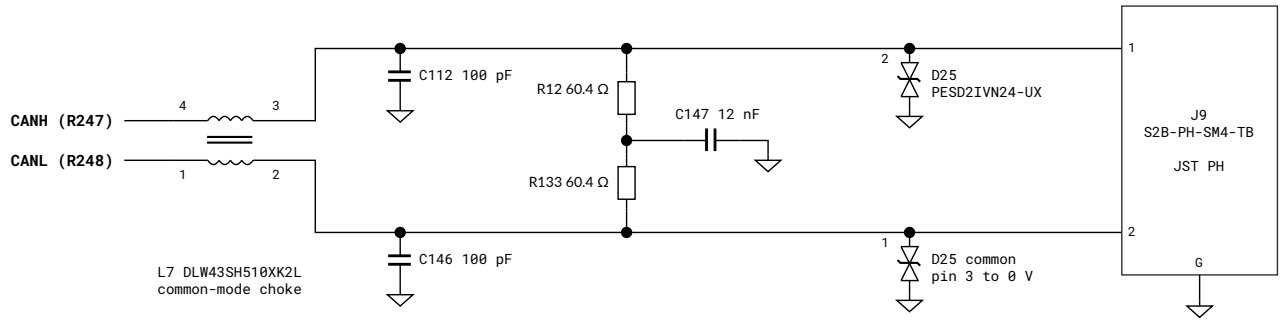
Warning: U6 is always fitted and its TXD / RXD connect to module pads B18 / B19 through 0 Ω resistors R34 / R246. A module with its own CAN PHY fitted drives bus-level CANH / CANL on those pads, which would reach U6 logic pins. For such a module remove R34, R246, R247 and R248, and fit R249 and R250 to connect the pads straight to the bus.

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9.2 Connector

J9 (S2B-PH-SM4-TB) is a 2-pin JST PH connector: pin 1 CANH, pin 2 CANL; its mounting tab G is on 0 V. Between R247 / R248 and J9 the bus passes common-mode choke L7 (DLW43SH510XK2L). On the connector side of L7 each line has 100 pF to 0 V (C112 on CANH, C146 on CANL), the split termination (R12 and R133, 60.4 Ω each, centre tap to 0 V through C147 12 nF) and the dual TVS D25 (PESD2IVN24-UX). The termination is always connected: terminate only the far end of the bus.

Warning: R12 and R133 are 0.1 W parts. A DC fault across the bus (for example CANH shorted to a 12 V supply) puts about 0.6 W in each and burns them. Protect the bus wiring against shorts to supply rails.



120 Ω split termination (R12 + R133) is always connected: there is no termination jumper.
Terminate the far end of the bus only.

Figure 31 CAN bus side: choke L7, split termination, TVS D25 and J9 (simplified)

Warning: The bus has a split 120 Ω termination (R12, R133 60.4 Ω each, with C147) that is **always connected**; there is no termination jumper. Do not add a second terminator at this end of the bus; a bus with more than two terminators has too low an impedance.

10 microSD and SDIO Muxing

10.1 microSD Socket

J7 (TF PUSH) is a push-push microSD socket. The data lines reach it from the module SDIO pads through side A of U38 / U39 (see SDIO Multiplexing); card detect and the card supply connect directly.

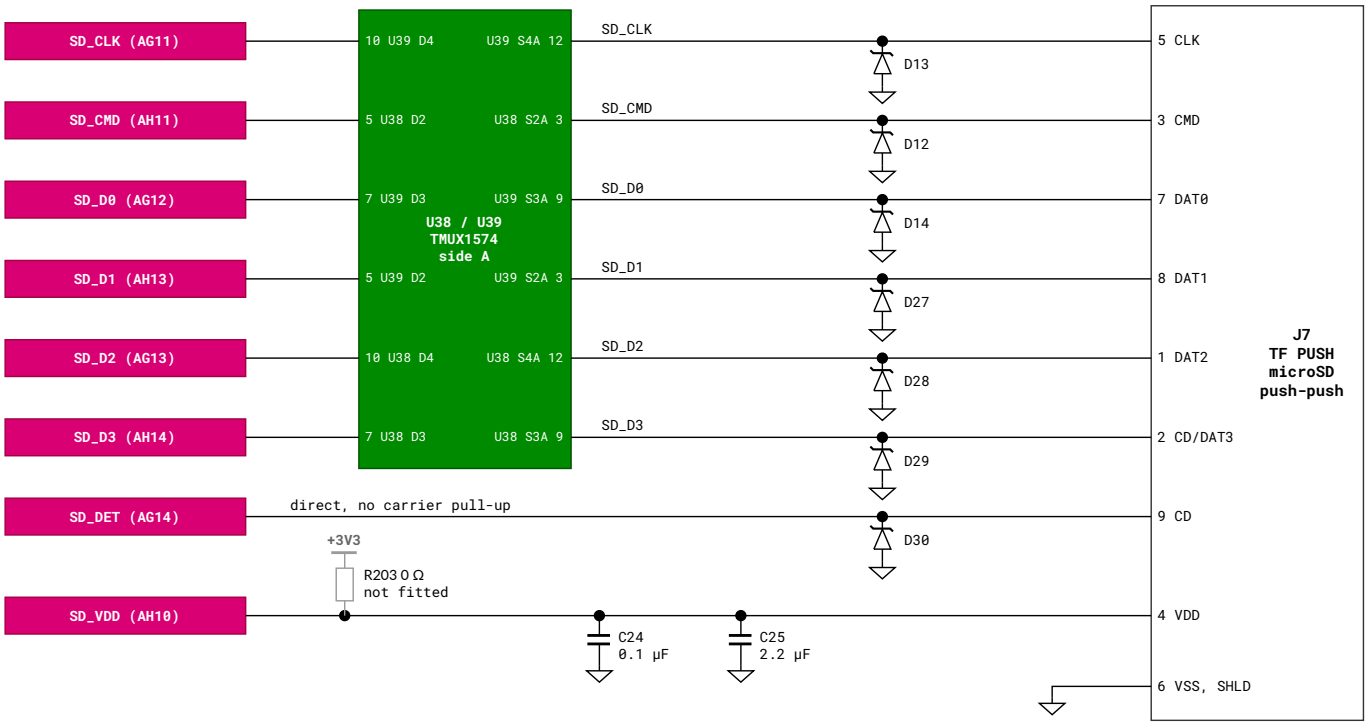
J7 pin	Net	Module pad	ESD
1 DAT2	SD_D2	AG13 (via U38)	D28
2 CD/DAT3	SD_D3	AH14 (via U38)	D29
3 CMD	SD_CMD	AH11 (via U38)	D12
4 VDD	SD_VDD	AH10	-
5 CLK	SD_CLK	AG11 (via U39)	D13
6 VSS	0 V	-	-
7 DAT0	SD_D0	AG12 (via U39)	D14
8 DAT1	SD_D1	AH13 (via U39)	D27
9 CD	SD_DET	AG14 (direct)	D30

Table 8 J7 microSD socket pinout

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The ESD diodes are ESD9101P2T5G, cathode on the line. The card supply SD_VDD is a module output (pad AH10) with C24 0.1 µF and C25 2.2 µF; R203 (0 Ω to +3V3) is not fitted. Do not fit R203 while a module drives AH10. There are no pull-ups on the SD lines or on SD_DET on the carrier: enable the module's internal pull-ups. SD_RST (AH12) reaches only U38 S1A, which is not connected, so it has no function on the microSD side.

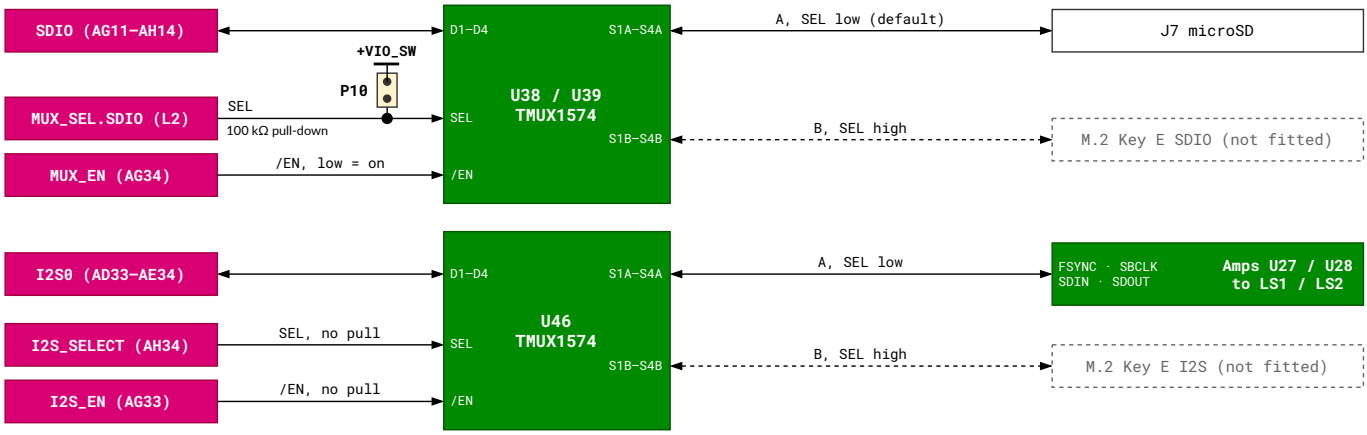
> **Note:** The data path through U38 / U39 needs MUX_EN (pad AG34, active low, no carrier pull resistor) driven low by the module. With MUX_EN high the switches are off and the card does not respond, even with MUX_SEL . SDIO at its default. Left floating, MUX_EN is held low only by the 6 MΩ internal pull-down, which nominally enables the switches but is not reliable: drive it low.



ESD diodes ESD9101P2T5G, cathode on the line. No pull-ups on the SD lines on the carrier.

Figure 32 microSD socket J7 with ESD, card detect and SD_VDD (simplified)

10.2 SDIO Multiplexing



MUX_EN, I2S_SELECT and I2S_EN have no carrier pull resistor: drive them low in board init.

Figure 33 SDIO mux U38 / U39 and I2S mux U46 (simplified)

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Two TMUX1574 muxes (U38 and U39) select the SD bus between the microSD socket (default) and the M.2 Key E SDIO nets (not fitted). The select line MUX_SEL.SDIO is on module pad L2 and the enable MUX_EN is on AG34. MUX_SEL.SDIO has a 100 kΩ pull-down to 0 V, so the default is the microSD socket. MUX_EN is active low and has no resistor on the carrier (only the mux's weak internal pull-down): drive it low in board init.

> **Tip:** The M.2 Key E slot is not fitted in this assembly, so leave SDIO routed to the microSD socket and leave P10 open. The enable line MUX_EN (and the audio I2S_SELECT, I2S_EN lines) have no pull resistor on the carrier: drive them from firmware.

11 Display (MIPI DSI)

- **J6:** 40-pin display connector; the sheet references the Rocktech RK055HDMIPI4MA0 panel (kernel compatible string rocktech,rk055hdmipi4ma0).
- MIPI DSI clock + 4 data lanes (pairs) are routed. E1M-AEN drives 2 lanes (lanes 0 and 1); lanes 2 and 3 stay unused.
- Supplies on J6: pin 25 +L_VIO (from P1), pin 30 +3V3, pins 39 and 40 +5V.
- Backlight: BL_LED_A and BL_LED_K come straight from module pads A31 and B31 to J6 pins 2 and 1; R9 (2.4 Ω) connects BL_LED_K to 0 V. BL_PWM (pin 34) is module pad A5 (CK_PWM4_L) through U4 (CK_PWM4_DISP on U4 B8) and R110 (0 Ω), pulled up to +L_VIO by R108 (4.7 kΩ). R109 (BL_LED_A to BL_PWM) is not fitted. Pad A5 also drives the Arduino CK_PWM4 through U18.
- Panel control: LCD_PWR_EN (module pad A10, R65 10 kΩ pull-down: panel power off by default) to pin 32; LCD_RST (B10, R83 100 kΩ pull-up to +VIO_SW) to pin 21.
- Touch: CTP_INT (AG18, R66 4.7 kΩ pull-up to +VIO_SW) from pin 29; CTP_RST (pin 28) has no pad of its own: it is LCD_RST through R3 (0 Ω), pulled up by R107 (100 kΩ to +VIO_SW), so the panel and touch resets move together. Touch and panel I2C: module I2C1 (pads AG17 SCL / AH17 SDA) to pins 27 / 26.
- The control, touch, I2C and BL_PWM signals pass through level shifter U4 (LSF0108, always enabled) to the panel I/O level +L_VIO, set by header P1 (1.8 V or 3.3 V). Panel-side pull-ups (R10, R11, R108, R166 to R169) go to +L_VIO.

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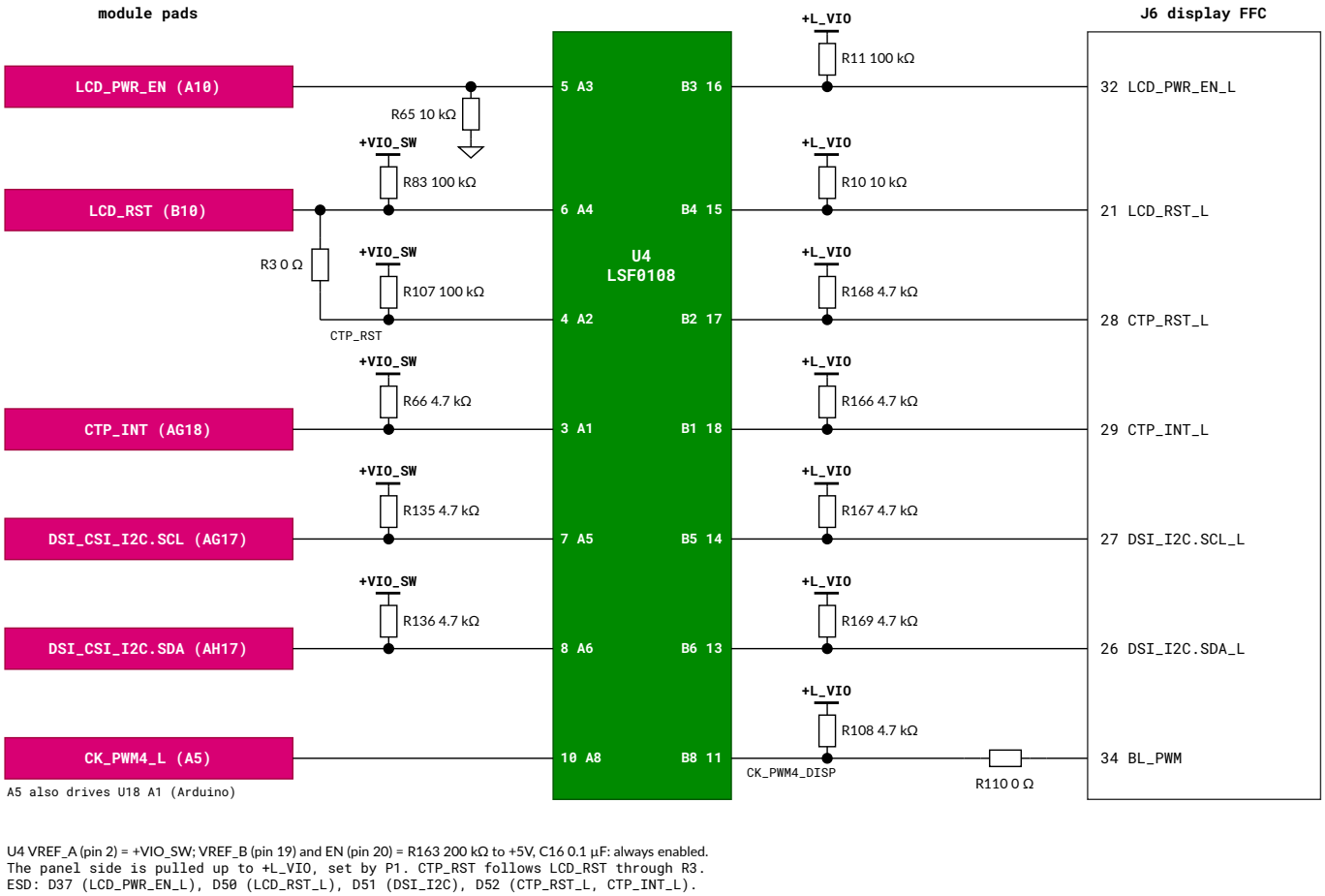


Figure 34 Display control and touch through level shifter U4, module-side pull resistors to +VIO_SW (R65 to 0 V) and panel-side pull-ups to +L_VIO (simplified from the 2641-R3 netlist)

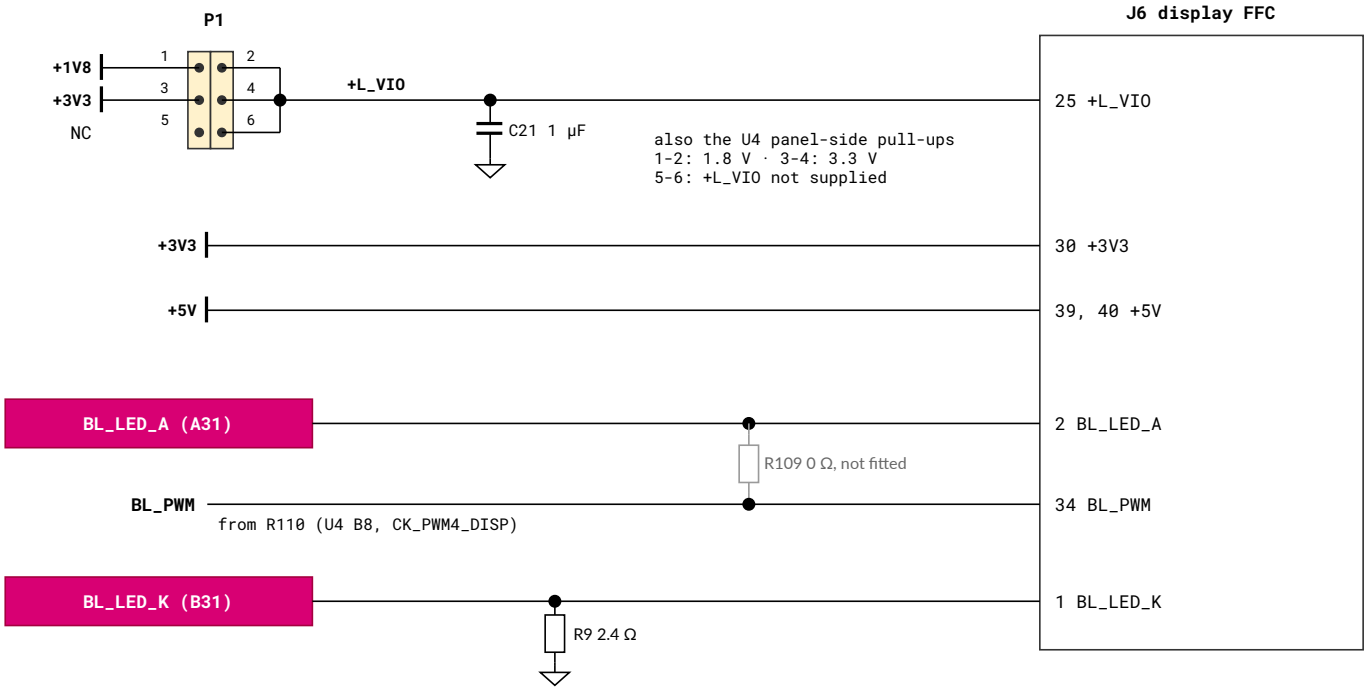


Figure 35 Display supplies (P1, +L_VIO) and backlight (simplified)

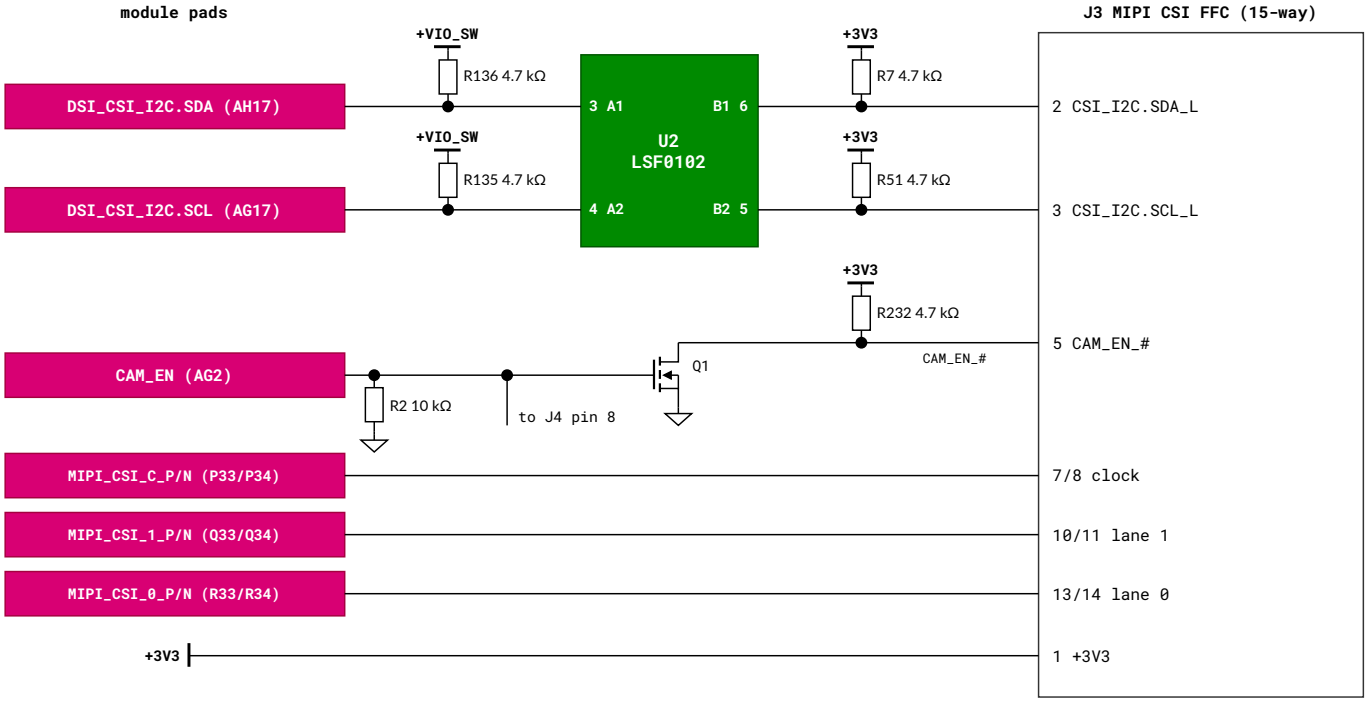
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Warning: Set P1 to the I/O level your panel needs before you connect it. A wrong level can damage the panel or the module.

12 Camera Interfaces

12.1 MIPI CSI Connector (J3)

J3: 15-way, 1.0 mm FFC connector with a MIPI CSI clock and two data lanes (module CSI0 pads P33 and P34 clock, Q33 and Q34 lane 1, R33 and R34 lane 0). Only two lanes are routed. Pin 1 is +3V3 (a plain rail: not switched, not monitored), pins 2 and 3 are the camera I2C (module I2C1 through level shifter U2, with 4.7 kΩ pull-ups to +3V3), pin 5 is CAM_EN_# (open drain from Q1, driven by module pad AG2). CAM_EN_# is pulled up to +3V3 (R232 4.7 kΩ) and AG2 has a 10 kΩ pull-down (R2), so by default pin 5 is high (camera enabled); driving AG2 high pulls pin 5 low and disables the camera. The same CAM_EN line also goes straight to J4 pin 8, so AG2 high also drives J4 pin 8 high. Pin 4 is not connected. Module CSI0 lanes 2 and 3 (N33/N34, 033/034) and all CSI1 pads are not connected. U2 is always enabled (R1 200 kΩ to +5V).



U2 REFA (pin 2) = +VIO_SW; REFB (pin 7) and EN (pin 8) = R1 200 kΩ to +5V, C4 0.1 µF: always enabled.
CAM_EN low (R2 default): Q1 off, J3 pin 5 high. CAM_EN high: J3 pin 5 low, J4 pin 8 high.
CSI0 lanes 2 and 3 (N33/N34, O33/O34) and all CSI1 pads are not connected. J3 pin 4 is not connected.
ESD: D47 (clock), D31 (lane 1), D42 (lane 0), D32 (I2C), D45 (CAM_EN_#).

Figure 36 MIPI CSI connector J3: camera I2C through U2, camera enable through Q1, two CSI0 lanes (simplified)

12.2 Parallel (DVP) Camera Connector (J4)

J4: 24-way, 0.5 mm FFC connector for a parallel 8-bit camera. Camera I2C is module I2C1 direct (pads AG17 / AH17, R135 / R136 4.7 kΩ pull-ups to +VIO_SW); the I/O supply on pin 11 is +VIO_SW. The same I2C1 bus (DSI_CSI_I2C.SDA / DSI_CSI_I2C.SCL) also reaches J3 through U2 and J6 through U4, so display, MIPI CSI and DVP devices share one bus: make sure their I2C addresses do not collide.

J4 pin	Net	Module pad	Note
1, 12, 14	–	–	not connected
2, 15	0 V	–	
3	DSI_CSI_I2C.SDA	AH17	I2C1 SDA

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J4 pin	Net	Module pad	Note
4	+2V6_CAM	–	via P15
5	DSI_CSI_I2C.SCL	AG17	I2C1 SCL
6	CAM_RST	AH18	R143 100 kΩ to +VIO_SW
7	CAM_VSYNC	S32	
8	CAM_EN	AG2	R2 10 kΩ to 0 V; also drives Q1 for J3
9	CAM_HSYNC	T32	
10	+1V2_CAM	–	via P14
11	+VIO_SW	–	
13	CAM_XVCLK	U32	
16	CAM_D0	AD32	module pad name CAM_D8
17	CAM_PCLK	V32	
18	CAM_D1	AC32	module pad name CAM_D7
19	CAM_D5	Y32	module pad name CAM_D3
20	CAM_D2	AB32	module pad name CAM_D6
21	CAM_D4	Z32	module pad name CAM_D4
22	CAM_D3	AA32	module pad name CAM_D5
23	CAM_D6	X32	module pad name CAM_D2
24	CAM_D7	W32	module pad name CAM_D1

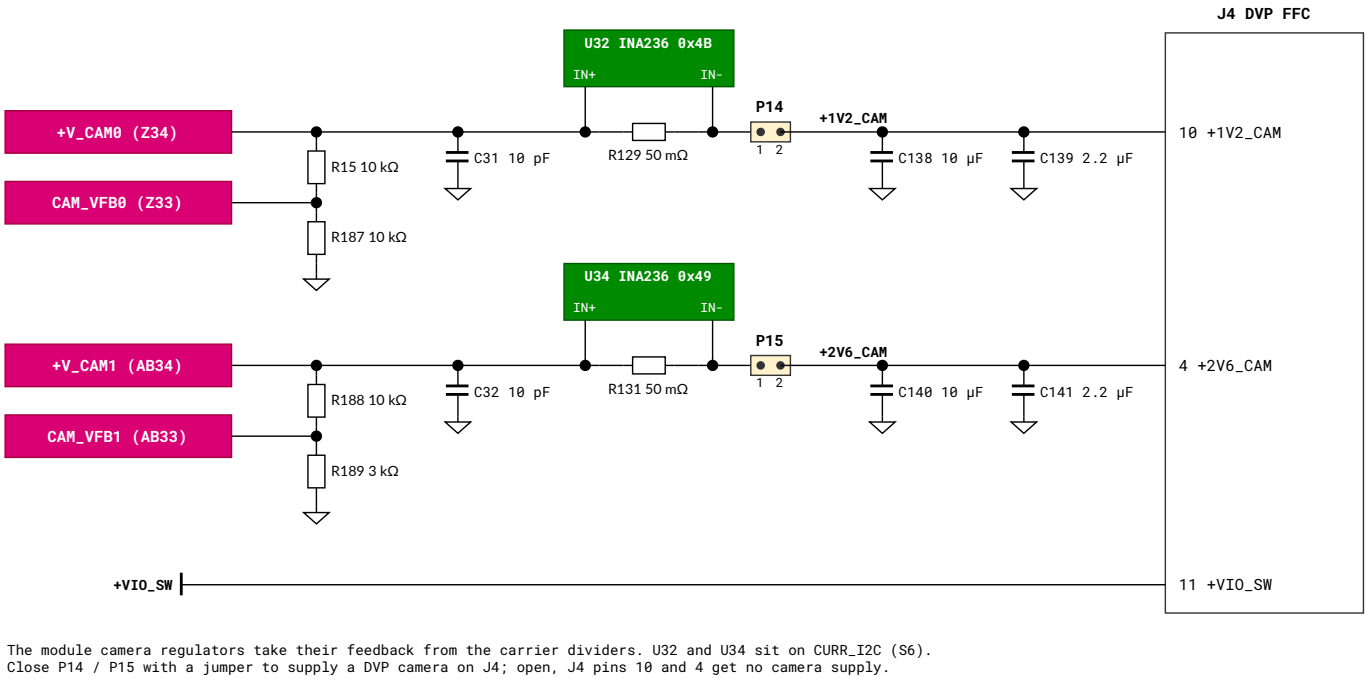
Table 9 J4 DVP camera connector pinout

The carrier net names of the data bus run in the opposite order to the module pad names: carrier CAM_D0 is module pad AD32 (CAM_D8) and carrier CAM_D7 is W32 (CAM_D1). Check the bit order against the module pinout before you configure the camera interface.

12.3 Camera Rails

The camera rails +1V2_CAM and +2V6_CAM come from two module outputs (+V_CAM0 on pad Z34 and +V_CAM1 on AB34). Feedback dividers on the carrier set their voltages: CAM_VFB0 (pad Z33) is R15 10 kΩ from +V_CAM0 over R187 10 kΩ to 0 V, and CAM_VFB1 (pad AB33) is R188 10 kΩ from +V_CAM1 over R189 3 kΩ to 0 V. Each rail reaches J4 through a 50 mΩ shunt (R129, R131, measured by INA236 U32 at 0x4B and U34 at 0x49 on CURR_I2C) and a jumper header (P14 to J4 pin 10, P15 to J4 pin 4). Close P14 / P15 with a jumper to supply a DVP camera on J4; with them open, J4 pins 10 and 4 get no camera supply.

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The module camera regulators take their feedback from the carrier dividers. U32 and U34 sit on CURR_I2C (S6).
Close P14 / P15 with a jumper to supply a DVP camera on J4; open, J4 pins 10 and 4 get no camera supply.

Figure 37 DVP camera supplies: feedback dividers, shunts and monitors, and jumpers P14 / P15 to J4 (simplified)

Warning: Do not hot-plug the camera FFCs. The +1V2_CAM and +2V6_CAM rails are set for the camera: check your camera's supply voltages against them before you connect it.

13 M.2 and PCIe (Not Fitted)

Not fitted on the E1M-AEN build The Alif Ensemble SoCs have no PCIe, so on the 2641-R3 E1M-AEN assembly the **M.2 card-edge connectors are not populated**: J16 (Key E), J23 (second M.2 slot), and the M.2 UART header J17. The PCIe lane switches (U42, U43, U50, U51), clock buffer (U44), I2C mux (U45), the I2C bridge U41 and the I/O expander U37 are not populated either. See Appendix B.

14 Audio

14.1 PDM Microphones

Four MSM261DHT006 PDM microphones are fitted: U19, U20, U25 and U26. All four are supplied from +VIO_SW (pin 1 VDD). They form two stereo pairs. Each microphone has its own 22 Ω series resistor on CLK (pin 3) and on OUTPUT (pin 4):

Ref	Clock	Data	L/R pin	Series R (clock / data)
U19	PDM_C0 (AA1)	PDM_D0 (AA2)	+VIO_SW	R70 / R69
U20	PDM_C0	PDM_D0	0 V	R71 / R72
U25	PDM_C1 (AB1)	PDM_D1 (AB2)	+VIO_SW	R113 / R115
U26	PDM_C1	PDM_D1	0 V	R114 / R116

Table 10 PDM microphones

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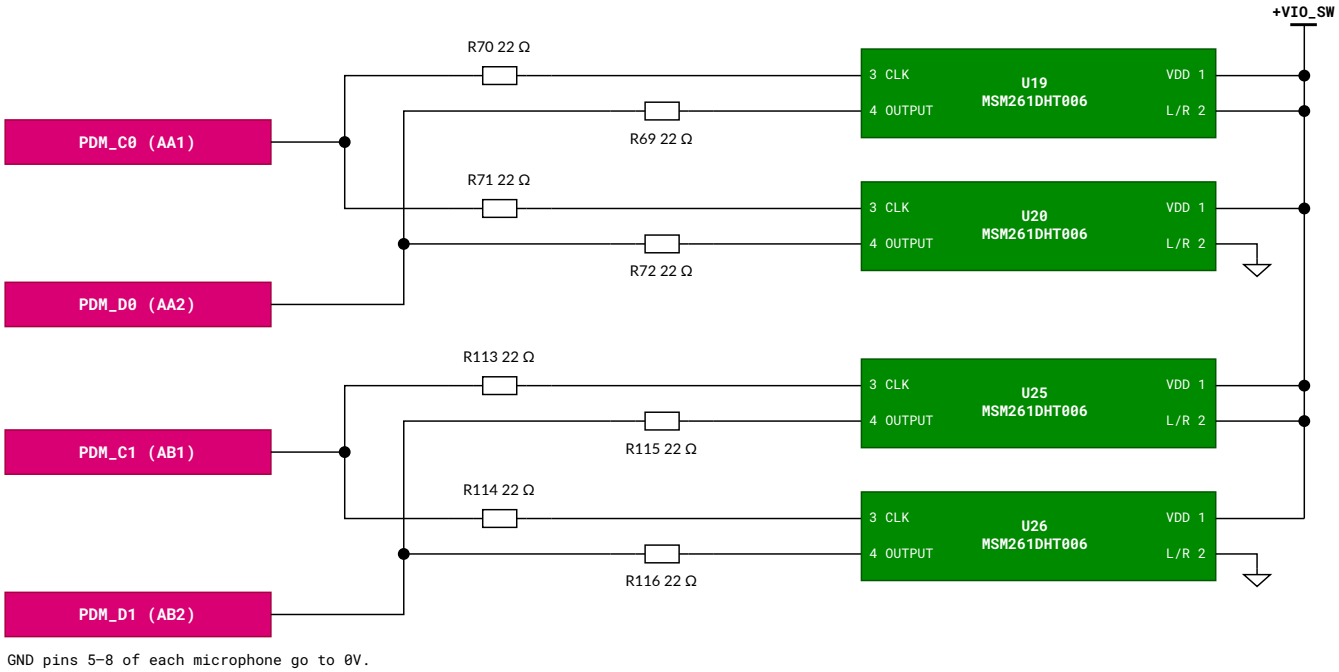


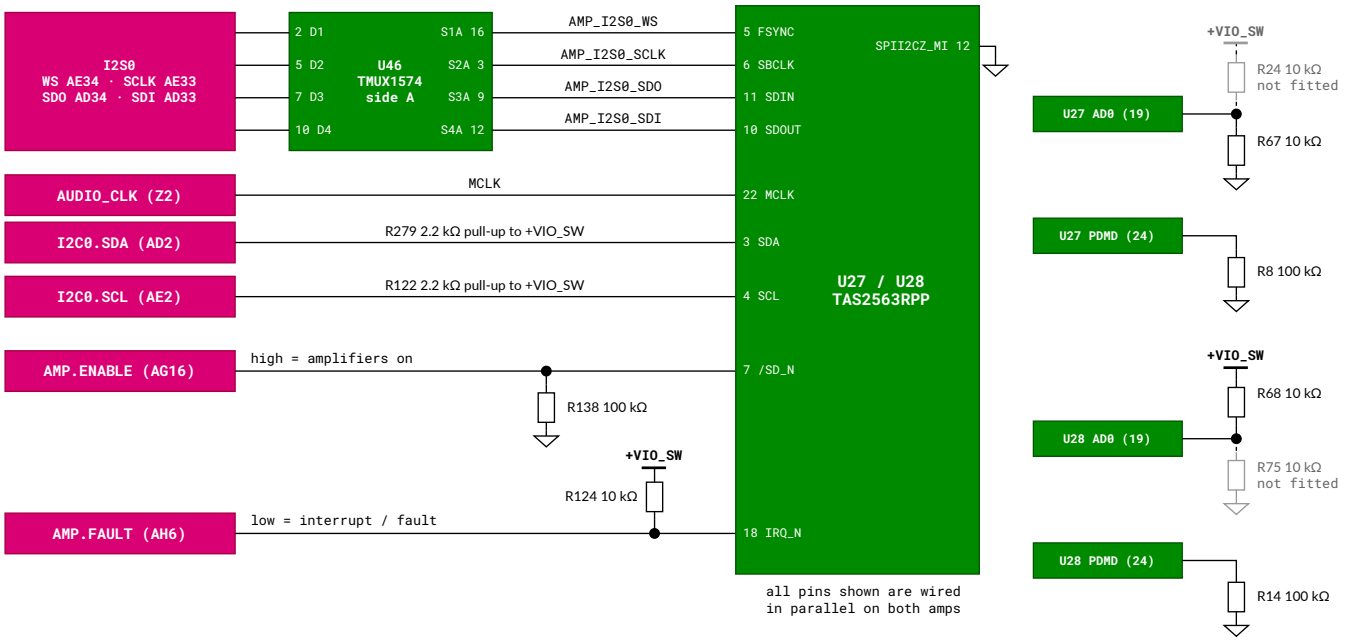
Figure 38 PDM microphones: two stereo pairs (U19/U20 on PDM_C0/PDM_D0, U25/U26 on PDM_C1/PDM_D1) with 22 Ω series resistors, L/R straps and the +VIO_SW supply

Each pair shares one clock and one data line. L/R is high on U19 and U25 (data driven after the rising CLK edge, latched by the module on the falling edge) and low on U20 and U26 (driven after the falling edge, latched on the rising edge), so the two microphones of a pair drive the shared data line on opposite clock edges.

14.2 Amplifiers and Speakers

- **U27 (left) and U28 (right):** TAS2563RPP Class-D smart-amp ICs on the module I2C0 bus (I2C0.SDA AD2 / I2C0.SCL AE2, pull-ups R279 / R122 2.2 kΩ to +VIO_SW). Supplies: VBAT = +5V, VDD = +1V8, IOVDD = +VIO_SW. The boost inductor is L5 / L6 1 µH from +5V; VBST / PVDD have 2 × 10 µF each (C83, C207 / C92, C208).
- **Clocks and data:** MCLK (pin 22) of both amplifiers is AUDIO_CLK (module pad Z2). FSYNC, SBCLK, SDIN and SDOUT of both are wired in parallel to U46 side A (AMP_I2S0_WS, AMP_I2S0_SCLK, AMP_I2S0_SDO, AMP_I2S0_SDI).
- **I2C address straps (AD0, pin 19, a four-level input):** U27 has R67 10 kΩ to 0 V (R24 to +VIO_SW not fitted), so it answers at 0x4D; U28 has R68 10 kΩ to +VIO_SW (R75 to 0 V not fitted), so it answers at 0x4E. Both also answer at the global address 0x48. PDMD (pin 24, the unused PDM data input, not an address pin) has 100 kΩ to 0 V on both (R8, R14); SPII2CZ_MI (pin 12) is tied to 0 V, which selects I2C mode.
- Two on-board 8 Ω, 700 mW speakers LS1 (left) and LS2 (right), both KLJ-01304T-08R07W, are fitted. Each is connected through two 0 Ω links (R234 / R233 for LEFT_P / LEFT_N, R236 / R235 for RIGHT_P / RIGHT_N). The external speaker connectors J14 (left) and J21 (right), both S2B-PH-SM4-TB, and the output EMI parts (C93 to C100 2.2 nF, R73, R74, R76, R123 68 Ω) are not fitted. To use an external speaker, fit J14 / J21 (pin 2 = _P, pin 1 = _N, G pads to 0 V) and remove the 0 Ω links to disconnect the on-board speaker.
- Control: AMP.ENABLE (module pad AG16) drives SD_N (pin 7) of both amplifiers and has R138 100 kΩ to 0 V, so the amplifiers are off by default. AMP.FAULT (module pad AH6, the module's I2S1_SDI pad) is the IRQ_N (pin 18) of both amplifiers tied together, pulled up by R124 10 kΩ to +VIO_SW; a low level means one of the amplifiers is signalling.
- Pulling AMP.ENABLE low puts both amplifiers in hardware shutdown, which clears all their registers: reload the full configuration after every enable. Keep AMP.ENABLE low until +VIO_SW has settled.

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The I2C0 bus is shared with the current monitors (via S6) and the RP2040 (via U58). U46 is shown on side A: I2S_SELECT low, I2S_EN low.

Figure 39 Amplifier control and data (simplified): I2S0 through U46 side A, AUDIO_CLK (MCLK), I2C0, AMP.ENABLE with R138 pull-down, shared AMP.FAULT with R124 pull-up, and the AD0 and PDMD straps for each amplifier

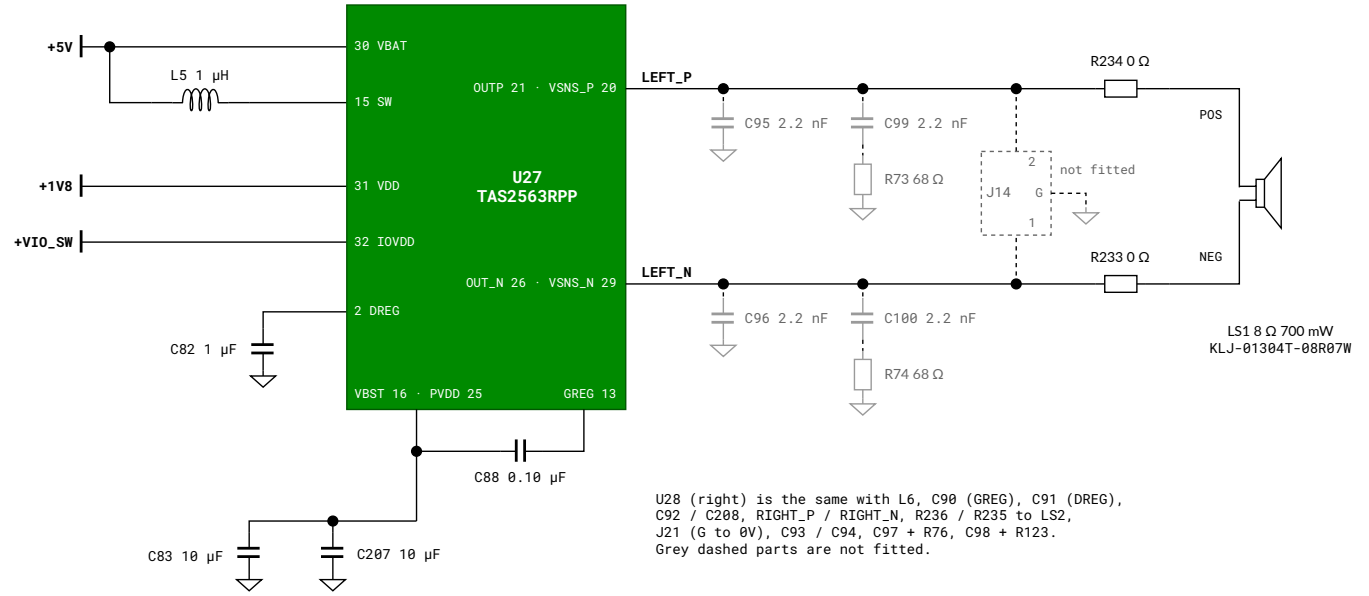


Figure 40 Left channel, U27 to LS1: supplies, boost inductor L5, regulator capacitors and 0 Ω links to the speaker. The connector J14 and the EMI parts are not fitted (grey, dashed). U28 / LS2 is the same, with the designators listed in the figure

14.3 I2S Routing

U46 (TMUX1574RSVR, supplied from +VIO_SW) switches module I2S0 (I2S0_WS AE34, I2S0_SCLK AE33, I2S0_SDO AD34, I2S0_SDI AD33) between the amplifiers and the M.2 slot. Control nets: I2S_EN (module pad AG33) and I2S_SELECT (AH34). Side A connects the module to the amplifiers; side B goes to the M.2 slot (not fitted). Neither control line has a pull resistor on the carrier: drive I2S_EN low (enable) and I2S_SELECT low (amplifiers) before starting audio.

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15 Expansion and User Interface

15.1 Arduino / mikroBUS

Arduino headers P3 to P6 and mikroBUS headers P7, P8 are fitted. Four LSF pass-gate translators link the module pads (at +VIO_SW) to the headers (at +VARD, selected with P9). Set +VARD equal to or higher than +VIO_SW: the LSF parts need VREF_A (+VIO_SW) to be the lowest voltage on any of their pins. With a 3.3 V module and P9 at 1.8 V the lines are not translated down and the shield sees 3.3 V. The same rule applies to P1 (+L_VIO) for the display shifter U4.

- **U40 (LSF0108RKSR), always on:** SPI0 (CK_MOSI, CK_MISO, CK_CS, CK_SCK), UART1 (CK_TXD, CK_RXD), CK_PWM0 and CK_INT.
- **U16 (LSF0102DQER), always on:** CK_SCL / CK_SDA from the I3C pads AG5 / AH5, with 4.7 kΩ pull-ups on both sides (R171 / R170 to +VIO_SW, R146 / R147 to +VARD).
- **U17 (LSF0102DQER), always on:** CK_RST from pad AH7; its second channel is unused.
- **U18 (LSF0108RKSR), off by default:** DIO1 to DIO4 and PWM1 to PWM4, see below.

"Always on" means EN and VREF_B are pulled to +5V through 200 kΩ (R176, R173, R174). Every header-side line has a 10 kΩ pull-up to +VARD (4.7 kΩ on CK_SCL / CK_SDA; CK_INT has two 10 kΩ in parallel, R267 and R268).

Only P3 pin 2 (IOREF) follows P9. The supply pins are fixed: P3 pin 4 and P7 pin 7 are +3V3, P3 pin 5 and P8 pin 7 are +5V. P5 pin 3 (AREF) and P3 pins 1 and 8 are not connected.

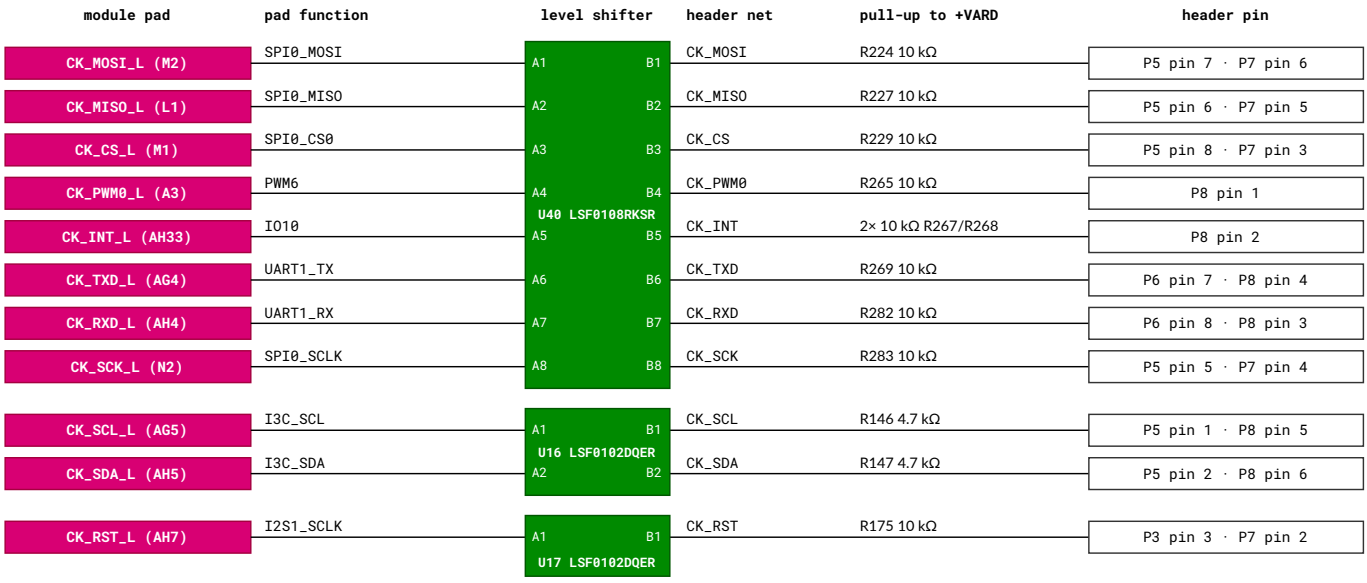
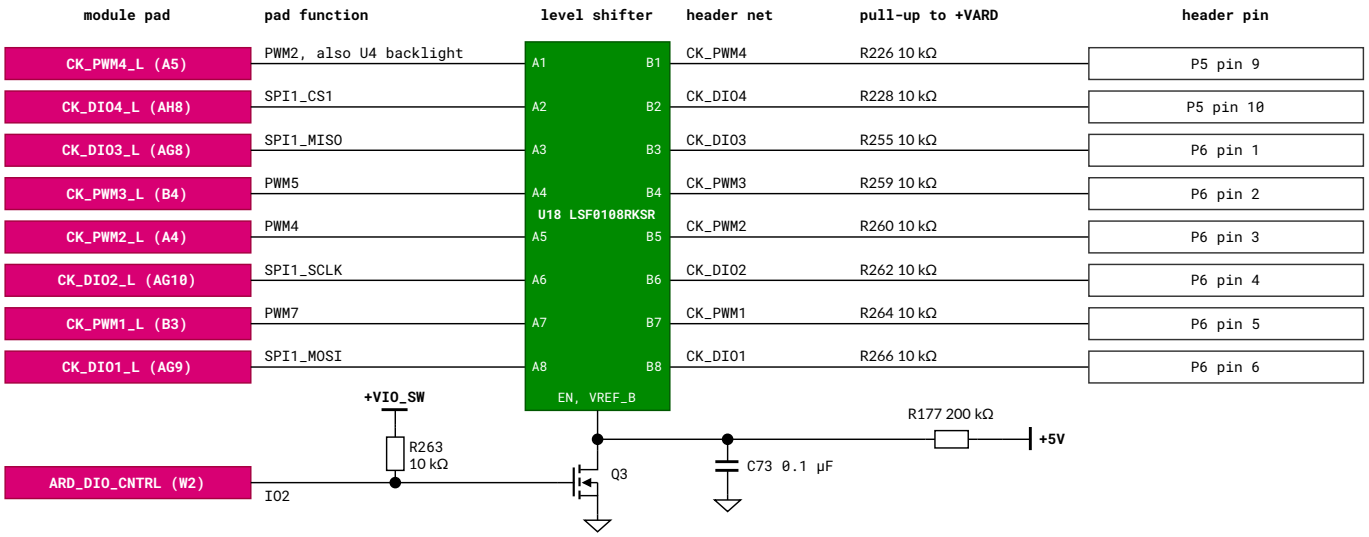


Figure 41 Arduino / mikroBUS lines behind the always-on translators U40, U16 and U17 (simplified)

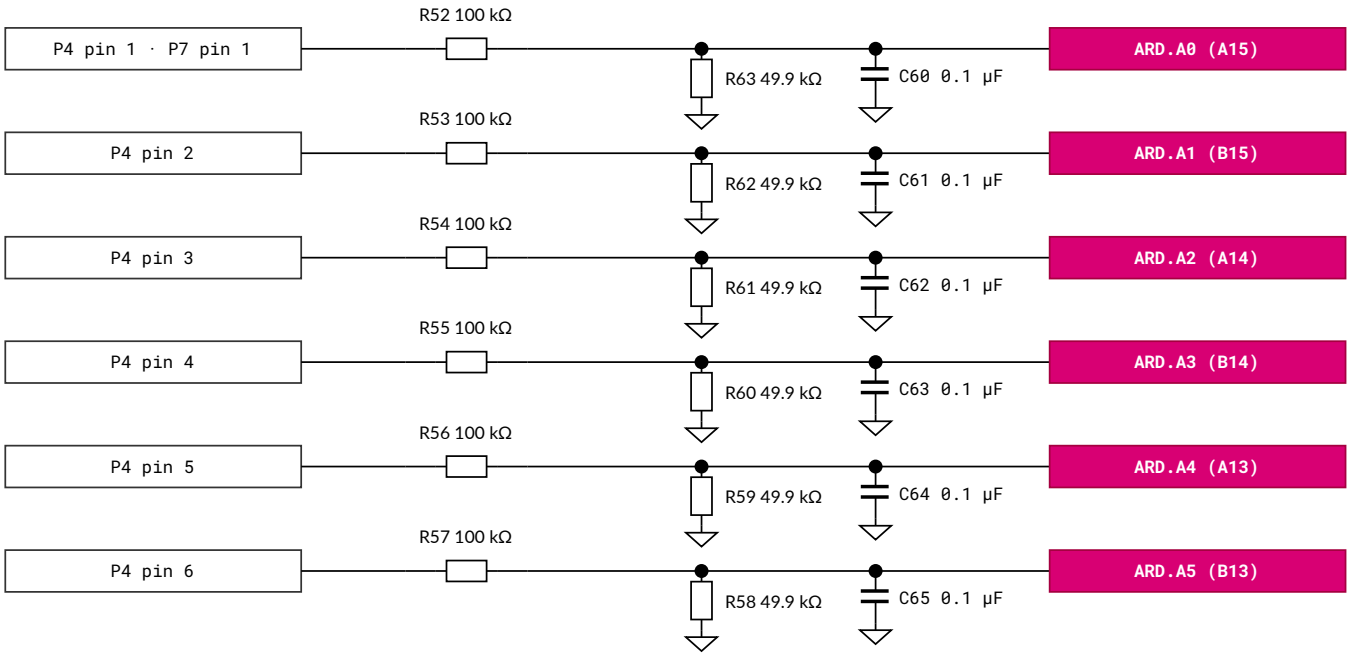
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W2 high or open (default): Q3 on, EN low, U18 off and the header lines are cut off from the module.
W2 driven low: Q3 off, R177 pulls EN up, U18 on. Drive W2 low in board init to use DIO1–DIO4 and PWM1–PWM4.
CK_PWM4_L (A5) is also the display backlight PWM (U4 to CK_PWM4_DISP), whatever the state of U18.

Figure 42 Arduino digital bank U18: off until ARD_DIO_CNTRL (W2) is driven low (simplified)

The analog inputs A0 to A5 (P4) have no translator. Each has a 100 kΩ series resistor and 49.9 kΩ plus 0.1 µF to 0 V at the module pad, so the pad sees the header voltage times 0.333 (5 V gives about 1.67 V). The input resistance is 149.9 kΩ and the filter corner is about 48 Hz. A0 (CK_ANA) is also the mikroBUS AN pin, P7 pin 1.



P4 pin 1 carries CK_ANA, shared with mikroBUS AN (P7 pin 1). No level shifter: these are plain analog paths.
Pad voltage = header voltage × 49.9 / 149.9 (0.333). Input resistance 149.9 kΩ; RC corner about 48 Hz.

Figure 43 Arduino analog inputs P4: 100 kΩ series, 49.9 kΩ + 0.1 µF to 0 V at the module pad

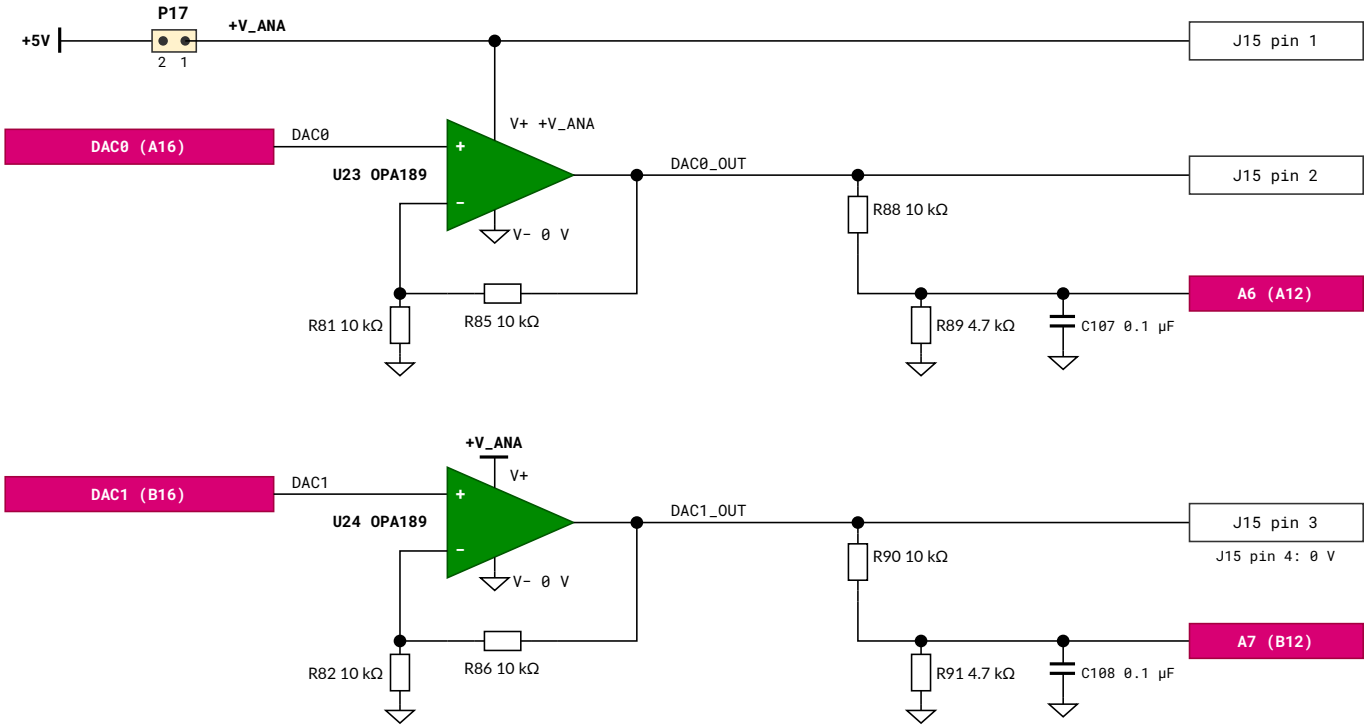
Important: Decide your +VARD level (P9) before attaching external shields or click boards: an over-voltage on IO can damage attached peripherals.

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> **Note:** The Arduino digital bank behind U18 (DIO1 to DIO4, PWM1 to PWM4) is **disabled by default**. ARD_DIO_CNTRL (module pad W2) has a 10 kΩ pull-up to +VIO_SW (R263) and drives the gate of Q3, which holds the U18 enable low. Drive W2 low in board init to enable the bank. CK_PWM4 shares module pad A5 with the display backlight PWM, which stays connected through U4 whatever the state of U18.

15.2 Other Headers

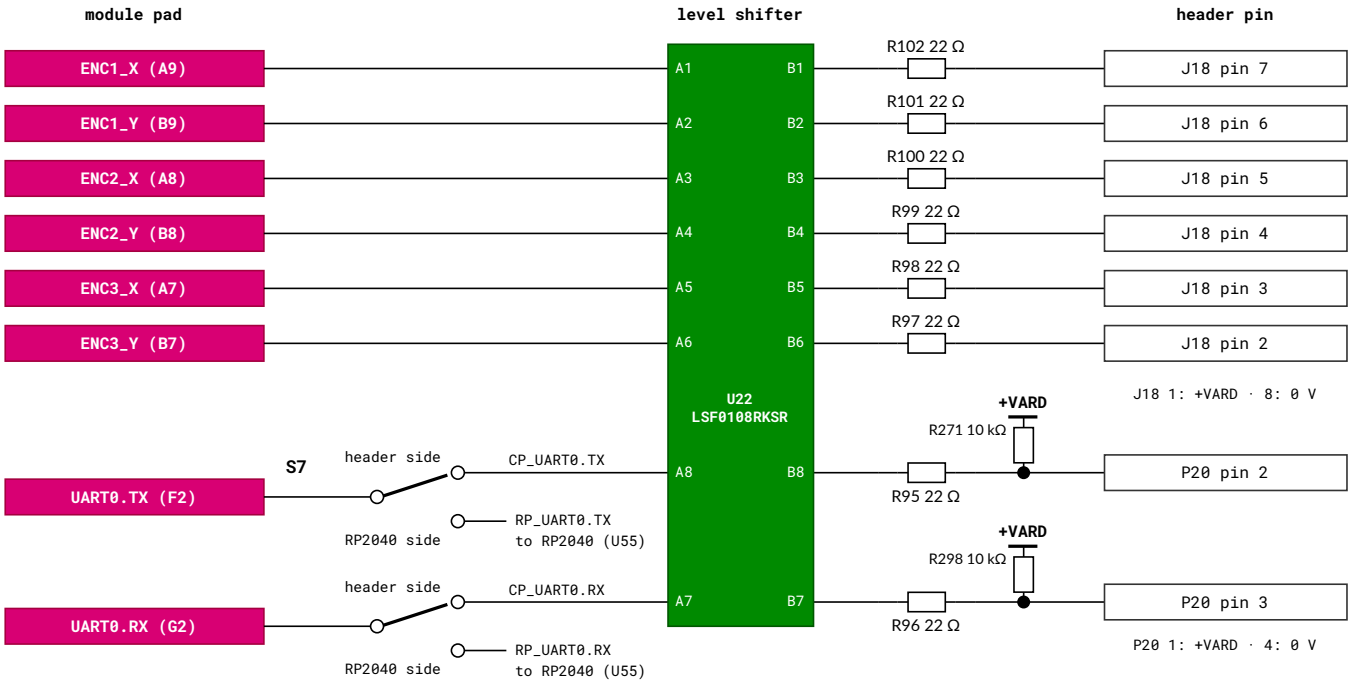
- **J15:** DAC outputs, 4-pin: 1 +V_ANA, 2 DAC0_OUT, 3 DAC1_OUT, 4 0 V. Module pads DAC0 (A16) and DAC1 (B16) are buffered by two OPA189 op-amps, U23 and U24, non-inverting with gain 2 (10 kΩ / 10 kΩ), powered from +V_ANA. Fit P17 to supply +V_ANA from +5V. Each output is also divided by 10 kΩ / 4.7 kΩ (times 0.320) to the module ADC pads A6 (A12) and A7 (B12), so firmware can read back what it drives.
- **J18:** 8-pin encoder header: 1 +VARD, 2 ENC3_Y, 3 ENC3_X, 4 ENC2_Y, 5 ENC2_X, 6 ENC1_Y, 7 ENC1_X, 8 0 V. Each line goes through a 22 Ω resistor and the always-on translator U22 (LSF0108RKSR) to module pads A9 / B9 (ENC1), A8 / B8 (ENC2) and A7 / B7 (ENC3). There is no pull-up on these lines: an open-collector encoder needs its own pull-ups to +VARD.
- **P20:** 4-pin UART header: 1 +VARD, 2 TX (module output), 3 RX, 4 0 V, through 22 Ω resistors (R95, R96), 10 kΩ pull-ups to +VARD (R271, R298), U22 and slide switch S7. In the other position S7 connects the module UART0 to the RP2040 (U55).



Gain 2 (1 + 10 kΩ / 10 kΩ). Fit P17 to power the buffers; with P17 open +V_ANA and J15 pin 1 are unpowered.
Readback: pad voltage = DAC_OUT × 4.7 / 14.7 (0.320); read A6 / A7 with the module ADC to check the output.

Figure 44 DAC outputs on J15: OPA189 buffers U23 / U24 (gain 2) on +V_ANA from P17, with readback dividers to A6 / A7 (simplified)

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U22 is always on: EN = VREF_B pulled to +5V by R178 200 kΩ. Module side at +VIO_SW, header side at +VARD (P9).
The encoder lines have no pull-up on the carrier: open-collector encoders need their own pull-ups to +VARD.

Figure 45 Encoder header J18 and UART header P20 behind U22; P20 is reached only in the header position of S7 (simplified)

15.3 UART0 Console Routing

Slide switch S7 connects module UART0 either to the RP2040 (GPIO0 / GPIO1) or to header P20. There is no RS-232 transceiver and no RS-232 connector on the EVK.

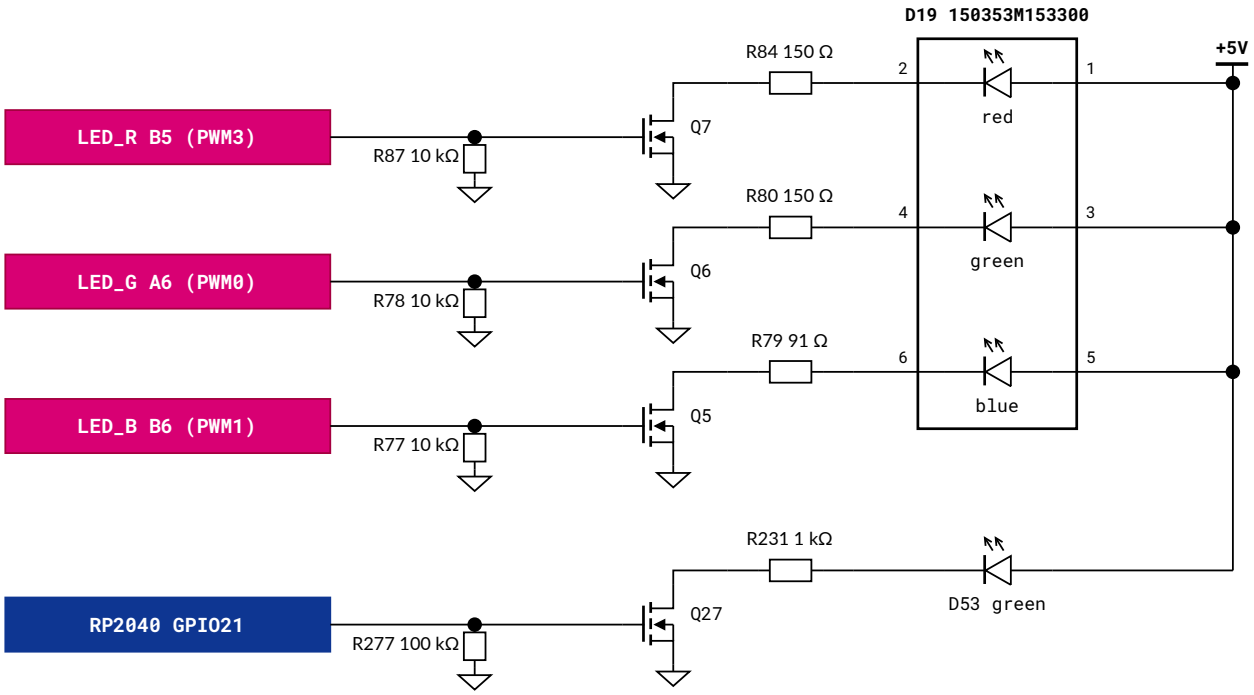
15.4 LEDs

15.4.1 User LEDs

The EVK has two user LEDs. Each is switched on the low side by an N-FET with a gate pull-down, so it is off until its control line is driven high.

- **D19, RGB:** red from module pad B5 (PWM3), green from A6 (PWM0), blue from B6 (PWM1). Drive the pads with PWM to set the colour and brightness. Series resistors: R84 150 Ω (red), R80 150 Ω (green), R79 91 Ω (blue).
- **D53, green:** the RP2040 status LED on GPIO21, with R231 1 kΩ in series.

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A high level on the source switches its LED on (low-side N-FET); drive the module pads with PWM to set brightness and colour. With the line low or floating the LED is off (gate pull-down).

Figure 46 User LEDs: D19 RGB from module PWM pads and D53 from the RP2040 (simplified)

15.4.2 Indicator LEDs

Ref	Indicates
D8, D9	Red: USB1_VBUS, USB2_VBUS
D10	Red: USB_HOST_VBUS
D18	Green: 5V_PG
D15	Yellow: 3V3_PG
D16	Yellow: 1V8_PG
D17	Yellow: VIO_PG (+VIO_SW)
D19	RGB LED driven by module pads B5 (red), A6 (green), B6 (blue)
D53	Green status LED driven by RP2040 GPIO21

Table 11 LEDs

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16 I2C Bus Map

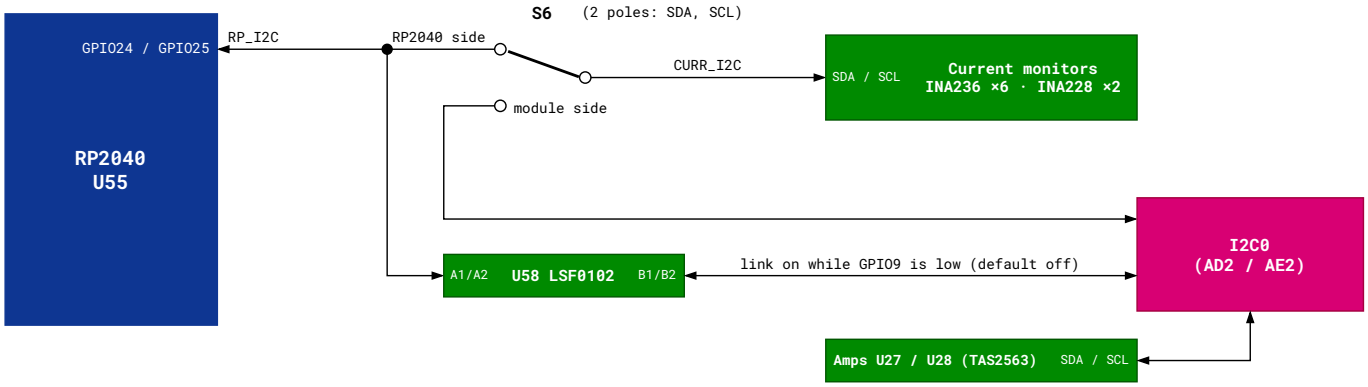


Figure 47 I2C routing: monitor switch S6 and RP2040 link U58 (simplified)

Bus	Description	Devices on the carrier
I2C0 (module pads AD2 SDA, AE2 SCL)	1.8 V (+VIO_SW), 2.2 kΩ pull-ups	Two TAS2563 amplifiers (U27, U28). With S6 on the module side the whole CURR_I2C bus joins here (eight monitors below). The RP2040 RP_I2C bus joins through U58 when GPIO9 is driven low.
CURR_I2C	Selected by slide switch S6: RP2040 I2C0 (GPIO24 / GPIO25) or module I2C0	INA236 U21 0x40, U31 0x41, U33 0x42, U34 0x49, U30 0x4A, U32 0x4B; INA228 U29 0x43, U53 0x47.
RP_I2C	RP2040 I2C0, 1.8 V (+1V8), 2.2 kΩ pull-ups	The CURR_I2C monitors (S6 on the RP2040 side); the module I2C0 through U58 (disabled by default).
RP2040 I2C1 (GPIO2 / GPIO3)	Through level shifter U14 to module pads V3 (SDA) and U3 (SCL)	No carrier devices.
Camera / display I2C (module I2C1: AH17 SDA, AG17 SCL)	1.8 V (+VIO_SW), 4.7 kΩ pull-ups	No carrier chip: J4 direct, J3 through U2, J6 through U4. Addresses belong to the attached camera or panel.
Arduino I2C (module I3C pads AH5 SDA, AG5 SCL)	Level shifter U16; 1.8 V (+VIO_SW) side	No carrier chip: pins on P5 and P8.

Table 12 I2C buses

All eight monitors have different addresses (0x40, 0x41, 0x42, 0x43, 0x47, 0x49, 0x4A, 0x4B).

17 Recommended Bring-Up Checklist

> **Note:** This is recommended engineering practice, not a verbatim procedure from the schematic.

1. **Visual inspection:** check for solder bridges around the module footprint and fine-pitch camera / display FFCs.
2. **Power-only test (no peripherals):**
   - Apply the barrel input at 9 V to 15 V, or a USB-PD source on J5 that offers 3 A at 9 V to 20 V.
   - Verify the power-good LEDs: D18 (5V_PG), D15 (3V3_PG), D16 (1V8_PG); D17 (VIO_PG) lights when the module has started and enabled +VIO_SW.
3. **Module enable:** ensure P11 (MODULE_EN) and P12 (MODULE_STBY) have no jumper fitted, and the RP2040 is not driving GPIO23 or GPIO22 high.

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4. **Boot configuration:** on E1M-AEN the BOOT pads are not connected and SW1 is not fitted.
5. **Debug access:** connect to J2 (SWD/JTAG) and confirm the IO reference voltage (+VIO_SW on pin 1).
6. **Check the jumpers:** P1, P9 and P16 set as intended, P10 open, P21 open.
7. **Add peripherals one at a time:** Ethernet, microSD, then display / camera.

18 Cautions Summary

- P11 or P12 fitted: the module is held off or in standby.
- P10 fitted on E1M-AEN: the SD bus is switched to the M.2 side, which is not fitted, and microSD stops working.
- P21 closed with a coin cell fitted or the trickle charger on: charges a primary lithium cell.
- P19 pin 6 is the carrier +1V8, not a module supply.
- P1 and P9 set for a level the connected device cannot take.
- A host on J12 or J13 drives 5 V into the module VBUS pads.
- Display, camera: no hot-plug.

Appendix A: Interface Quick Reference

Block	What's on the board
Power	Barrel J10 (9 V or higher, 15 V maximum), USB-PD J5, two eFuses, +5V / +3V3 / +1V8 / +VIO_SW rails, PG LEDs, +S_CAP supercap C38
USB	USB-C J12, J13, USB-A host J11, two TMUXHS221 data muxes, host-ID jumper P2
Ethernet	2 RJ45 MagJack J8, J20 (HR851178A); E1M-AEN uses J8 only (100 Mbit)
CAN	TCAN1044AV transceiver U6, connector J9
Storage	microSD J7, TMUX1574 SDIO muxes
Display	40-pin MIPI-DSI J6 (RK055HDMIPI4MA0), touch RST/INT
Camera	15-pin MIPI CSI J3, 24-pin DVP J4, camera rails
Audio	4 PDM microphones (MSM261DHT006), 2 TAS2563, 2 on-board speakers, I2S mux U46
Debug	RP2040 probe U55, J2 SWD/JTAG, P19, reset S1, module enable P11, standby P12
Antenna	On-board chip antenna A1 (default); U.FL J1 after fitting R111 and removing R132
Expansion	Arduino plus mikroBUS, I/O level select P9, DAC J15, encoder J18, UART P20
Profiling	6 INA236 and 2 INA228 monitors with shunts and fixed I2C addresses
Not fitted	M.2 slots and PCIe path, IO expander, external speaker connectors, SW1, P13, P18, BT1 (see Appendix B)

Table 13 EVK interface summary

Appendix B: Assembly Variant — E1M-AEN (Alif) Build

The E1M EVK carrier is laid out to the full E1M standard (superset) pinout. When assembled for an **E1M-AEN** (Alif Ensemble) module, the features that the SoM does not expose are left unpopulated. The list below is taken from the **2641-R3** BOM (68 not-populated designators), plus BT1, D11 and R126, which are unfitted +S_CAP options; footprints remain on the PCB so the same carrier can be rebuilt for other E1M variants.

Designator(s)	Function	Reason not fitted
J16, J23, J17	M.2 slots (Key E and a second slot) and M.2 UART header	Alif Ensemble has no PCIe; the M.2 slots are unused.

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Designator(s)	Function	Reason not fitted
U42, U43, U50, U51, U44, U45, U49, U41, U37, R154, R155, R160, R161, R162, R179, R180, R181, C161	PCIe lane switches, clock buffer, I2C mux and bridge, TCAL9538 IO expander and their pull-ups	Support the unfitted M.2 slots.
C93–C100, R73, R74, R76, R123, J14, J21	External speaker connectors and their EMI parts	The on-board speakers LS1, LS2 are used.
SW1, S4, S5, R93, R94, R105, R106	BOOT0 to BOOT3 DIP switch and pull options	BOOT pads are not connected on E1M-AEN.
P13, P18	Module debug UART header; RP2040 SWD header	Not used on this build.
J26	RSVD pad header	Not used on this build.
L4, R111	R111: 0 Ω link from the module antenna pad (ANT, AH1) to the U.FL J1; L4: 22 nH shunt at the on-board antenna	The AEN build feeds the module RF output to the on-board chip antenna (A1, Ignion NN02-201) through R132, L2, L3; J1 is not connected. To use an external antenna on J1, fit R111 and remove R132.
D54, R50, R49, R103, R112, R145	USB-PD controller option parts	Build-time options left open.
R24, R75	TAS2563 address strap options	Build-time options left open.
R109, R203, R223, R249, R250	Backlight, SD_VDD, +S_CAP tie-to-0 V and CAN options	Build-time options left open.
BT1, D11, R126	Coin-cell holder, and external RTC charger diode and resistor, for +S_CAP	Unfitted +S_CAP options: the 47 mF supercapacitor C38 is the fitted backup store. Fit exactly one store.
C68, C118, C144, C145, C154, C155, C160, C169	Optional 0.1 µ F decoupling	Build-time options left open.

Table 14 Not-populated components — 2641-R3 (E1M-AEN) build

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