ALP LAB

E1M-X Development Board

User Guide

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Release History

Revision	Changes	Date
0.1	• Initial draft. • Structural mirror of UG-E1M-001 with V2N / V2N-M1 specifics; TBD callouts for carrier-board details pending authoritative HW writeup.	May 2026
0.2	• Safety & Handling: removed the “S-grade” module nomenclature from the max ambient operating temperature (single +85 °C spec).	July 2026
0.3	• Re-verified against the E1M-X EVK board data in Alp SDK™ v0.17.0. • Current Measurement: the monitor addresses are no longer TBD — three INA236 (`0x40`, `0x41`, `0x49`) plus an INA228 +5V input monitor (`0x42`); the +VCAM2 monitor is not fitted and `0x48` is reserved as the TAS2563 shared address. • Sensors: replaced the BME688 / AS7341 / ICM-42688-P / TMP117 table with the populated ICM-42670-P, BMI323 and BMP581, and added the `alp_i2c0` address map. • I/O expanders are TI TCAL9538 (`0x73` main, `0x71` PCIe), not TCA9554; DX-M1 PCIe routing is on-module. • Audio: two TI TAS2563 smart amplifiers on `I2S0`, not a TAS5825M; no codec fitted. • Display: Display 2 (`DSI1`) is unavailable with V2N / V2N-M1 SoMs; the IT6162 HDMI bridge and the PI3WVR648 lane mux are not populated. • `alp_i2c1` reaches the expansion header only; the mikroBUS I²C is not wired to the SoM on the X-EVK V2. • Bring-up checklist: SCIF download is no longer described as the re-flash mode (the SDK writes the Cortex-M33 image from the running Linux system). • Secondary rails: the primary PMIC is the Qorvo ACT88760. • Replaced the private `alp-product-docs` issue-tracker link with the Alp Lab Community forum.	October 2026
0.4	• Power: the optional +S_CAP backup element is described generically, and a warning was added never to enable the RTC trickle charger with a primary lithium coin cell fitted on +S_CAP (leak, vent or burst hazard); enable it only with a supercapacitor and tie +S_CAP to GND when nothing is fitted.	October 2026
0.5	• Added drawn figures from the E1M-X Dev Board V2 netlist: block diagram, 5 V generation, power tree, current monitors, debug / console routing, SWD header, reset and boot switch, USB, Ethernet, CAN (replaces the CAN placeholder), microSD / SDIO mux, antenna, display, cameras, PCIe and M.2, audio, mikroBUS, expansion headers, user interface and status LEDs, jumpers and the I²C0 map. • Replaced the 5 V-generation and per-rail-monitor placeholders. • Corrected against the netlist: ▸ Power: USB-PD only on USB-C J11 (CYPD3177 sink, back-to-back FET Q2, Schottky D1), not on three ports; the buck input is named by its net `NetC33_2` (there is no `VIN` net); with `P10` open +S_CAP floats, so keep `P10` fitted or the trickle charger disabled; the 5 V buck is the TI LM61480 (U9) followed by the TPS25210 eFuse (U11); there is no ORing eFuse; the barrel input has no blocking diode; carrier rails +3V3, +1V8, CAM_3V8 and the USB VBUS switch are now described.	October 2026

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Revision	Changes	Date
	▸ Debug: the USB-UART bridge is a single-port Silicon Labs CP2102 (U29) on USB-C J27, selected by jumpers P11 and P14; not an FTDI dual-channel bridge. P0Rn has no carrier pull-up. MODULE_EN is the jumper P12, not a push-button; MODULE_STBY is not connected. ▸ Boot and reset: SW1 covers B0OT0–B0OT3 (B0OT2 is not hard-strapped); of its option links only R108 is fitted (1 kΩ); R93 / R94, R105–R107, R109 and R110 are not fitted (warning added, including that fitting both links of a pair shorts +VI0 to GND). S1 acts on P0Rn only; the claim that holding it asserts B0OT3 was removed. ▸ Boot Mode Selection: the board ships with 1 kΩ at R108 (B0OT1 to GND) and SW1 position 2 closed, so B0OT1 = 0; the other straps have no link fitted and read 1 through the RZ/V2N internal pull-ups. The factory default is Mode 1 (eMMC) with a CA55 boot (was: the module's own strap defaults apply). Any other setting needs a link position fitted with a 1 kΩ resistor in place of the 0 Ω link, with B0OT2 kept at 1 (R106 not fitted). Mode 3 is the RZ/V2N boot ROM's SCIF serial download over the CP2102 on J27 (was: SCIF download (USB)). Note added that a custom carrier must not copy the EVK's reliance on the internal pull-ups. Bring-up checklist and the reset / boot figure updated. ▸ USB: USB0 (USB 3.0) goes to the Type-A host J29; USB2 goes through mux U47 to J27 or M.2 Key E; J11 carries power only. ▸ Antenna: only ANT_2.4GHz is routed, to the RF receptacle J1; on the chip-antenna path L2 / L3 are fitted and R132, L4, A1 are not. ▸ CAN: 2-pin connectors J24 / J25 with fixed split termination (no jumpers, no screw terminals); the carrier also carries TCAN1044 transceivers U51 / U52 on alternative 0 Ω links. Warning added: with a V2N / V2N-M1 module (1.8 V logic-level CAN pads) the transceiver links R227–R234 must be fitted and the bypass links R235–R238 removed; as assembled (pick-and-place) the bypass links are fitted, which puts J24 / J25 straight on the SoC CAN-FD pins. ▸ microSD: the SDIO lines are multiplexed (U38 / U39) between J7 and M.2 Key E. ▸ microSD and PCIe mux: SD_RST reaches only J16 pin 23 (through U39, SEL low; otherwise not connected; J7 has no reset pin). The PCIe lane muxes are off at power-up (PD pulled high by R154) until the module drives I00 low; SEL low selects J23, high selects J16. ▸ Cameras: CSI0 goes through mux U1 to J5 (15-pin) or J4 (22-pin); CSI1 is on the 60-pin board-to-board J12; the 8-bit parallel camera connector J22 is now described; the carrier fits ESD clamps on the CSI lanes. ▸ PCIe: four PI3DBS12212A lane muxes, the SY75602 clock buffer and the TMUX121 I²C switch replace the "PI3WVR648 not populated / TBD" text; Key M on a V2N module is reached only through the muxes (not "always, no mux"). ▸ mikroBUS: SPI1, UART1, PWM0, IO3 and ANA_S0 (not SPI2); its reset line is not wired to the module. ▸ User interface: RGB LED D19, encoder E1, reset S1 and the power-good LEDs replace the non-existent USR LEDs / button and IO_EN / M1_RDY LEDs. ▸ Notes added: +L_VIO (display level shifters) and VCC_IN_5V (Display 2 backlight) have no supply connection, and the U13 BMI323 address strap selects 0x69 in the V2 netlist. ▸ Current Measurement: the +V_CAM2 monitor U32 (INA236B, A0 = GND) is fitted and strapped to 0x48; shown fitted in the power-tree, current-monitor and I²C0 figures. ▸ Current Measurement and I²C: 0x48 is also the TAS2563 global address, which U27 / U28 answer from power-up, so as built U32 cannot be read; warning added with the rework (U32 A0 from 0V to I2C0.SCL, address 0x4B). Address tables, Known Design Notes and the current-monitor and I²C0 figures show 0x48 as built and 0x4B after the rework. ▸ Audio: the TAS2563 address straps R24 and R75 are not fitted (R67, R68 fitted), so AD0 of U27 has 10 kΩ to GND (0x4D) and AD0 of U28 has 10 kΩ to +1V8 (0x4E); shown in the audio figure. ▸ USB figure: the U47 select pin (pin 10) is labelled SEL, TI's name for it.	

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Revision	Changes	Date
	▸ Module mounting: the E1M-X EVK uses a spacer PCB under the SoM (E1M-STD 1.5 section 5.2, option (a)). ▸ I^2C and Current Measurement tables: the U34 rail is named by its net +V_CAM3 (was +VCAM3). ▸ Expansion headers figure: the DAC0 / DAC1 amplifiers U23 / U24 (OPA189) are drawn as op-amp symbols (was a box), with their feedback R85 / R86 (OUT to –IN) and R81 / R82 (–IN to GND), 10 kΩ each.	
0.6	• Document status: the title page now reads Preliminary, matching the running header (it read Draft).	October 2026
0.7	• Board overview: four INA236 current monitors plus one INA228 (was three INA236), as in Current Measurement. • Ethernet: the on-module PHYs are the Realtek RTL8211FI-VD-CG (was RTL8211FDI), as in DS-V2N-001.	October 2026
0.8	• Release history: every entry formatted as a bullet list.	October 2026
0.9	• Table of Contents: each entry links to its section; the front-matter lists are set tighter.	October 2026
0.10	• Questions and corrections: removed the shut-down community forum; they go to email.	November 2026
0.11	• Product name on page 1 links to the product page on alplab.ai.	November 2026
0.12	• PCIe Reference Clock: the reference clock comes from the on-module clock generator through the on-module reference-clock buffer to PCIE0_CLK_P / PCIE0_CLK_N (was “generated on-module by the RZ/V2N”); the carrier adds no second source; the EVK clock buffer U44 still drives both M.2 slots. • PCIe Reference Clock: on a V2N-M1 module the M.2 slots have a reference clock only while the DX-M1 rails are up; hardware-damage warning added on the clock-generator DIFF1 output. PCIe figure note updated. • PCIe and M.2 Expansion: the on-module PCIe lane switches connect the controller either to the DX-M1 or to the PCIE0 pads (was “permanently routed to the DX-M1 and multiplexed out”). • New Module Control Pads section: AD3 (RTC_WAKE_N), AI3 (PMIC_GPIO5_10V), AK3–AM3 (M1_BOOT0–M1_BOOT2, V2N-M1), AO3 / AP3 (GP_I2C), and the row-62 pads AE62, AL62–AP62, which are not connected on the module; the EVK connection of these pads is to be confirmed against the board netlist. • Module Control Pads: hardware-damage warning on 10 V at AI3, back-power warning on M1_BOOT0–M1_BOOT2, and a warning against carrier pull-ups on GP_I2C. • Module Control Pads: back-power warning (V2N-M1) against carrier pull-ups on the DX-M1 GPIO pads IO0–IO6 and IO17–IO24. • M.2 Key M: on a V2N-M1 module the slot also needs the EVK lane muxes enabled and set to the slot; their controls IO0 / IO1 are then the DX-M1 GPIOs GPIO00_15 / GPIO00_13. • Module Enable / Standby: hold MODULE_EN low (P12 fitted) at least 150 ms before removing 5 V. • Reset: S1 resets the RZ/V2N with the module rails up (was: a power-on reset of the RZ/V2N, GD32 and DX-M1); reset-and-boot figure note updated. • SuperCap Rail: +S_CAP is the backup input of the on-module RTC; the module has no backup capacitor of its own (was: hold-up for the RTC and DX-M1 model context). • Secondary Rails: the on-module PMIC is named by its function. • Expansion Headers: with these modules the row-62 pads AE62 and AL62–AP62 have no module connection.	November 2026

Table 1 Release History

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1 Purpose and Scope

This document is the schematic-level user guide for the **E1M-X Evaluation Kit** (45 × 65 mm carrier), targeting the **E1M-X V2N** and **E1M-X V2N-M1** SoM families based on the Renesas RZ/V2N vision-AI MPU (with the V2N-M1 family adding an on-module DeepX DX-M1 25-TOPS AI accelerator). The E1M-X EVK mounts the SoM on a spacer PCB that sits on the carrier (mounting option (a) of E1M-STD 1.5 section 5.2); the SoM is never placed directly on the carrier.

It complements:

- The **E1M-X V2N Datasheet** (DS-V2N-001) and **E1M-X V2N-M1 Datasheet** (DS-V2N-M1-001) — the canonical pin and electrical reference.
- The **E1M-X V2N HW Design Guide** (HG-V2N-001) and **E1M-X V2N-M1 HW Design Guide** (HG-V2N-M1-001) — carrier-board design rules.
- The **E1M EVK User Guide** (UG-E1M-001) — the smaller 35 × 35 mm sibling kit, structurally mirrored here.
- The **E1M Specification** (E1M-STD-1.0) — the open standard the form factor and pinout conform to.

This guide answers “where does each signal go on the E1M-X EVK carrier?” — it is not a tutorial; for that, see the **E1M-X EVK Getting Started Guide** (QS-E1M-X-EVK-001).

2 Safety, Handling, and ESD

- **ESD-sensitive**. Handle on a grounded mat with a wrist strap.
- **Hot-plug not supported** for the M.2 slots, USB host port, or display / camera FFCs.
- **No customer-rework** of the SoM is permitted; rework voids warranty.
- **Max ambient operating temperature**: +85 °C. Free-air convection is sufficient for hello-world workloads; full DRP-AI + DX-M1 + dual-Ethernet pushes the SoM towards its thermal limit and a heatsink is recommended.

> **Warning:** The on-module DeepX DX-M1 (V2N-M1 variants only) dissipates significant heat at full load. Plan for active cooling or a copper-pour heatsink contact when running sustained inference.

3 Functional Overview

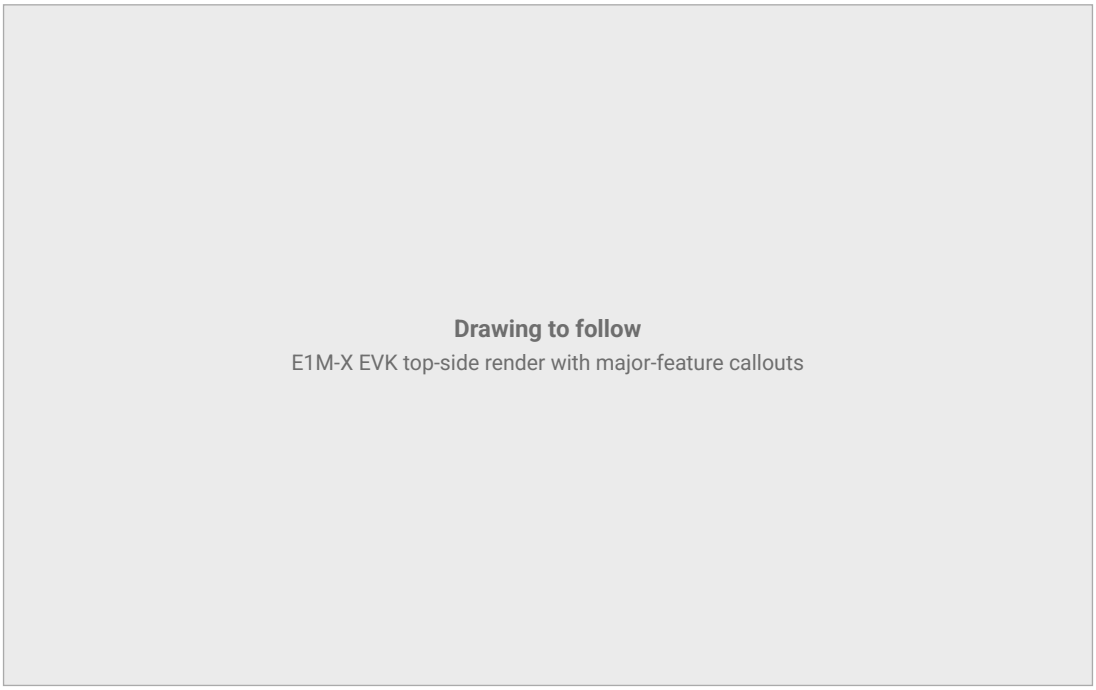
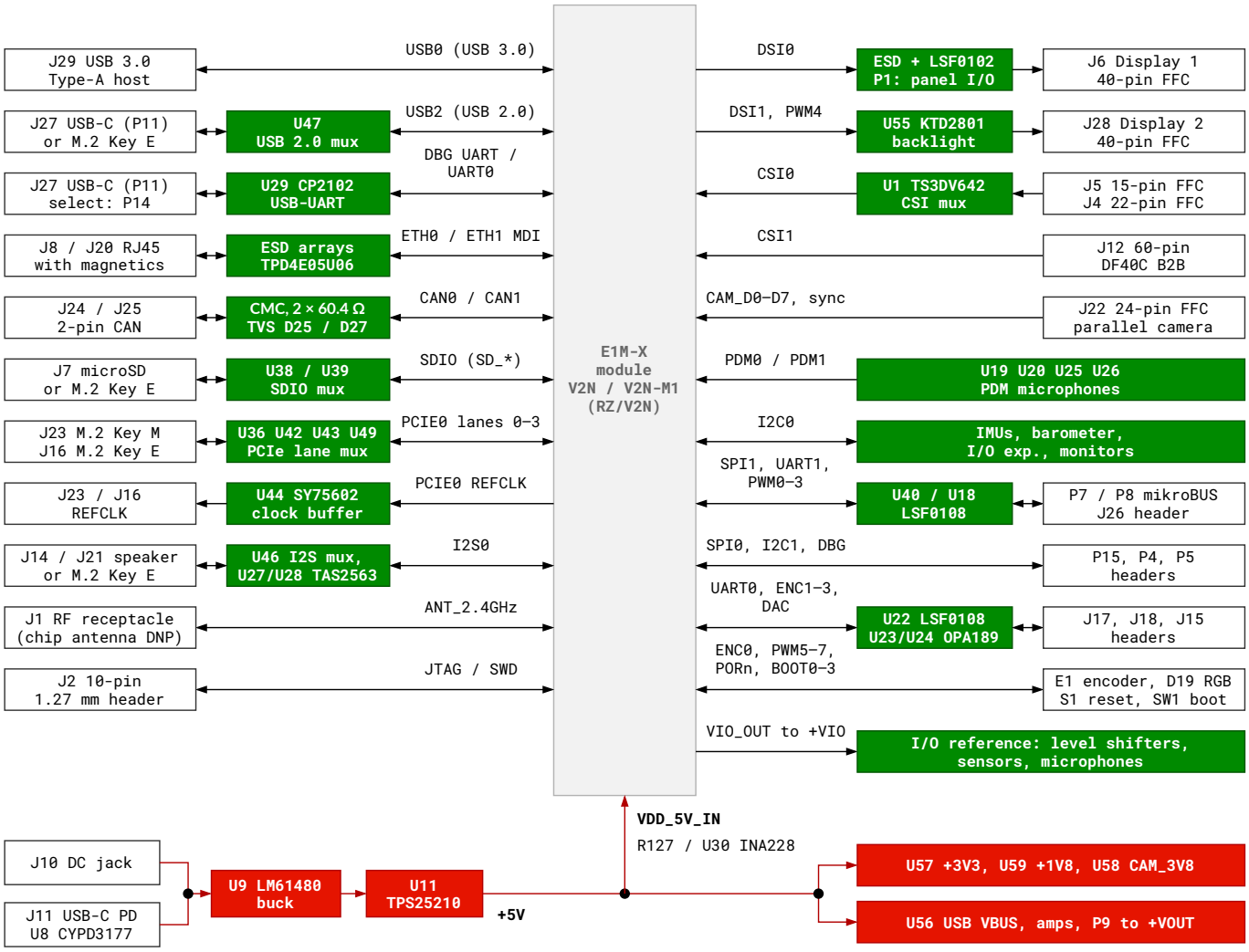


Figure 1 E1M-X EVK top-side render with major-feature callouts

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The E1M-X EVK exposes every interface defined in the E1M-X form factor that the V2N family routes. Section §4 onward covers each block in detail. The figures in this guide are drawn from the E1M-X Dev Board V2 netlist; the module is shown only as an outline.



Green: carrier ICs. Red: power. White: connectors. Arrows: signal direction seen from the module. Mux selects: see each section. CAN: as assembled J24 / J25 are wired straight to the **SoC CAN-FD pins (R235–R238 fitted); with a V2N / V2N-M1 module remove R235–R238 and fit R227–R234 for U51 / U52 (see CAN Bus).**

Figure 2 E1M-X EVK block diagram (E1M-X Dev Board V2)

Block	Description
Power	12 V barrel jack J10 and a USB-PD sink on USB-C J11. LM61480 buck and TPS25210 eFuse make +5V, which feeds the SoM's VDD_5V_IN pads through a sense resistor; carrier bucks make +3V3, +1V8 and CAM_3V8. INA236 / INA228 current monitors on the main rails.
Boot / Reset / Debug	4-position DIP switch SW1 on BOOT0–BOOT3; PORn push-button S1; MODULE_EN jumper P12; 10-pin 1.27 mm SWD/JTAG header J2; Silicon Labs CP2102 USB-UART bridge on USB-C J27.
USB	USB 3.0 Type-A host J29 (USB0, switched VBUS); USB-C J27 for USB2 (through mux U47) or the CP2102 console; USB-C J11 is a power input only.
Ethernet	2 × RJ45 with integrated magnetics (J8, J20) and ESD arrays, routed to both on-module Realtek RTL8211FI-VD-CG PHYs.

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Block	Description
Storage	microSD socket J7 on the SoM's SDIO interface, through an SDIO mux shared with M.2 Key E; M.2 Key M J23 for NVMe SSDs.
Display	2 × MIPI-DSI 40-pin FFC connectors (J6 on DSI0, J28 on DSI1); only Display 1 (DSI0) is usable with V2N / V2N-M1 SoMs. The MIPI-DSI → HDMI bridge is not populated.
Camera	CSI0 on J5 (15-pin) or J4 (22-pin) through mux U1; CSI1 on the 60-pin board-to-board J12; 8-bit parallel camera on J22.
CAN-bus	2 × 2-pin connectors (J24, J25) with fixed split 120 Ω termination, common-mode chokes and TVS diodes.
Audio	Four PDM microphones; two TI TAS2563 smart amplifiers on I2S0 for speaker output.
Expansion	mikroBUS sockets P7 / P8, 10-pin socket J26, headers P15, J15, J17, J18; M.2 Key E J16 for Wi-Fi / cellular / co-processor cards.
Sensors	On-board IMUs (TDK ICM-42670-P, Bosch BMI323) and barometer (Bosch BMP581) on the EVK's alp_i2c0 bus.
Current monitoring	Four TI INA236 monitors and one TI INA228 (+5V input) expose live current / voltage telemetry through the SDK's <alp/chips/ina236.h> and <alp/chips/ina228.h> drivers.

Table 2 Major functional blocks on the E1M-X EVK

4 Power System

4.1 Power Inputs

4.1.1 Barrel Jack (primary)

12 V DC, centre-positive, 5 A maximum, on J10 (Würth 694108301002, a 5 A / 24 V rated jack). This is the recommended supply for the E1M-X EVK because the V2N family's peak power (full DRP-AI + dual-Ethernet + M.2 SSD + display + camera) exceeds the USB-PD ceiling on most hosts. J10 pin 1 connects straight to the buck input (the U9 VIN pins, net NetC33_2); the only protection on it is the TVS D48 (SMF15A).

> **Warning:** J10 has no reverse-polarity protection and no series diode. Check the polarity of the supply before you connect it.

4.1.2 USB-C Inputs

Only USB-C J11 powers the board. It carries no data (its D+ / D− pins are not connected). The Infineon CYPD3177 USB-PD sink U8 negotiates on CC1 / CC2 and switches USBPD_VBUS through the back-to-back P-channel pair Q2 (DMP3036SSD-13, gate drive R197, R16, R21, zener D2); the Schottky diode D1 (CMS04) then joins USBPD_V to the buck input (NetC33_2).

The other two USB ports do not power the board: the VBUS of USB-C J27 feeds only the CP2102 USB-UART bridge and the red LED D8, and USB-A J29 is a host output.

> **Warning:** Do not connect J10 and J11 at the same time. The barrel input has no blocking diode, so a USB-PD contract above the barrel voltage drives current back into the barrel supply.

4.2 Main 5 V Generation and Protection

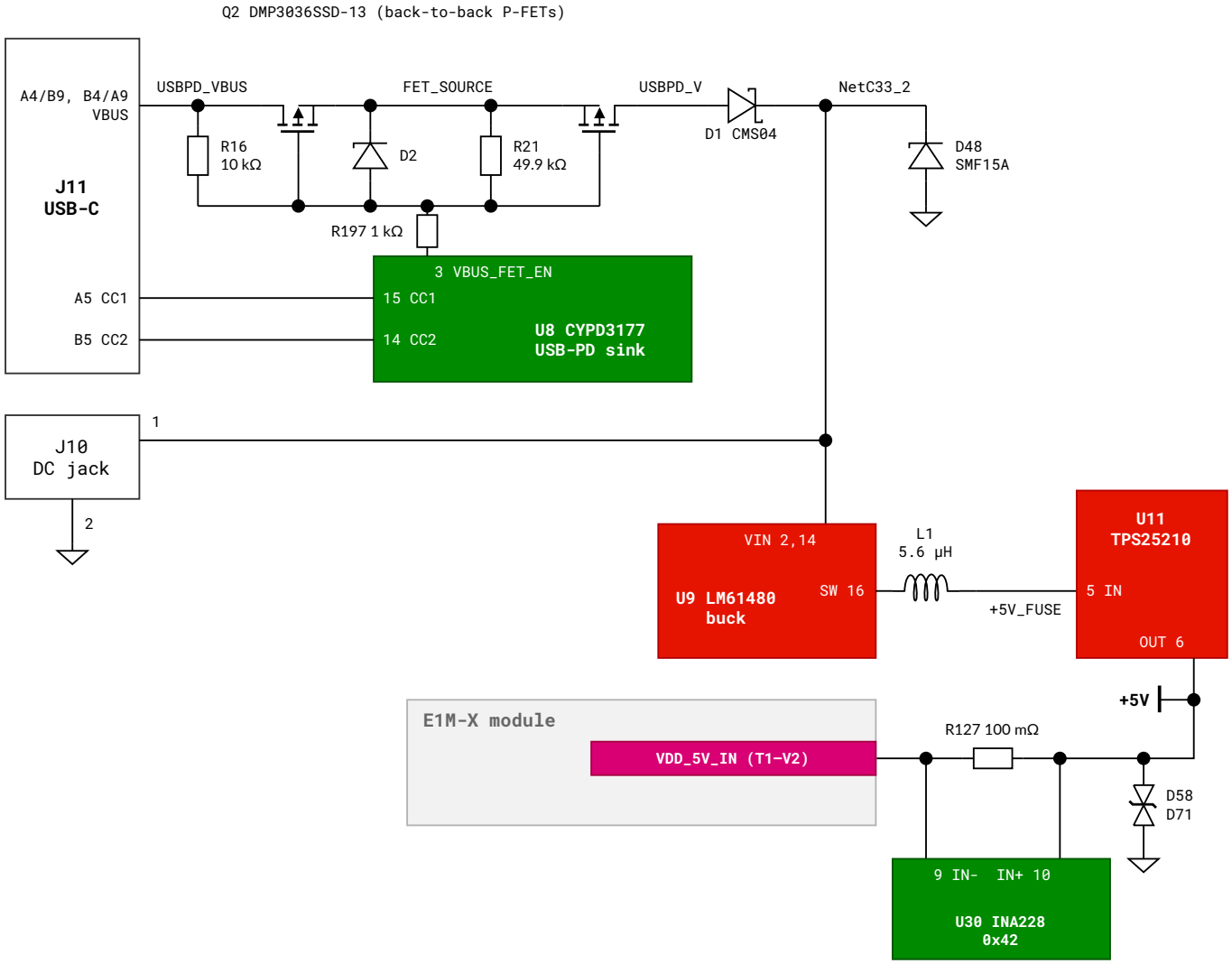
A TI LM61480 buck converter (U9, L1 5.6 µ H) turns its input (NetC33_2, the U9 VIN pins) into +5V_FUSE. A TI TPS25210 eFuse (U11) switches it onto +5V with inrush (dV/dt) control and current limiting; its power-good output 5V_PG starts the rest of the carrier rails. Protection elements:

- TVS D48 (SMF15A) on the buck input (NetC33_2).
- eFuse U11: UVLO divider R36 470 kΩ / R37 182 kΩ, current-limit resistor R42 1.13 kΩ, dV/dt capacitor C46 2.2 nF.

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- Bidirectional TVS diodes D58 / D71 on +5V.

+5V reaches the SoM's VDD_5V_IN pads through the 100 mΩ shunt R127 of the INA228 monitor U30.



U9 EN divider: R26 100 kΩ / R28 11.3 kΩ. U11: UVLO R36 470 kΩ / R37 182 kΩ, ILM R42 1.13 kΩ, dVdt C46 2.2 nF.

J11 data lines are not connected (power only). U11 PG (5V_PG) enables U57 (+3V3) and the green LED D3.

Figure 3 E1M-X EVK 5 V generation: USB-PD input, barrel input, buck, eFuse and the module supply shunt (simplified)

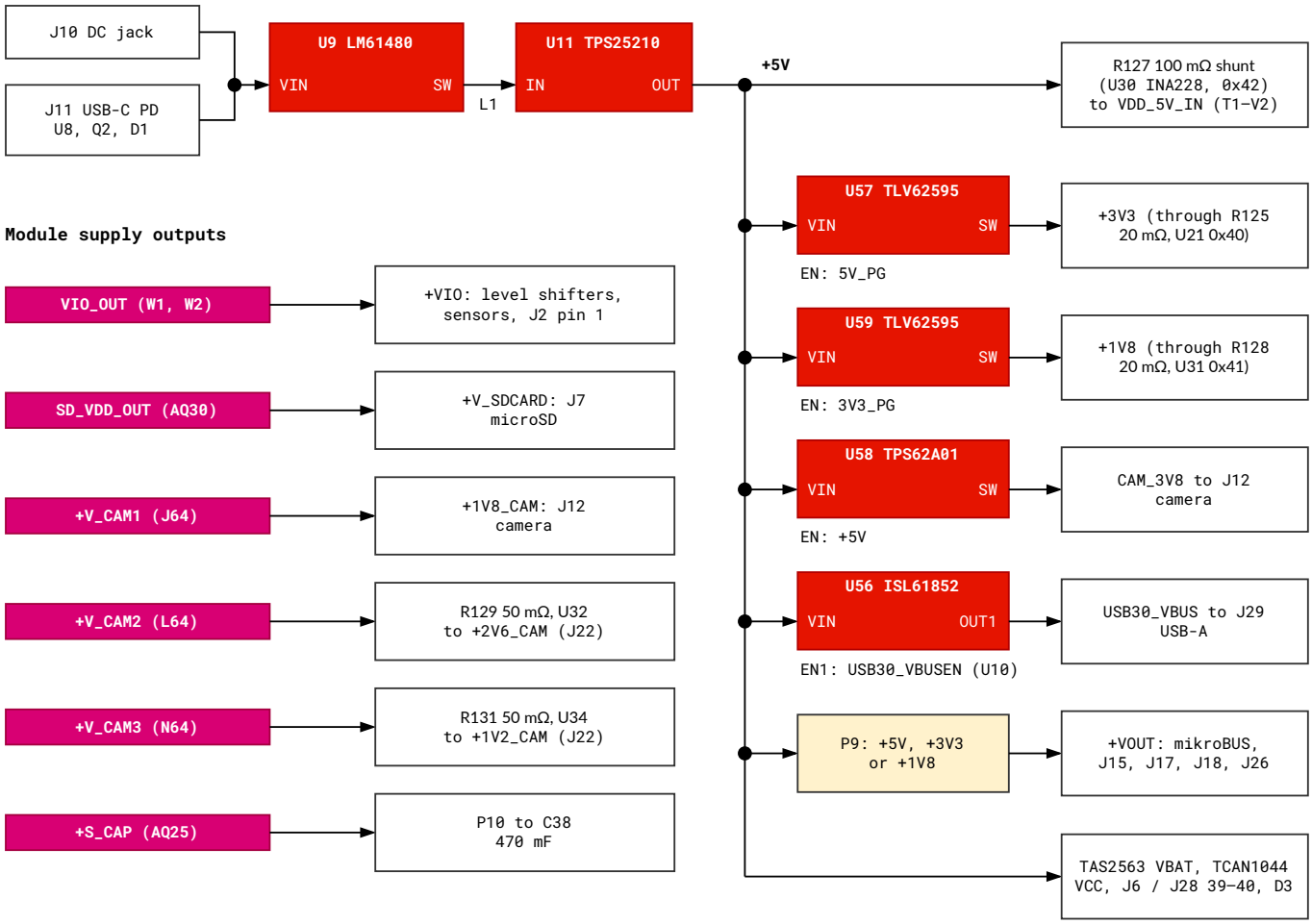
4.3 Secondary Rails

The on-module main PMIC, together with a Renesas DA9292 dual buck converter and discrete regulators, generates every silicon-internal rail (LPDDR4X DRAM, RZ/V2N core, IO 1V8, etc.). The carrier supplies **only** the 5 V input to the module.

For its own circuits the carrier makes, from +5V:

- +3V3: TI TLV62595 U57, enabled by 5V_PG; its power-good 3V3_PG enables +1V8.
- +1V8: TI TLV62595 U59.
- CAM_3V8: TI TPS62A01 U58, for the camera connector J12.
- USB30_VBUS: Renesas ISL61852 power switch U56 for J29, enabled by the module through U10.

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Power-up order: +5V (U11 PG = 5V_PG), then +3V3 (U57 PG = 3V3_PG), then +1V8 (U59 PG = 1V8_PG).
D3 / D4 / D9 light with each PG. All current monitors sit on I2C0 (see Current Measurement).

Figure 4 E1M-X EVK power tree: inputs, regulators, current monitors and the module supply outputs

Two output rails are sourced **from** the SoM to the carrier board:

- VIO_OUT (1V8) drives the I/O-reference rails of every level-shifter on the carrier (USB-C CC, I/O-expander logic, etc.).
- SD_VDD_OUT (1V8 / 3V3 selectable) supplies the microSD socket; the SoM auto-switches it for high-speed vs default-speed cards.

> **Warning:** VIO_OUT and SD_VDD_OUT are outputs from the module, not power inputs. Do not source them externally.

4.4 SuperCap Rail

Jumper P10 connects the module's +S_CAP pad to the on-board supercapacitor C38 (470 mF, 3.5 V, FC0V474ZFTBR24). With P10 open, +S_CAP is left floating, and the carrier has no other way to tie it to GND: keep P10 fitted, or keep the RTC trickle charger disabled while P10 is open. +S_CAP is the backup input of the on-module RTC (RV-3028-C7): the backup element keeps the RTC running while 5 V is absent. The module has no backup capacitor of its own. TBD — the V2N reference firmware does not yet exercise this path; see **bring-up-v2n.md** in the SDK.

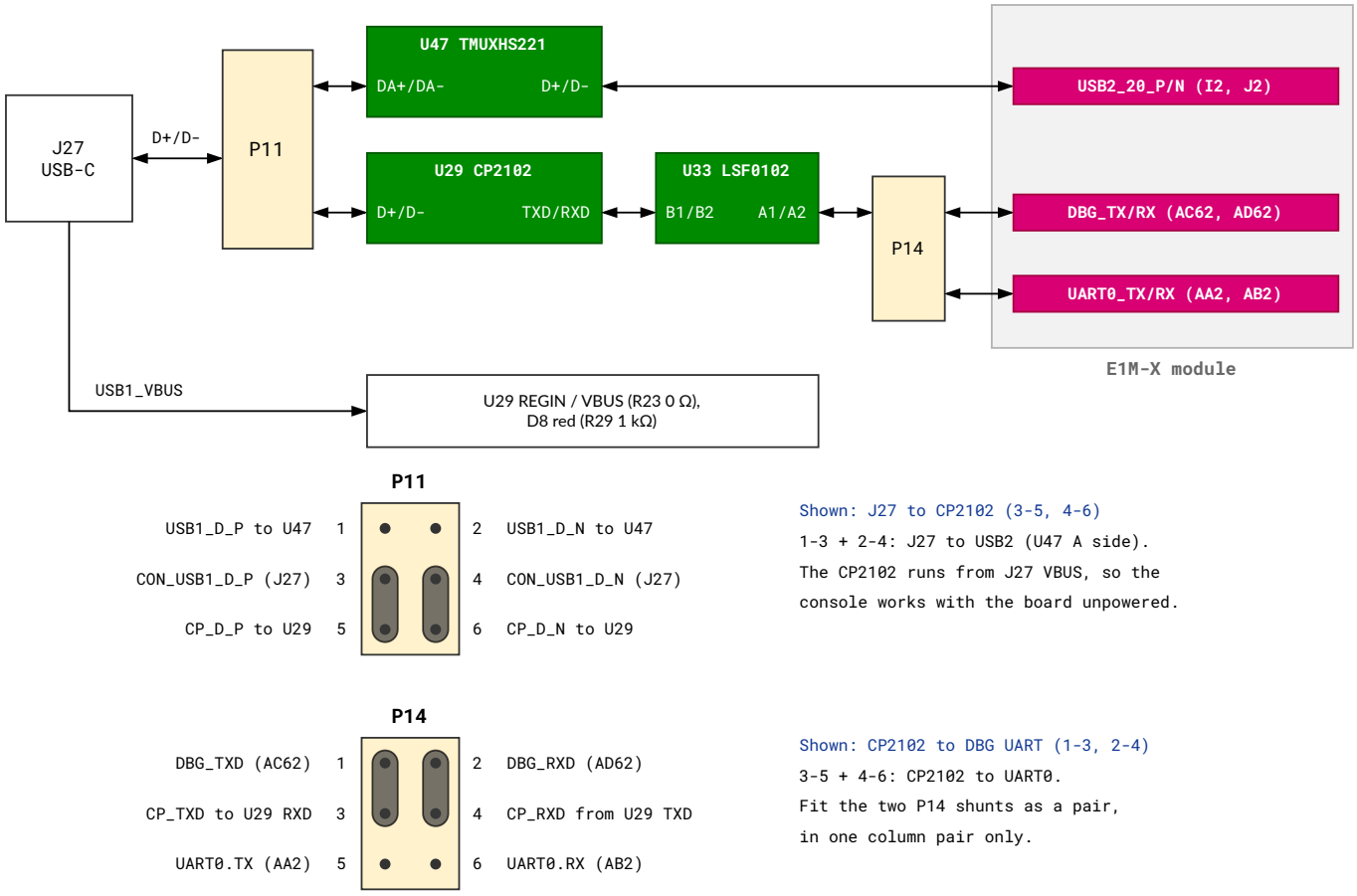
> **Warning:** **Never enable the RTC trickle charger with a primary lithium coin cell fitted on +S_CAP.** The cell can leak, vent or burst. Enable the trickle charger only when a supercapacitor is fitted, and keep it disabled for a coin cell or when nothing is fitted (tie +S_CAP to GND; do not leave it floating). On the E1M-X EVK that means: P10 fitted (C38 connected) before the trickle charger is enabled.

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5 Boot, Reset, and Debug

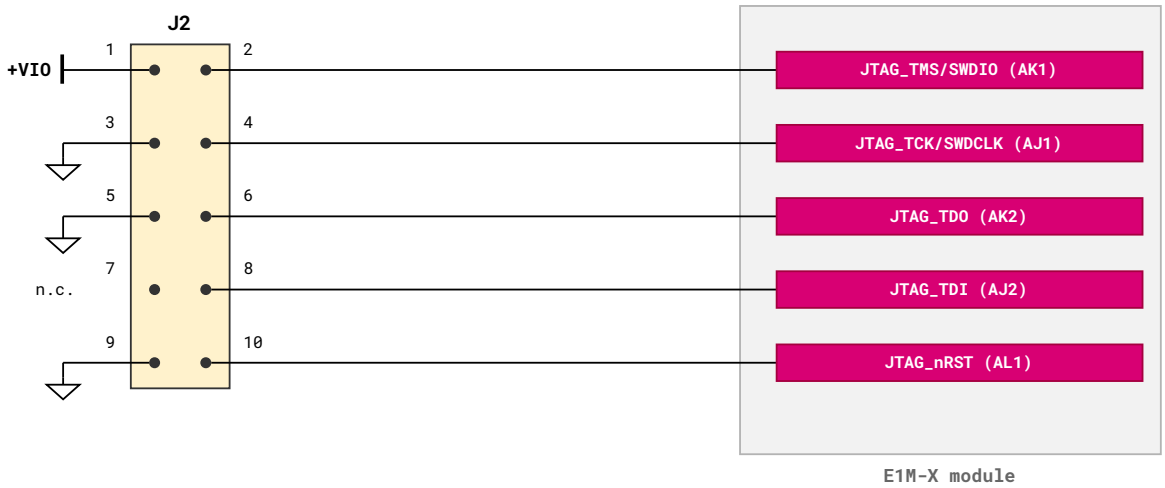
5.1 Debug Connectors

- **Cortex 10-pin SWD/JTAG header** J2 (1.27 mm pitch) for external SEGGER J-Link or any CMSIS-DAP probe. Connects directly to the SoM's JTAG_* pads; pin 1 carries +VIO, the probe's I/O reference. The 6-pin footprint J3 is not fitted.
- **Silicon Labs CP2102 USB-UART bridge** (U29) on USB-C J27: a single serial port. Jumper P11 connects the J27 data lines either to the CP2102 or to the module's USB2 (through mux U47); jumper P14 connects the CP2102 either to the module's DBG_TX / DBG_RX pads or to UART0. The level shifter U33 adapts the CP2102 3.3 V UART to +VIO. The CP2102 is powered from J27 VBUS, so the port enumerates even with the board unpowered.



U47 A/B (pin 10) = USB_MUX_SELECT (IO24, AR29). U33 shifts the CP2102 3.3 V UART to +VIO.
UART0 also reaches J17 through U22 (LSF0108).

Figure 5 USB-C J27 routing: P11 selects USB2 or the CP2102; P14 selects the UART the CP2102 serves



Pin 7: no connection. Probe I/O level = +VIO (pin 1). J3 (6-pin SWD footprint) is not fitted.

Figure 6 10-pin SWD/JTAG header J2

5.2 Reset

The PORn push-button S1 pulls the SoM's PORn pad (net MCU_RST) to GND. The carrier adds only C1 (0.10 µ F) on the line; there is no carrier pull-up.

- Press momentarily to reset the RZ/V2N with the module rails up. PORn is open drain at 1.8 V on the module (10 kΩ pull-up to the module 1.8 V rail), driven by the PMIC reset output and the power controller.
- S1 has no connection to the boot straps: it does not change BOOT3 or any other BOOTx level.

5.3 Boot Mode Selection

The 4-position DIP switch selects the RZ/V2N boot source. The mapping mirrors **DS-V2N-001 §4.1**:

BOOT1	BOOT0	Mode	Device	CA55 boot	CM33 boot
0	0	Mode 0	eSD (3.3 V execution)	Supported	Not supported
0	1	Mode 1	eMMC (1.8 V I/O) *(factory default: R108 fitted, SW1 position 2 closed)*	Supported	Not supported
1	0	Mode 2	QSPI NOR (1.8 V I/O)	Supported	Supported
1	1	Mode 3	SCIF serial download (CP2102 on J27)	Supported	Supported

Table 3 Boot DIP-switch mapping

The DIP switch SW1 has one position for each of BOOT0, BOOT1, BOOT2 and BOOT3. BOOT3 selects the boot CPU (high = CA55, low = CM33).

> **Warning:** Each SW1 position joins its BOOTx pad to a node with two option-link positions, one to +VIO and one to GND (0V): R109 / R110 (BOOT0, position 1), R107 / R108 (BOOT1, position 2), R105 / R106 (BOOT2, position 3) and R93 / R94 (BOOT3, position 4); the first link of each pair goes to +VIO, the second to GND. As shipped only R108 is fitted (1 kΩ); the other links are **not fitted**, so positions 1, 3 and 4 do not change the straps.

Factory default. The board ships with a 1 kΩ resistor at R108 (BOOT1 to GND) and SW1 position 2 closed, so BOOT1 = 0. The other straps have no link fitted and read 1 through the RZ/V2N internal pull-ups: BOOT0 = 1, BOOT2 = 1, and BOOT3 = 1 selects the CA55 boot. BOOT1 = 0 with BOOT0 = 1 selects Mode 1: the CA55 boots the image in eMMC. Positions 1, 3 and 4 of SW1 have no effect as shipped. Opening position 2 leaves BOOT1 to its internal pull-up (BOOT1 = 1), which selects Mode 3: SCIF serial download, the

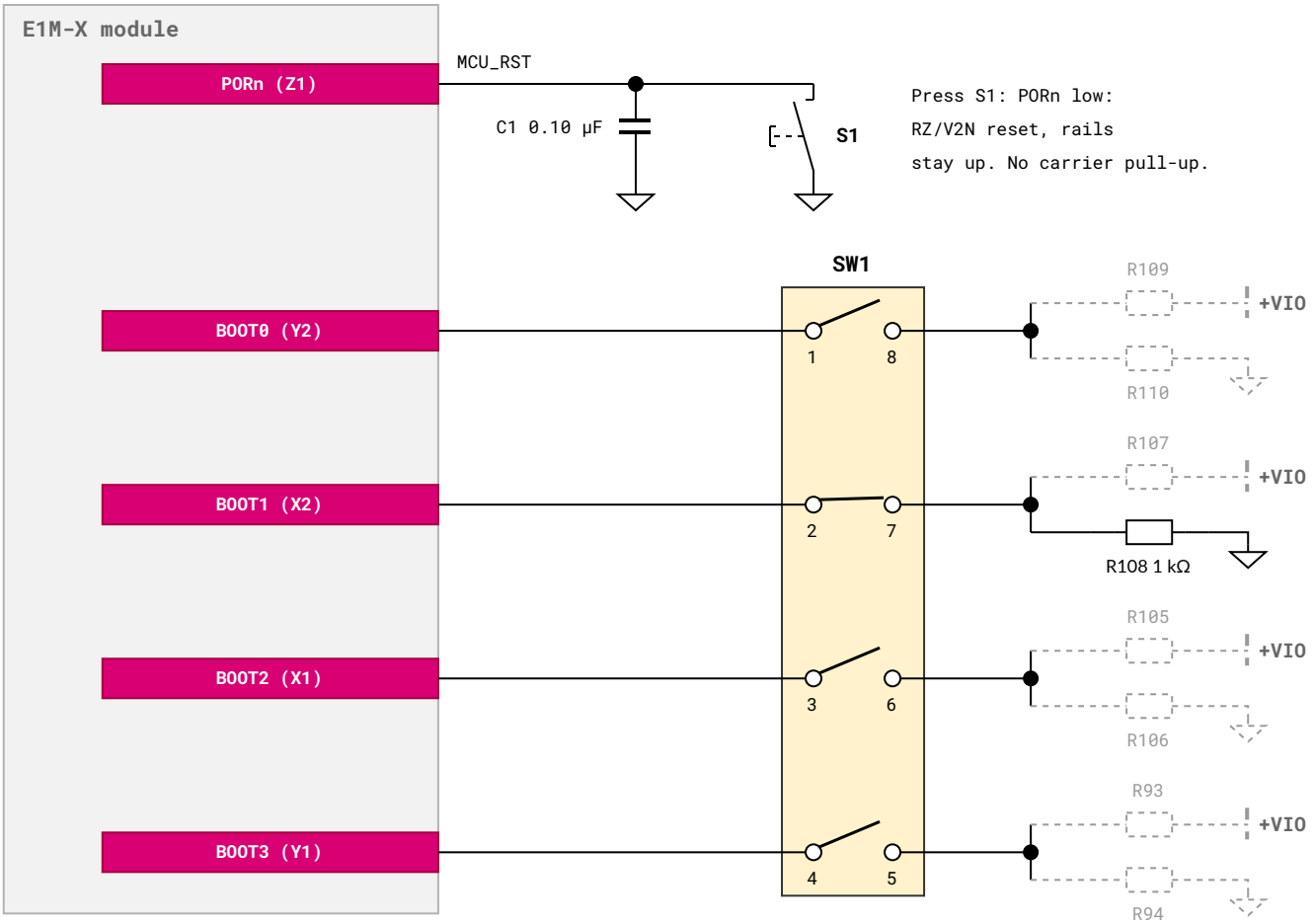
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RZ/V2N boot ROM's download mode over SCIF, which reaches the CP2102 (U29) on USB-C J27 through the DBG_TX / DBG_RX pads (P14 on 1-3 and 2-4, P11 on 3-5 and 4-6).

Note: The EVK leaves BOOT0, BOOT2 and BOOT3 on the RZ/V2N internal pull-ups. Do not copy this on a custom carrier: strap every boot pin with its own 1 kΩ resistor, as the **E1M-X V2N** and **E1M-X V2N-M1** datasheets require (Boot Modes).

Any other setting needs the links fitted. On V2N / V2N-M1 carriers every boot strap is set through 1 kΩ, so fit a 1 kΩ resistor in place of the 0 Ω link: in the GND-side position (R110, R108, R106, R94) the strap reads 0 while its SW1 position is closed; in the +VIO-side position (R109, R107, R105, R93) it reads 1 while closed. With the switch position open the strap is left to the internal pull-up and reads 1. Keep BOOT2 at 1: the V2N family needs BOOT2 = 1, so do not fit R106. R108 is fitted as shipped, so do not fit R107. For example, to boot from QSPI NOR (Mode 2: BOOT1 = 1, BOOT0 = 0) open SW1 position 2, fit 1 kΩ at R110 and close SW1 position 1 (BOOT0).

Warning: Fit only one position of each pair. With 0 Ω links, fitting both (for example R109 and R110) shorts +VIO to GND; with 1 kΩ in both, the closed strap sits at mid-rail and its level is undefined.



As shipped: R108 1 kΩ fitted and SW1 position 2 closed, so BOOT1 = 0. BOOT0, BOOT2 and BOOT3 have no link and read 1 (RZ/V2N internal pull-up): Mode 1 (eMMC), CA55 boot. Dashed grey: not fitted (R93 / R94, R105–R107, R109, R110). For another setting fit 1 kΩ in one position of a pair, never both. Keep BOOT2 at 1: do not fit R106. With R108 fitted, do not fit R107. MODULE_EN (AA1): P12 to GND. MODULE_STBY (AB1): not connected on the carrier.

Figure 7 Reset button S1 and boot switch SW1 with its option links as shipped (R108 1 kΩ fitted, position 2 closed: Mode 1, eMMC; dashed: not fitted)

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5.4 Module Enable / Standby

- MODULE_EN: 2-pin jumper P12 to GND. Fitting it pulls MODULE_EN low and disables the module; leave it open for normal use.
- MODULE_STBY is not connected on the carrier (no test point). The reference firmware does not yet use it; see **bring-up-v2n.md**.

Warning: Hold MODULE_EN low (fit P12) at least 150 ms before removing 5 V. Removing 5 V with the module on is for recovery only.

5.5 Module Control Pads

On the current E1M-X V2N / V2N-M1 modules (DS-V2N-001 0.18, DS-V2N-M1-001 0.22) some pads that the E1M-X standard lists as NC carry module signals, and the row-62 pads AE62 and AL62–AP62 are not connected on the module. The EVK column is not yet checked against the X-EVK V2 board netlist: treat it as **to be confirmed**.

Pad	Module signal	On the module	On the E1M-X EVK
AD3	RTC_WAKE_N	RTC wake output, active low, open drain. Valid in every state while 5 V is present. Carrier pull-up to its always-on rail: ≤ 5.5 V, ≥ 10 kΩ.	Not used; to be confirmed.
AI3	PMIC_GPIO5_10V	PMIC GPIO5, the PMIC in-circuit programming path (about 10 V). Joined to BOOT3 (Y1) through an on-module 0 Ω link: in normal use the same node as BOOT3.	Not used; to be confirmed. SW1 position 4 and its links R93 / R94 act on this node too.
AK3, AL3, AM3	M1_BOOT0–M1_BOOT2 (V2N-M1 only)	DX-M1 boot straps. On-module 10 kΩ pull-downs fitted (default 0); 10 kΩ pull-ups to M1_VDD_1V8 not fitted. Not connected on V2N.	Not used (straps at their default 0); to be confirmed.
AO3, AP3	GP_I2C.SCL, GP_I2C.SDA	Always-on 3.3 V I^2C, open drain, to the power controller (0x08) and the RTC (0x52); also the programming port of the power controller. 4.7 kΩ pull-ups to +3V3_AON on the module. The RZ/V2N reaches both parts on its on-module bus.	Not used, no carrier pull-ups; to be confirmed.
AE62, AL62–AP62	—	Not connected on the module.	An EVK header pin wired to one of these pads has no function with these modules.

Table 4 Module control pads and open row-62 pads on the E1M-X EVK

Warning: Hardware-damage hazard. PMIC_GPIO5_10V (AI3) is the PMIC in-circuit programming path, which takes about 10 V. Apply 10 V to AI3 only with the on-module 0 Ω link to BOOT3 removed. With that link fitted, the 10 V reaches the RZ/V2N BOOTSELCPU input and destroys the RZ/V2N. Never connect a programming supply to AI3 on the EVK.

Warning: Back-power hazard (V2N-M1). A carrier pull-up on M1_BOOT0–M1_BOOT2 (AK3–AM3) must come from a rail that is off whenever the DX-M1 I/O rail M1_VDD_1V8 is off; otherwise the DX-M1 I/O is back-powered through the pull-up.

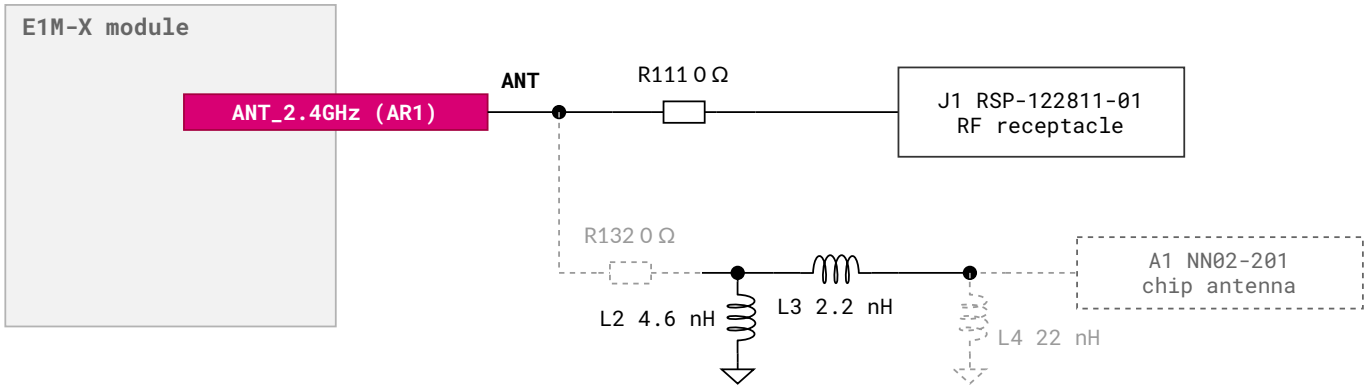
Warning: Fit no carrier pull-ups on GP_I2C (AO3 / AP3); the module has 4.7 kΩ pull-ups to +3V3_AON. Keep both pads high-impedance whenever module 5 V is absent.

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Warning: Back-power hazard (V2N-M1). On a V2N-M1 module the pads IO0–IO6 and IO17–IO24 are DX-M1 GPIOs (DS-V2N-M1-001, DX-M1 GPIO Pads), powered only while the DX-M1 rails are up. Fit no carrier pull-ups on these pads; whether the EVK has any on its IO0, IO1, IO2, IO3, IO18 and IO24 circuits is to be confirmed.

5.6 Antenna

Only ANT_2.4GHz is routed: through the 0 Ω link R111 to the RF receptacle J1 (RSP-122811-01). An alternative path to the chip antenna A1 (NN02-201) runs through R132 and the matching network L2 (4.6 nH), L3 (2.2 nH) and L4 (22 nH); L2 and L3 are fitted, but R132, L4 and A1 are not, so the path is unused. ANT_5GHz and ANT_6GHz are not connected. 50 Ω controlled-impedance trace.



Fitted: R111 to J1, L2, L3. Not fitted (grey): R132, L4, A1.
ANT_5GHz (AP1) and ANT_6GHz (AN1) are not connected.

Figure 8 2.4 GHz antenna path (grey: not fitted)

6 USB Subsystem

6.1 USB Ports

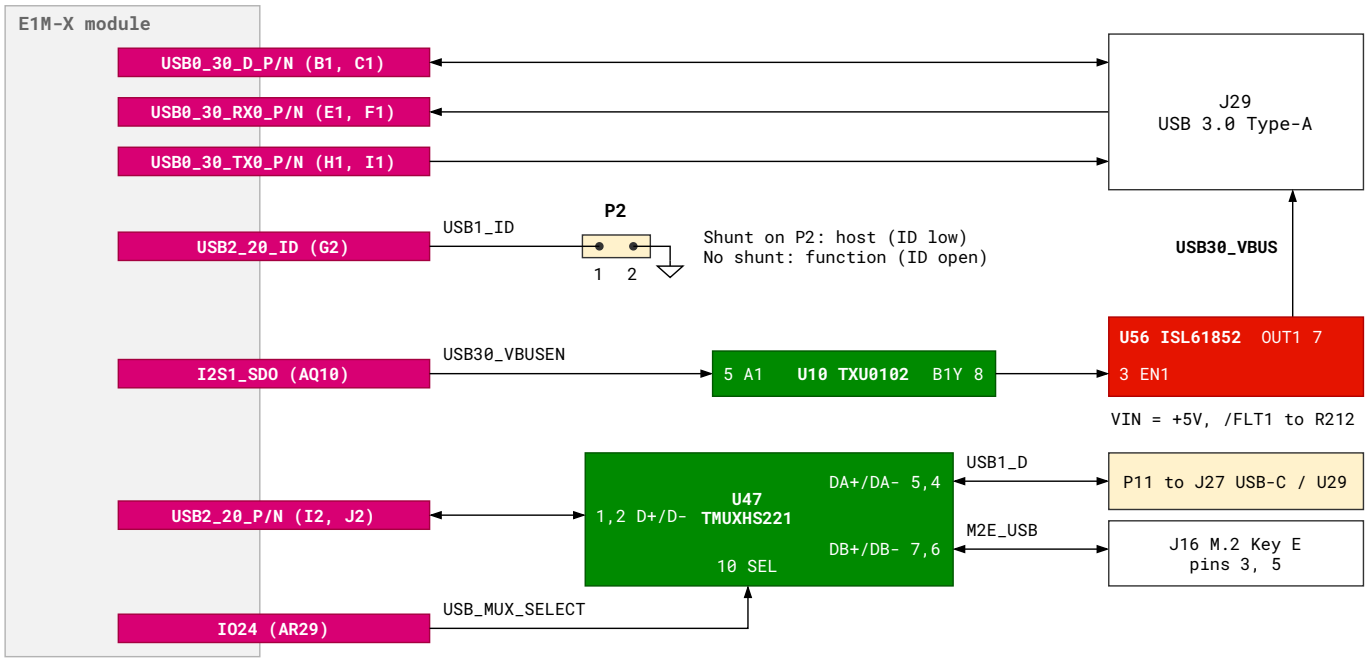
The carrier has three USB connectors:

Connector	Module port	Notes
J29 USB 3.0 Type-A	USB0 (USB0_30_*)	Host port. Data and SuperSpeed pairs go straight to the pads. VBUS (USB30_VBUS) comes from the power switch U56 (ISL61852), enabled by the module's I2S1_SDO pad (USB30_VBUSEN) through U10.
J27 USB-C	USB2 (USB2_20_*) or none	Through jumper P11: to mux U47 (TMUXHS221) and on to USB2, or to the CP2102 console bridge. CC1 / CC2 have 5.1 kΩ pull-downs (R214, R215).
J11 USB-C	none	Power input only (USB-PD sink); see Power Inputs.

Table 5 USB connectors on the E1M-X EVK

U47 routes USB2 either to J27 (through P11) or to the M.2 Key E slot; the module selects with IO24 (USB_MUX_SELECT). Jumper P2 ties USB2_20_ID to GND: fitted selects Host, open leaves the pin NC (Function). USB0_30_ID, USB0_30_VBUS, USB2_20_VBUS and the USB1_30 pads are not connected on the carrier.

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Not connected on the carrier: USB0_30_ID, USB0_30_VBUS, USB2_20_VBUS, the USB1_30 pads, U56 OUT2.
U47 /OEN is tied to GND. U10 B1Y is 5 V logic; U10 A2 (USB20_VBUSEN, I2S1_WS AQ11) drives U56 EN2.
J11 (USB-C) carries power only; J27 data goes through P11 (see Debug and Console).

Figure 9 USB routing: USB0 to J29, USB2 through U47, VBUS switch U56

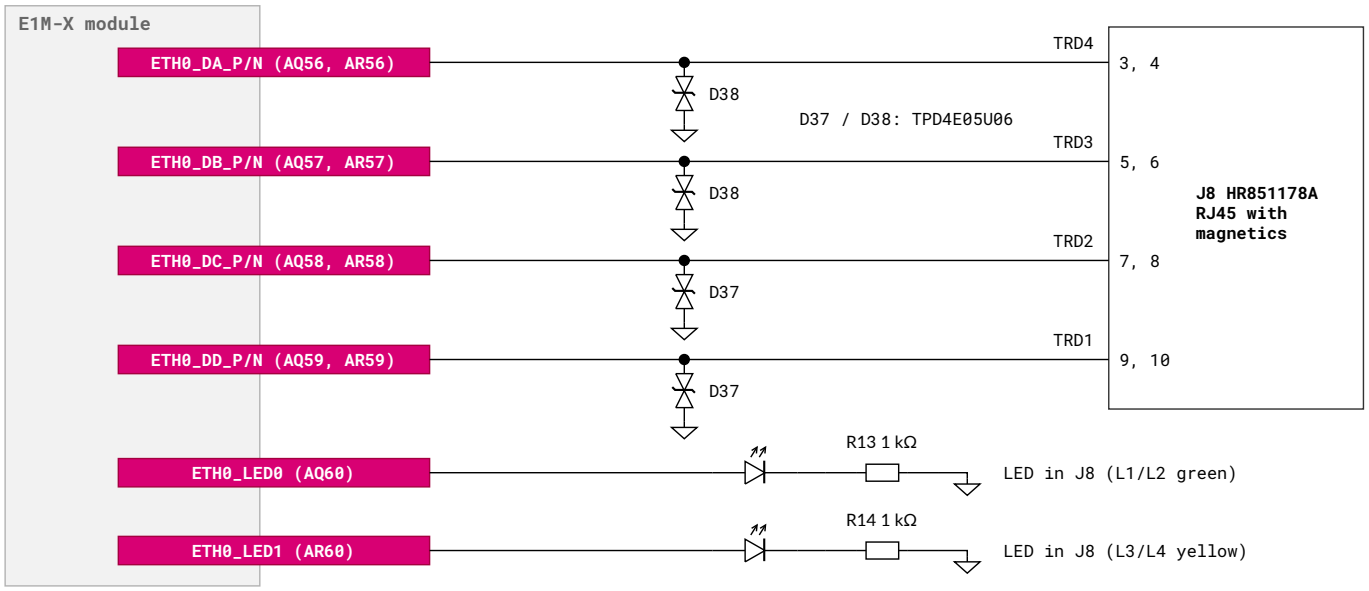
7 Ethernet

Two RJ45 jacks with integrated magnetics connect to the SoM's two on-module Realtek RTL8211FI-VD-CG PHYs (mandatory on-module per **E1M Spec** §6.5). The PHYs sit on the SoM; the carrier provides the jacks (Hanrun HR851178A, magnetics and LEDs integrated), TI TPD4E05U06 ESD arrays (D37–D40) and 1 kΩ LED resistors.

Jack	SoM port	Notes
ETH0	ETH0_DA*–ETH0_DD*	Primary 1 GbE. LEDs driven by ETH0_LED0/1.
ETH1	ETH1_DA*–ETH1_DD*	Secondary 1 GbE. LEDs driven by ETH1_LED0/1.

Table 6 Ethernet jacks on the E1M-X EVK

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ETH1 is identical: pads AQ49–AR53, ESD D39 / D40, jack J20, LED resistors R120 / R121.
Jack shield: C124 / C129 1 nF 2 kV to Shield. The pad pairs reach the jack in reverse order
(DA to TRD4 … DD to TRD1) with P and N exchanged; the PHYs are on the module.

Figure 10 Ethernet port ETH0 (ETH1 is identical)

Both ports support IEEE 1588 PTP (the V2N's MAC supports it; PHY pin-strap is set to enable PTP on power-up). Cable specifications: Cat-5e or better, 100 m max.

8 CAN Bus

8.1 Transceiver

On V2N / V2N-M1 modules the on-module CAN transceivers (TI TCAN1044AVDRBRQ1) are not fitted. The pads CAN0H/CAN0_TX (B21), CAN0L/CAN0_RX (B22), CAN1H/CAN1_TX (B24) and CAN1L/CAN1_RX (B25) carry the 1.8 V CAN-FD TX / RX logic signals of the SoC (CANFD3_CTX3 / CANFD3_CRX3 and CANFD2_CTX2 / CANFD2_CRX2), not bus levels, so the carrier transceiver is required.

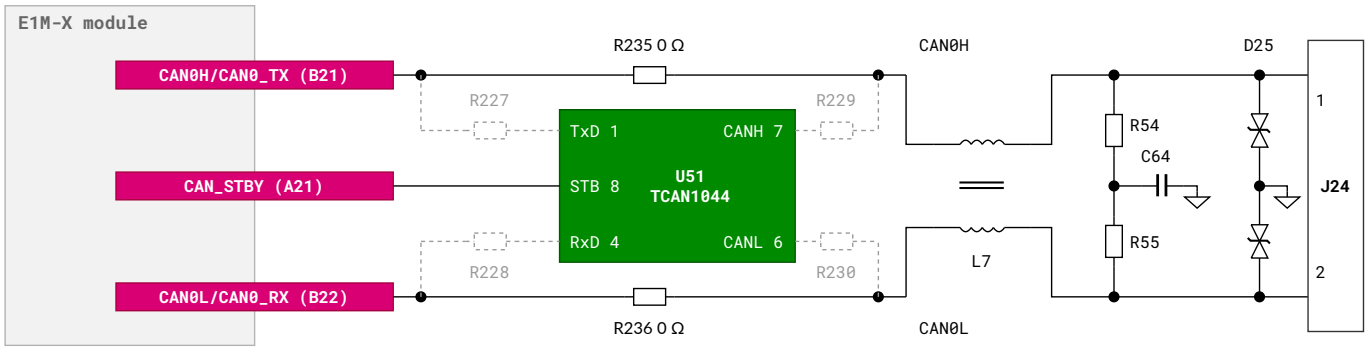
The carrier carries TCAN1044AVDRBRQ1 transceivers (U51, U52; VCC +5V, VIO +VIO, standby on CAN_STBY) on the links R227–R230 (CAN0) and R231–R234 (CAN1). The bypass links R235 / R236 (CAN0) and R237 / R238 (CAN1) connect the pads straight to J24 / J25, for modules whose CAN pads are at bus level. The two link sets are alternatives: fit one set only, never both (both sets tie the transceiver RxD output to the bus line). With a V2N / V2N-M1 module fit R227–R234 and remove R235–R238.

> **Warning:** Hardware-damage hazard. As assembled (2626-R2 pick-and-place, DNP variant) the board has R235–R238 fitted and R227–R234 not fitted, which connects J24 / J25 directly to the 1.8 V SoC CAN-FD pins. Do not connect a CAN bus to J24 / J25 with a V2N / V2N-M1 module until R235–R238 are removed and R227–R234 fitted; a live bus can overstress the SoC pins.

8.2 Connectors and Termination

- 2-pin 2 mm connectors J24 (CAN0) and J25 (CAN1), JST S2B-PH-SM4-TB: pin 1 CANH, pin 2 CANL.
- Split 120 Ω termination on each bus (2 × 60.4 Ω, centre to GND through 12 nF); it is fixed, with no jumper.
- Common-mode chokes L7 / L8 (DLW43SH510XK2L) and TVS diodes D25 / D27 (PESD2IVN24-UX).

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Solid: bypass links R235 / R236, fitted as assembled. Dashed grey: carrier transceiver U51 path (R227–R230), not fitted as assembled. The two sets are alternatives: fit one set only. V2N / V2N-M1 have no on-module CAN transceivers: the pads carry 1.8 V CAN-FD TX / RX logic. U51 VCC = +5V, VIO = +VIO. R54 / R55 60.4 Ω, C64 12 nF, D25 PESD2IVN24. CAN1 is identical: pads B24 / B25, U52, R231–R234 / R237 / R238, L8, R56 / R57, C65, D27, J25. J24 / J25: 2-pin 2 mm (S2B-PH-SM4-TB), pin 1 CANH, pin 2 CANL. The 120 Ω split termination is fixed (no jumper).

Hazard: as assembled, J24 is wired straight to the SoC CAN-FD pins (R235 / R236 fitted, R227–R230 not fitted). With a V2N / V2N-M1 module (1.8 V logic-level pads), remove R235–R238 and fit R227–R234 before connecting a CAN bus.

Figure 11 CAN0 bus path: bypass links R235 / R236 (fitted as assembled) and the transceiver U51 path (links R227–R230, fit for V2N / V2N-M1), choke, split termination, TVS and J24

9 microSD and SDIO Muxing

9.1 microSD Socket

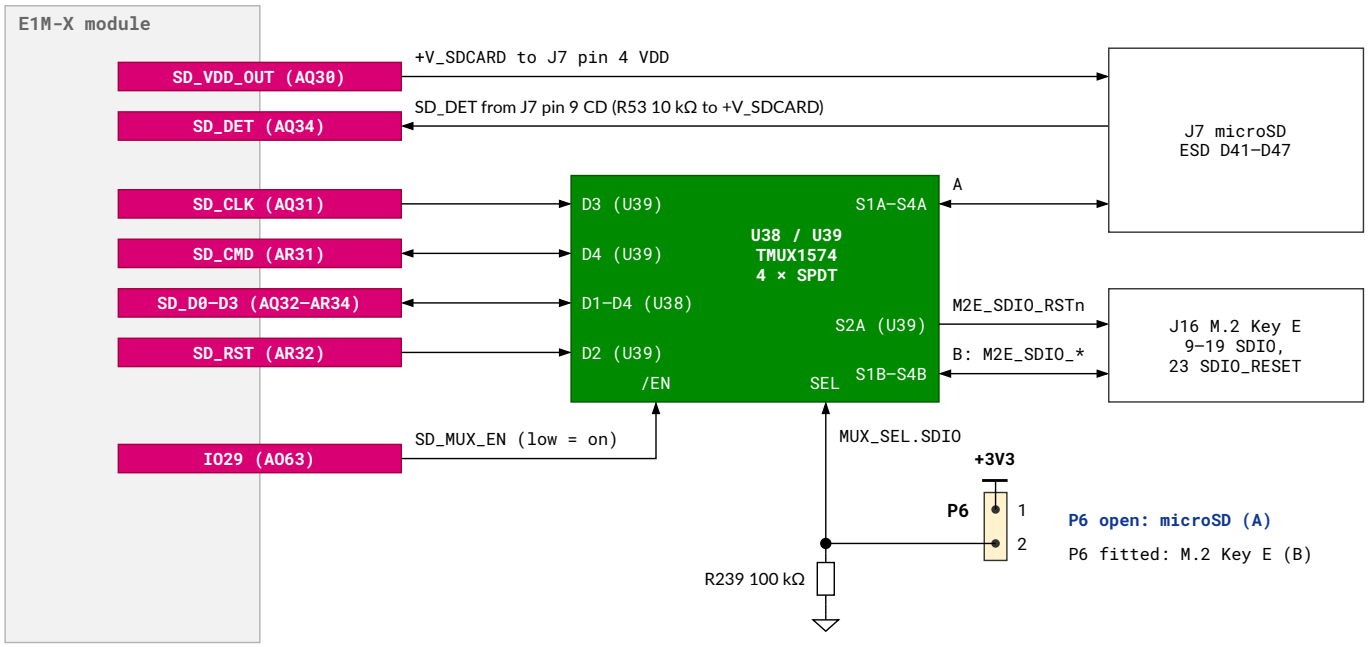
A standard push-push microSD socket on the SoM's SDIO interface (SD_CLK, SD_CMD, SD_D0–SD_D3, SD_DET, SD_RST). SD-card power comes from the SoM's SD_VDD_OUT rail (auto-switching 1V8 / 3V3).

The card-detect line (SD_DET) comes from the socket's mechanical detect contact, with R53 (10 kΩ) to +V_SDCARD. ESD diodes D41–D47 protect the card lines.

9.2 SDIO Multiplexing

Two TI TMUX1574 switches (U38, U39) route the module's SDIO lines (SD_CLK, SD_CMD, SD_D0–SD_D3) either to the microSD socket J7 or to the SDIO pins of the M.2 Key E slot J16. SD_RST goes through U39 only: in the SEL low position (the microSD position) it connects to SDIO_RESET# on J16 pin 23, and in the SEL high position it is not connected. J7 has no reset pin. IO29 (SD_MUX_EN) enables them (active low); jumper P6 selects the target: open = microSD, fitted = M.2 Key E. The M.2 Key M slot uses PCIe, not SDIO.

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U38 / U39 VDD = +3V3. P6 pin 1 = +3V3, pin 2 = MUX_SEL.SDIO through R40 (0 Ω).
SD_RST reaches J16 pin 23 (SDIO_RESET) through U39 S2A, so only with A (microSD) selected;
U39 S2B is not connected and J7 has no reset pin.

Figure 12 microSD socket and the SDIO mux U38 / U39

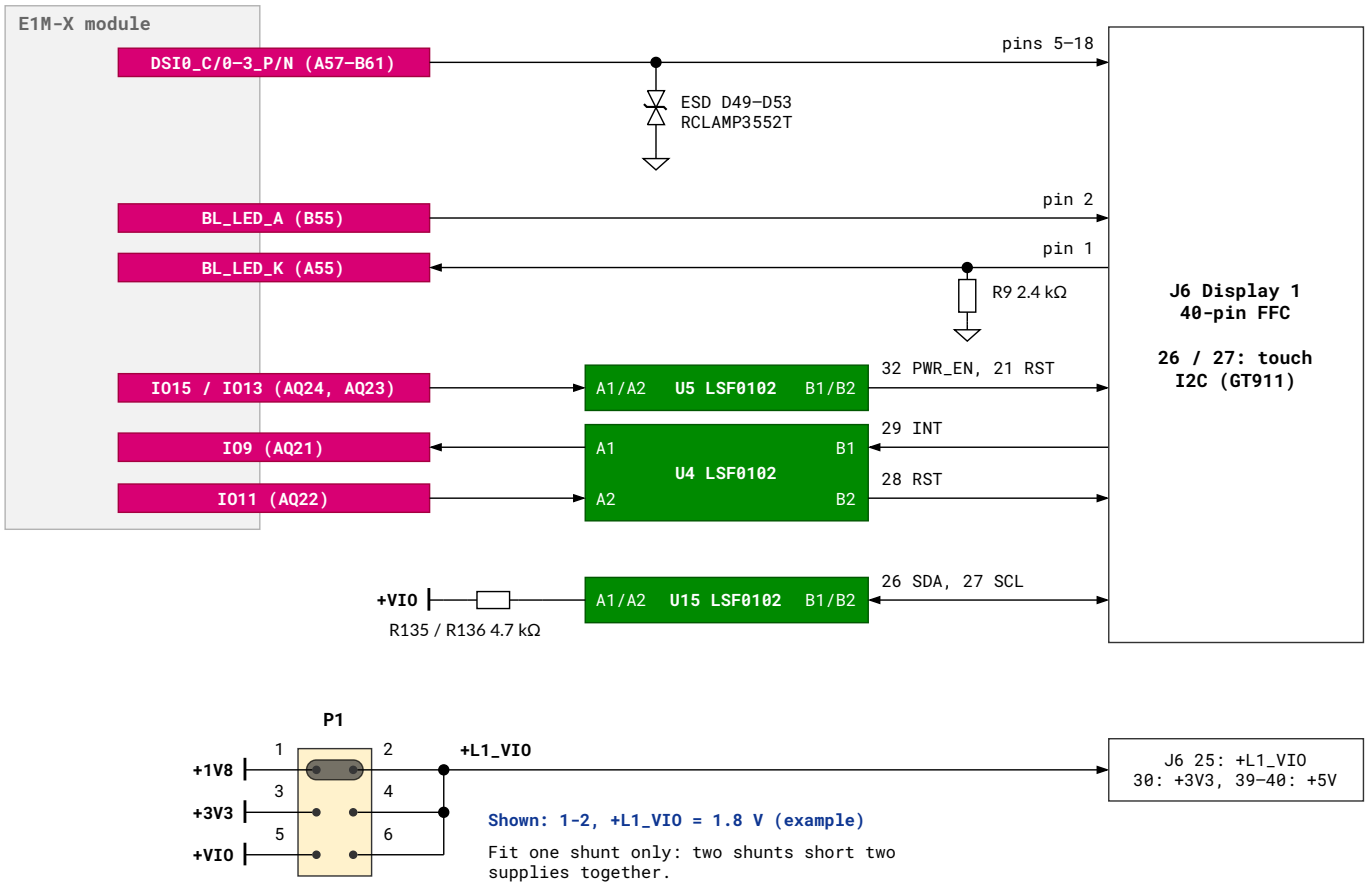
10 Display (MIPI DSI)

The V2N family has a **single** MIPI-DSI output. The E1M-X EVK carries two 40-pin DSI connectors, wired point-to-point (ESD clamps and LSF0102 level shifters only): Display 1 (J6) on the DSI0 lane set is the V2N-family display path; Display 2 (J28) on the DSI1 lane set is wired for future dual-DSI SoMs and is **permanently unavailable** with V2N / V2N-M1 SoMs at this hardware revision. The ITE IT6162 MIPI-DSI ⟶ HDMI bridge is **not populated** on the E1M-X EVK.

Output	DSI port	Notes
Display 1 FFC (J6)	DSI0	Reference panel: Rocktech RK055HDMIPI4MA0 (5.5-inch, 720 × 1280, Himax HX8394-F), 2-lane MIPI-DSI. Its Goodix GT911 touch controller sits on the J6 display I^2C, which the X-EVK V2 carrier does not connect to any module bus (carrier fix needed), so touch is not reachable on this revision.
Display 2 FFC (J28)	DSI1	Unavailable with V2N / V2N-M1 SoMs (the SoM has no second DSI output).
HDMI Type-A	—	Not functional: the IT6162 bridge is not populated.

Table 7 Display outputs on the E1M-X EVK

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In the V2 netlist +L_VIO (REFB of U4 / U5 / U15 and the panel-side pull-ups) has no supply connection; R10 / R11 are not fitted. Display 2 (J28, DSI1 pads A49–B53) is wired the same way with U50 / U53 / U54 and P3 (+L2_VIO); its backlight driver U55 KTD2801 takes BL PWM from PWM4 (A5) and feedback R193 2.4 kΩ; its VIN net VCC_IN_5V has no supply connection. Not usable with V2N.

Figure 13 Display 1 (J6): DSI0, backlight, control level shifters and the panel I/O jumper P1

> **Note:** In the V2 netlist the net +L_VIO — the panel-side reference of the display level shifters U4, U5, U15, U50, U53, U54 and their pull-ups — has no supply connection, and the Display 2 backlight driver U55 input VCC_IN_5V has none either. Check your board revision before relying on the panel reset, power-enable and touch lines.

The on-module backlight driver is fed by BL_LED_A, BL_LED_K, and BL_PWM (see **DS-V2N-001 §7.7**). The backlight feedback resistor is sized per the requested LED current:

$$I_{\mathrm{LED}} = 95 \frac{\mathrm{mV}}{R_{\mathrm{FB}}}$$

11 Camera Interfaces

The V2N family routes **two** 4-lane MIPI CSI-2 interfaces (CSI0, CSI1).

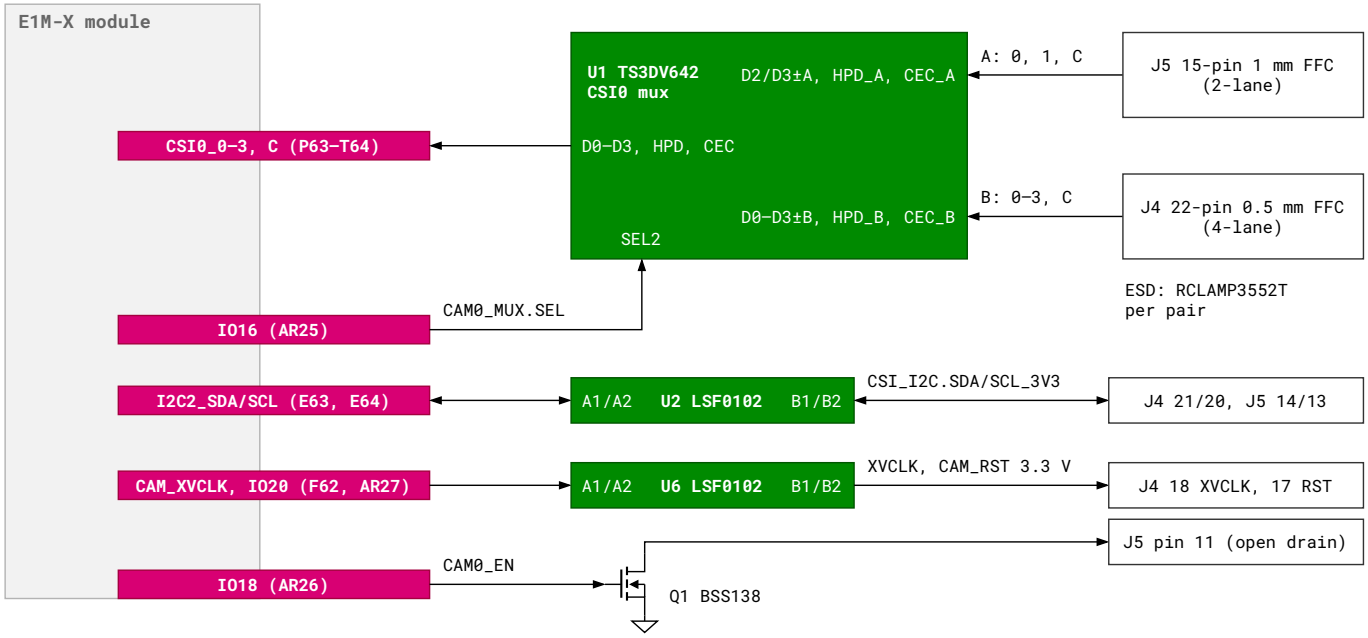
11.1 CSI0: 15-pin and 22-pin FFC

CSI0 goes through the TI TS3DV642 mux U1 (select: IO16, CAM0_MUX.SEL) to one of two FFC connectors:

- J5, 15-pin 1 mm (Raspberry Pi camera pinout): lanes 0 and 1 and the clock. Compatible with Raspberry Pi V2 / HQ cameras and most third-party RPi-pinout modules.
- J4, 22-pin 0.5 mm: all four lanes and the clock.

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Both share the camera I²C (I2C2, level-shifted to 3.3 V by U2); J4 also gets CAM_XVCLK and CAM0_RST at 3.3 V through U6, and J5 pin 11 is driven open-drain from CAM0_EN (IO18) by Q1. The on-module Mali-C55 ISP processes this stream.



J4 pin 22 and J5 pin 15: +3V3. U1 EN = +3V3; SEL1 pulled to +3V3 by R3 4.7 kΩ. I2C pull-ups: R7 / R51 4.7 kΩ to +3V3. CAM0_EN also reaches J22 pin 8 (R2 10 kΩ to GND). U1 port A carries lanes 0 and 1 and the clock only: CSI0 lanes 2 and 3 have no A-side connection.

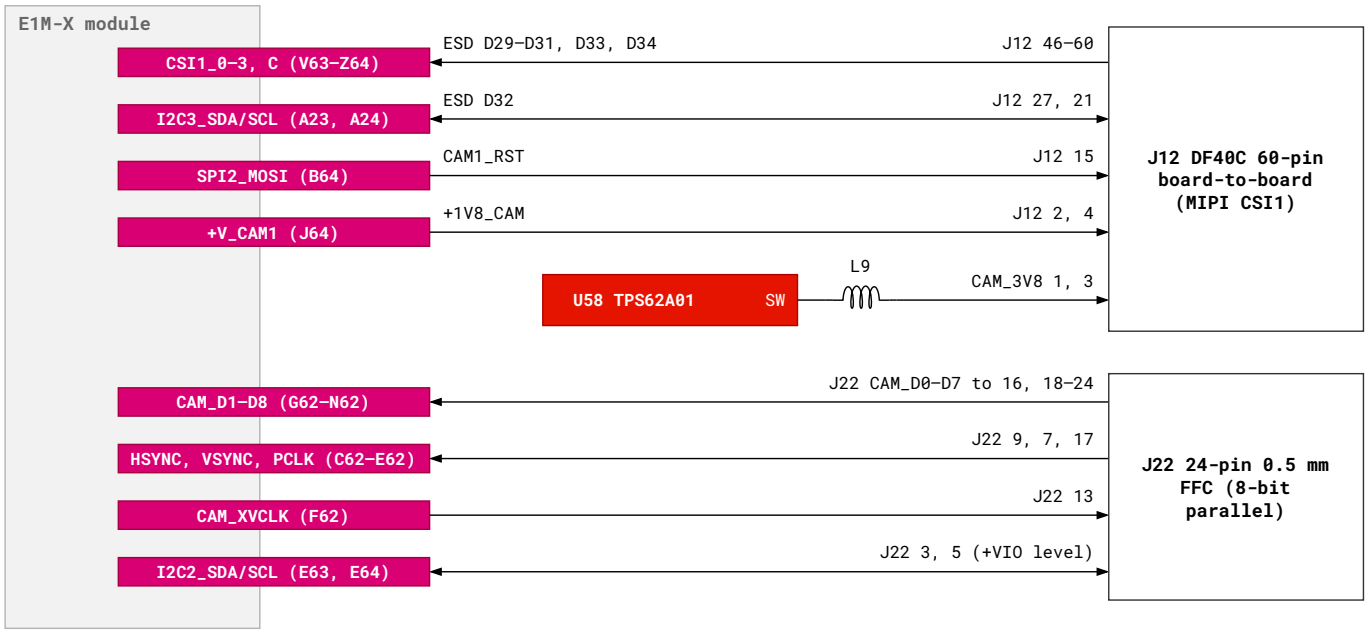
Figure 14 CSI0 camera path: mux U1, connectors J5 / J4 and their control lines

11.2 CSI1 and Parallel Camera

CSI1 is exposed on J12, a 60-pin Hirose DF40C board-to-board receptacle, with its I²C on I2C3, reset CAM1_RST on pad B64, +1V8_CAM from the module's +V_CAM1 and CAM_3V8 from the carrier buck U58.

An 8-bit parallel camera connects to J22 (24-pin 0.5 mm FFC): CAM_D0–CAM_D7 (pads CAM_D1–CAM_D8), HSYNC, VSYNC, PCLK, CAM_XVCLK and I2C2, with +2V6_CAM and +1V2_CAM from the module's +V_CAM2 / +V_CAM3 through the monitor shunts.

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J22 power: pin 4 +2V6_CAM (+V_CAM2 through R129), pin 10 +1V2_CAM (+V_CAM3 through R131), pin 11 +VIO. Pin 6 CAM_RST: R143 to +VIO only. Pad names CAM_D1–CAM_D8 carry the nets CAM_D0–CAM_D7. J12 SLAVEMODE0 / 1 (35, 36): R31 / R207 10 kΩ to +1V8_CAM. U58 VIN = EN = +5V.

Figure 15 CSI1 connector J12 and parallel camera connector J22

11.3 Camera Switching, Rails, and Level Shifting

Per-camera LDOs (+V_CAM0–+V_CAM3) are on the SoM. The feedback divider for each rail is placed on the **carrier** near the CAM_VFBx pin:

$$V_{\mathrm{CAM}} = 0.6\ \mathrm{V} \times \left(1 + \frac{R_1}{R_2}\right)$$

EMI and ESD protection on the MIPI CSI lanes is on-module; the carrier also fits Semtech RCLAMP3552T clamps on each CSI pair.

12 PCIe and M.2 Expansion

The V2N family has a single PCIe Gen3 × 2 controller (PCIE0_*). On the module it passes through on-module PCIe lane switches. On V2N-M1 modules they connect the controller either to the on-module DeepX DX-M1 or to the PCIE0 pads; software selects at runtime (see **HG-V2N-M1-001 §6.7**). On V2N modules they connect it to the PCIE0 pads.

12.1 M.2 Key M

A 2280 M.2 Key M slot (J23) accepts NVMe SSDs up to PCIe Gen3 × 2 (≈1.6 GB/s sustained). The carrier routes PCIE0 lanes 0–3 to it through four Diodes PI3DBS12212A 2:1 lane muxes (U36, U42, U43, U49); the RZ/V2N uses two lanes. Active only when:

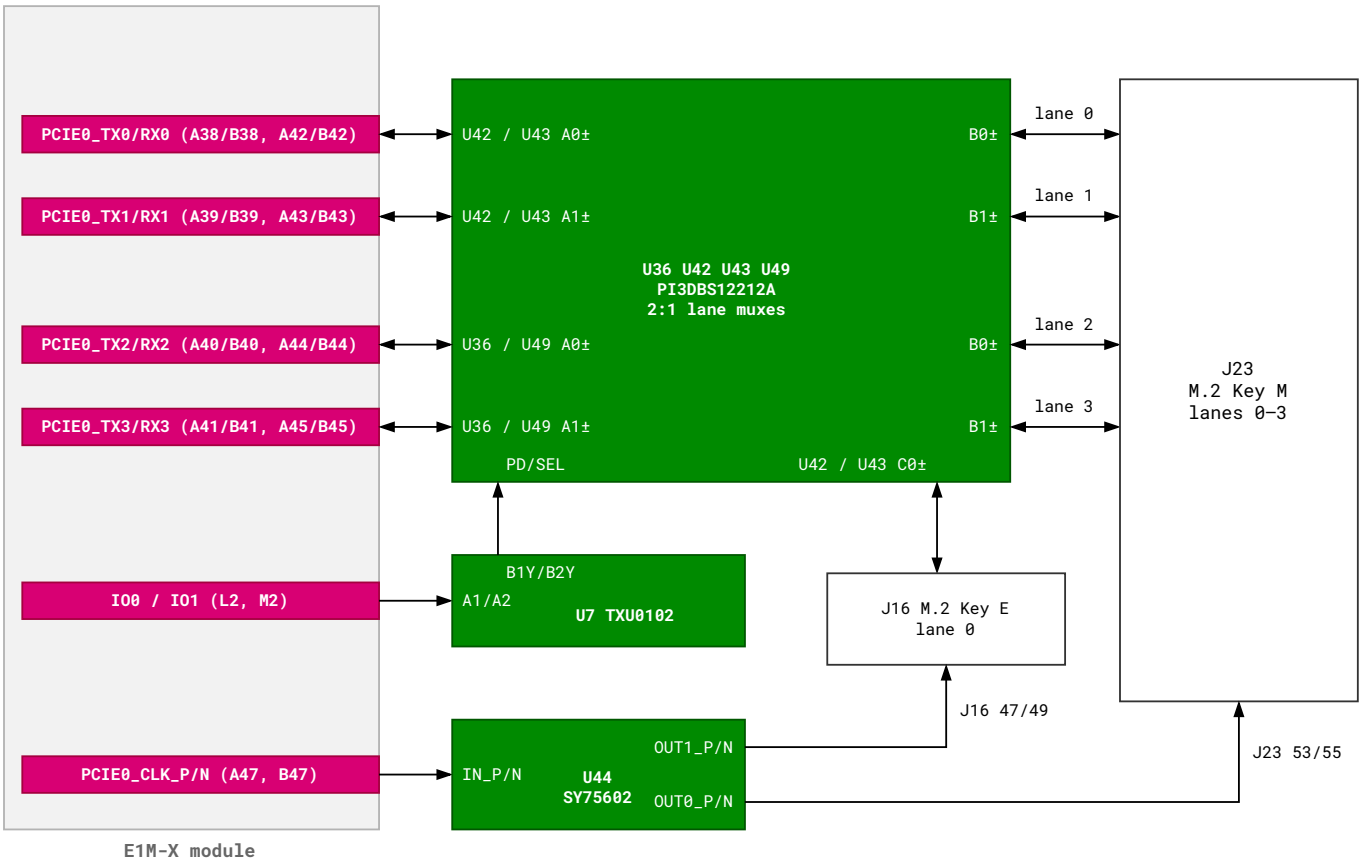
- On a V2N module: when the muxes are enabled and select the slot. Lanes 0–3 reach J23 only through the muxes' B side; their power-down input PD (net PCIe.MUX_PD_L) is pulled to +3V3 by R154 (10 kΩ) and SEL (PCIe.MUX_SEL_L) to GND by R155 (10 kΩ), and the module drives both through U7 (TXU0102) from IO0 / IO1. U7 does not invert, so PD follows IO0 and SEL follows IO1. PD is active-high (high = all switches Hi-Z): at power-up the pull-up keeps all four muxes off until the module drives IO0 low. With PD low, SEL low (the R155 default, IO1 low) connects the A side to B, which is the J23 path; SEL high (IO1 high) connects A to C, the M.2 Key E side, and disconnects J23.
- On a V2N-M1 module: when the on-module lane switches select the PCIE0 pads (M.2) and the DX-M1 rails are up (the slot reference clock runs only then; see PCIe Reference Clock and Switching), and the EVK lane muxes are enabled and select the slot (IO0 low, IO1 low; on V2N-M1 these pads are the DX-M1 GPIOs GPIO00_15 / GPIO00_13, so the DX-M1 firmware drives them; to be confirmed). When the lane switches select the on-module DX-M1, this slot is inactive.

The slot is powered from the carrier's protected 3.3 V rail.

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12.2 M.2 Key E

A 2230 M.2 Key E slot (J16) accepts Wi-Fi / cellular / co-processor cards on a 1-lane PCIe Gen3 link. The lane muxes give lane 0 either to J23 or to J16: the module drives IO1 (PCIe.MUX_SEL, pulled low by R155) and IO0 (PCIe.MUX_PD, pulled high by R154) through the level shifter U7. Key E also receives USB2 (through U47), SDIO (through U38 / U39) and I2S0 (through U46); its UART goes only to header P13.



All four muxes switch together (PD and SEL from U7). PD: R154 10 kΩ to +3V3; SEL: R155 10 kΩ to GND.

Default: PD high = all switches Hi-Z until the module drives IO0 low. Then IO1 low = B (J23), IO1 high = C (J16).

Key E uses only lane 0: with the C side selected, J23 lane 0 is disconnected. Mux and buffer supply: +3V3.

PCIE0_CLK comes from the module: on-module clock generator (DIFF1) and reference-clock buffer.

V2N-M1: on-module lane switches select the DX-M1 or PCIE0; PCIE0_CLK runs only with the DX-M1 rails up.

Figure 16 PCIe lane muxes and reference-clock buffer for the M.2 slots

12.3 PCIe Reference Clock and Switching

The PCIe reference clock comes from the module: the on-module clock generator (output DIFF1) drives the PCIE0_CLK_P / PCIE0_CLK_N pads (A47 / B47) through the on-module reference-clock buffer. The RZ/V2N root complex uses a second output (DIFF2) of the same clock generator, so the link runs with a common clock. The carrier does not add a clock source and must not add a second one. On the EVK the PCIE0_CLK_P / PCIE0_CLK_N pair feeds the Microchip SY75602 1:2 clock buffer U44, which drives both M.2 slots.

On a V2N-M1 module the DX-M1 takes its reference clock from the same DIFF1 output. The firmware enables DIFF1 only while the DX-M1 rails are up, so on a V2N-M1 neither M.2 slot has a reference clock while the DX-M1 is powered down.

> **Warning:** Hardware-damage hazard (V2N-M1). The on-module reference-clock buffer has no output enable. Enable DIFF1 (clock generator, I^2C 0x69) only while the DX-M1 rails are up; otherwise the buffer drives the unpowered DX-M1 reference-clock input.

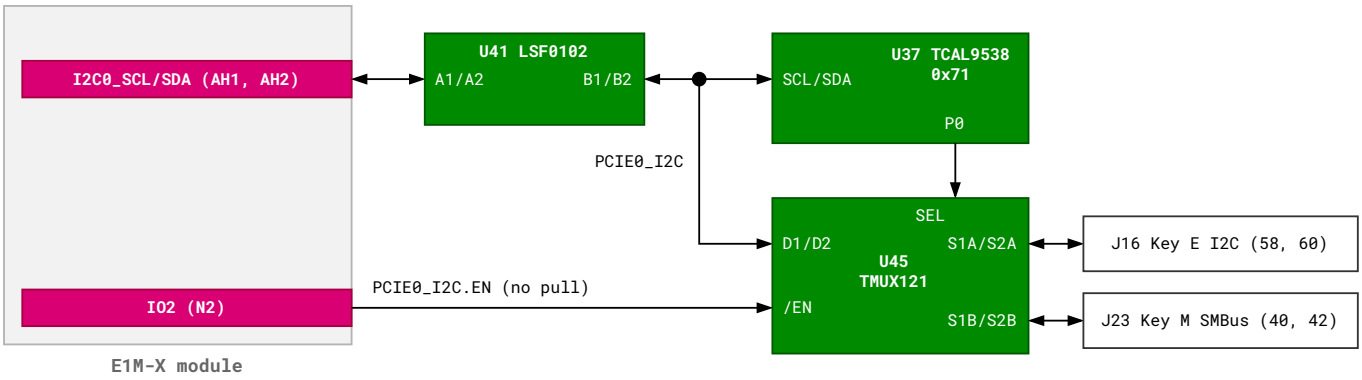
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12.4 PCIe I/O Expander

A Texas Instruments TCAL9538 8-bit I/O expander (U37) answers at 0x71 (A1 low, A0 high). It sits on the PCIe I²C segment (PCIE0_I2C), which an LSF0102 level shifter joins to alp_i2c0. Port map (from the design data; not yet bench-verified):

- P0 — select for the TI TMUX121 PCIe / M.2 I²C switch (E-key or M-key slot).
- P1 — M.2 Key E alert.
- P2–P4 — M.2 Key E reset / wake / clock request.
- P5–P7 — M.2 Key M reset / wake / clock request.

The TMUX121 enable input is active-low and its net has no pull resistor: drive XEVK_PIN_PCIE0_I2C_EN (E1M-X IO2) low to connect the M.2 slots, and never leave it floating. DX-M1 PCIe routing on V2N-M1 modules is on-module and is not controlled from this expander. The SDK driver is <alp/chips/tcal9538.h>.



U37 port map (PCIE0_I2C, 0x71)

P0	U45 SEL (Key E / Key M I2C)
P1	M2E_ALERT from J16 62
P2	E_PCIE0_RST to J16 52
P3	E_PCIE0_WAKE from J16 55 (R153)
P4	E_PCIE0_CLKREQ from J16 53
P5	M_PCIE0_RST to J23 50
P6	M_PCIE0_WAKE from J23 54 (R148)
P7	M_PCIE0_CLKREQ from J23 52

Other M.2 signals

UART TXD/RXD/RTS/CTS (22, 32, 34, 36) to P13 only

UART_WAKE (20) through U48 to IO6 (AL2)

SUSCLK (50) from RTC_CLKOUT (AQ16) through U48

W_DISABLE1/2 (56, 54): Q8 / Q9, gates pulled to GND (R158 / R159), drains pulled to +3V3: radios enabled

USB (3, 5) from U47 B side; SDIO from U38 / U39 B side

I2S (8–14) from U46 B side

SDIO_WAKE (21): R184 10 kΩ to +1V8 only

J23 LED (10): R151 470 Ω, D26 green to +3V3

Slot supply: +3V3 (both slots)

U37 /RESET and /INT: pulled up to +VIO, not wired to the module. U41 pull-ups on PCIE0_I2C: R161 / R162 10 kΩ to +3V3.

Figure 17 M.2 sideband signals: PCIe I²C segment, expander U37 port map and other slot signals

13 Audio

13.1 PDM Microphones

The V2N family routes 2 × PDM clock/data pairs (PDM_C0/D0, PDM_C1/D1), each supporting two microphones (stereo per PDM port). The carrier populates four Memsensing MSM261DHT006 microphones (U19, U20 on PDM0; U25, U26 on PDM1), one left and one right per pair by their L/R strap.

13.2 Amplifiers and Speaker Outputs

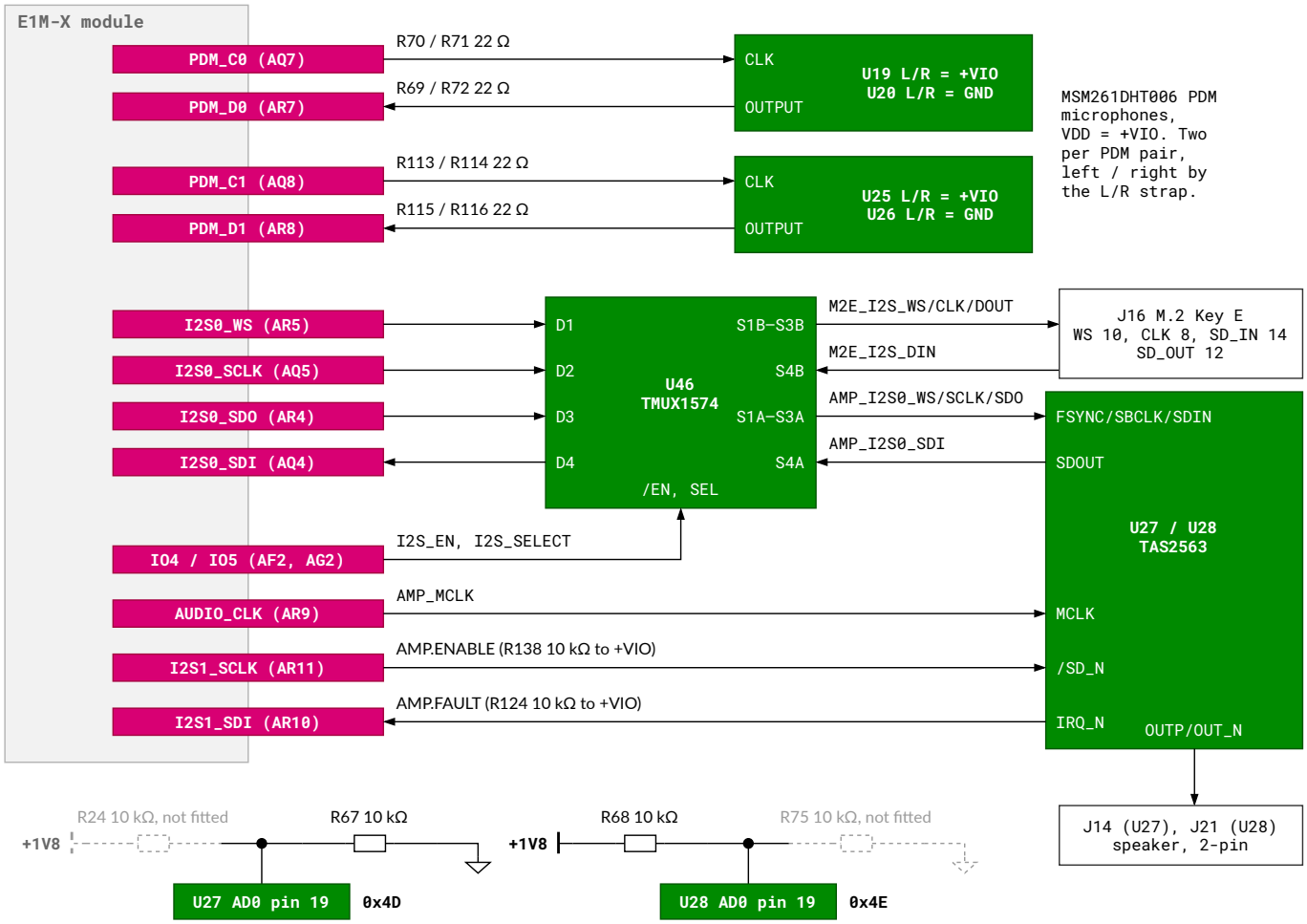
Two TI TAS2563 boosted class-D smart amplifiers form a stereo pair on alp_i2c0: U27 (left) and U28 (right), at 0x4D and 0x4E. The address pin AD0 (pin 19, TI name ADDR_SPICLK) selects 0x4C (GND), 0x4D (10 kΩ to GND), 0x4E (10 kΩ to VDD) or 0x4F

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(VDD). On the carrier R24 and R75 are not fitted: U27 AD0 has R67 (10 kΩ to GND) and answers at 0x4D; U28 AD0 has R68 (10 kΩ to +1V8) and answers at 0x4E. The SDK driver is <alp/chips/tas2563.h>; on Linux the kernel tas2562 codec driver owns them for ALSA.

13.3 I²S Routing

I2S0 carries playback to the amplifiers; an I²S path mux (TI TMUX1574) routes it either to the amplifiers or to the M.2 Key E slot (both control lines active-low; drive them low for the amplifiers). The I2S1 pads are used as plain GPIO for the amplifiers' shared shutdown and fault lines. No audio codec is populated (the RZ/V2N EVK's DA7212 is not fitted), so there is no capture path.



U46 VDD = +VIO. /EN and SEL are active low: drive both low for the amplifiers (A). Amplifier control: I2C0, U27 at 0x4D, U28 at 0x4E; both also answer the TAS2563 global address 0x48 (see I2C). TAS2563 VBAT = +5V (boost inductors L5 / L6 1 µH), VDD = +1V8, IOVDD = +VIO. No codec is fitted, so there is no analog capture path.

Figure 18 Audio: PDM microphones, I²S mux U46 and the TAS2563 amplifiers

14 Sensors and I/O Expansion

14.1 Sensor Devices

The E1M-X EVK populates the same sensor lineup as the E1M EVK:

Sensor	Function	Bus / address	Driver
TDK ICM-42670-P (U12)	6-axis IMU, primary	alp_i2c0 @ 0x69	<alp/chips/icm42670.h>

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Sensor	Function	Bus / address	Driver
Bosch BMI323 (U13)	6-axis IMU, alternate	`alp_i2c0` @ `0x68`	`<alp/chips/bmi323.h>`
Bosch BMP581 (U14)	Barometric pressure	`alp_i2c0` @ `0x47`	`<alp/chips/bmp581.h>`

Table 8 On-board sensors on the E1M-X EVK

The ICM-42670-P INT1 / INT2 / FSYNC and the BMP581 interrupt are on the main I/O expander (P4–P6 and P7); the BMI323 INT1 is on E1M-X `IO32` (`XEVK_PIN_BMI323_INT1`).

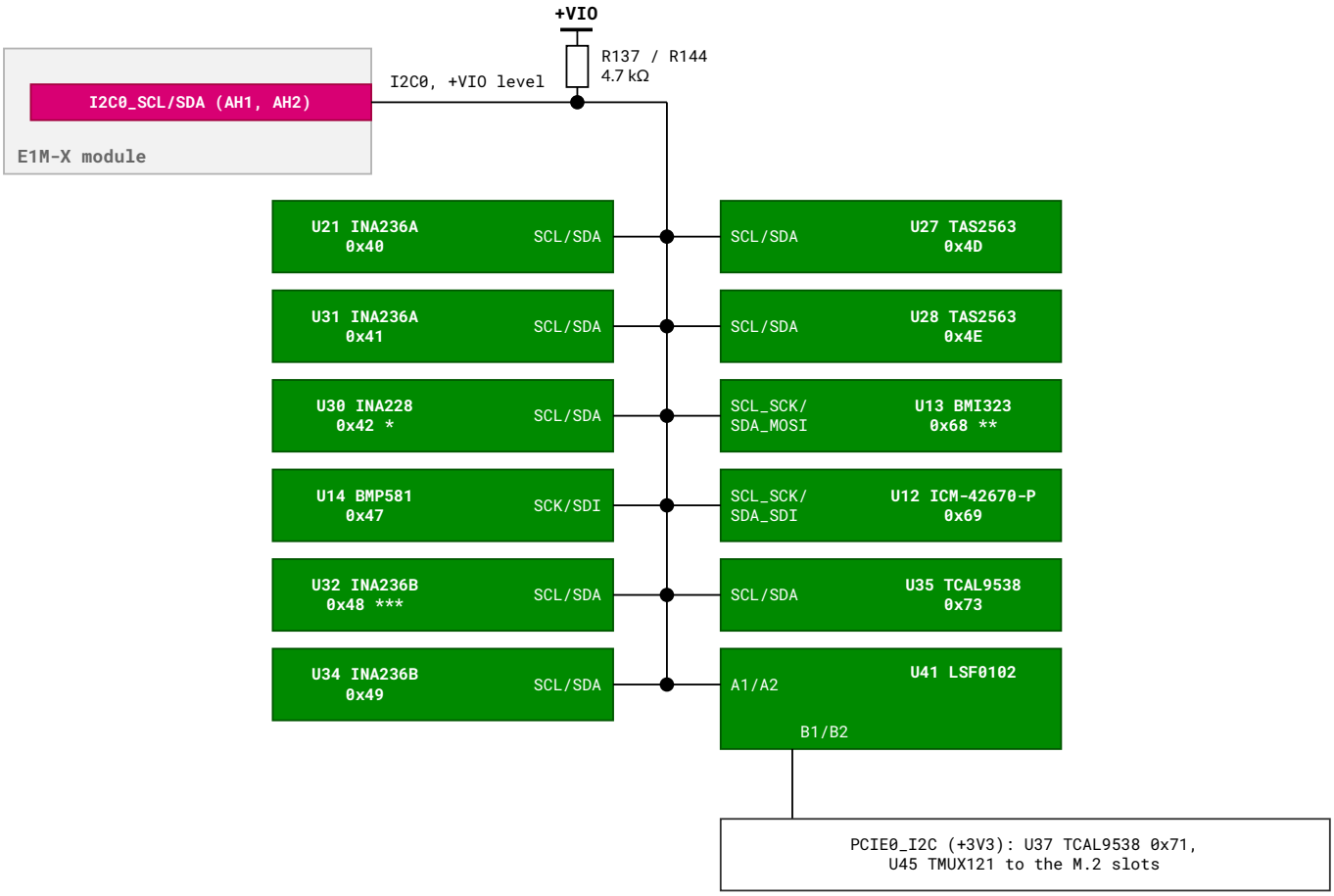
14.2 I²C Bus and Pullups

`alp_i2c0` is the EVK's primary sensor bus, routed from the SoM's `I2C0` pads and run at 100 kHz. Pull-ups: 4.7 kΩ to `+VIO`. Every fixed device on it (7-bit addresses):

Address	Device	Notes
`0x40`	INA236A (U21)	+3V3 rail monitor
`0x41`	INA236A (U31)	+1V8 rail monitor
`0x42`	INA228 (U30)	+5V input monitor; answers only on carriers with the bus-pin rework (see Current Measurement)
`0x47`	BMP581 (U14)	Barometer
`0x48`	INA236B (U32)	+V_CAM2 rail monitor, as built. Not readable: `0x48` is also the TAS2563 global address (U27 / U28). `0x4B` after the A0 rework (see Current Measurement)
`0x49`	INA236B (U34)	+V_CAM3 rail monitor
`0x4D`	TAS2563 (U27)	Left amplifier
`0x4E`	TAS2563 (U28)	Right amplifier
`0x50`, `0x58`	N24S128 identity EEPROM	On the SoM, not the carrier; `0x58` is its identity page
`0x68`	BMI323 (U13)	Alternate IMU
`0x69`	ICM-42670-P (U12)	Primary IMU
`0x71`	TCAL9538 (U37)	PCIe I/O expander (through a level shifter)
`0x73`	TCAL9538 (U35)	Main I/O expander

Table 9 Fixed devices on `alp_i2c0`

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On the module (not the carrier): N24S128 identity EEPROM at 0x50 / 0x58.
* U30 answers only after the SDA / SCL swap rework.
** The V2 netlist straps U13 SDO high (R47 to +VIO, R48 not fitted): 0x69, the address of U12.
*** 0x48 is also the TAS2563 global address (U27 / U28): U32 cannot be read as built.
Rework: U32 A0 (B1) from 0V to I2C0.SCL, address 0x4B.
Other buses: I2C1 (AQ47, AR47) to P15 only. I2C2 (E63, E64) to the cameras (J22 direct;
J4 / J5 through U2). I2C3 (A23, A24) to J12. The display touch I2C (U15 / U54) and the
mikroBUS I2C (U16) have no module-side connection.

Figure 19 `alp_i2c0` device map

> **Note:** In the V2 netlist the BMI323 (U13) address strap SDO is tied to +VIO (R47 fitted, R48 not fitted), which selects `0x69` — the address of the ICM-42670-P. The `0x68` above needs R48 fitted and R47 removed.

On Linux these parts are driven by the SDK's chip drivers over `/dev/i2c-0`, not by kernel drivers (the two TAS2563 amplifiers are the exception). A kernel driver bound to one of these addresses makes the SDK driver fail with `ALP_ERR_BUSY`.

A secondary I²C bus (`alp_i2c1`) exits the SoM on `I2C1` pads, runs at 400 kHz and is exposed on the 14-pin expansion header only. The mikroBUS socket's I²C sits behind its own level shifter whose module side is not wired to any E1M-X I²C bus on the X-EVK V2 (carrier fix needed), so a Click board's I²C is not reachable from the SoM on this revision.

14.3 I/O Expander

The main TI TCAL9538 I/O expander (U35) sits on `alp_i2c0` at `0x73` (A1 and A0 high) and carries the IMU and barometer interrupt lines listed above. Its ports P0–P3 have no other connection. Its reset and interrupt pins are pulled up on the carrier and do not reach the SoM. The SDK driver is `<alp/chips/tcal9538.h>`.

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15 Current Measurement (Power Profiling)

The E1M-X EVK carries four TI INA236 high-side current-shunt monitors and one TI INA228, all on `alp_i2c0`. INA236A parts occupy `0x40–0x43` and INA236B parts `0x48–0x4B`, selected by the A0 strap.

Address	Designator	Part	Rail	Shunt / full scale
`0x40`	U21	INA236A	+3V3	20 mΩ, 4.0 A max (A0 = GND)
`0x41`	U31	INA236A	+1V8	20 mΩ, 4.0 A max (A0 = V+)
`0x48` as built, `0x4B` after rework	U32	INA236B	+V_CAM2	50 mΩ (R129), 1.6 A max (A0 = GND; A0 = SCL after rework)
`0x49`	U34	INA236B	+V_CAM3	50 mΩ, 1.6 A max (A0 = V+)
`0x42`	U30	INA228	+5V input	100 mΩ, 1.6384 A shunt full scale at the board-default ±163.84 mV range (A1 = GND, A0 = SDA)

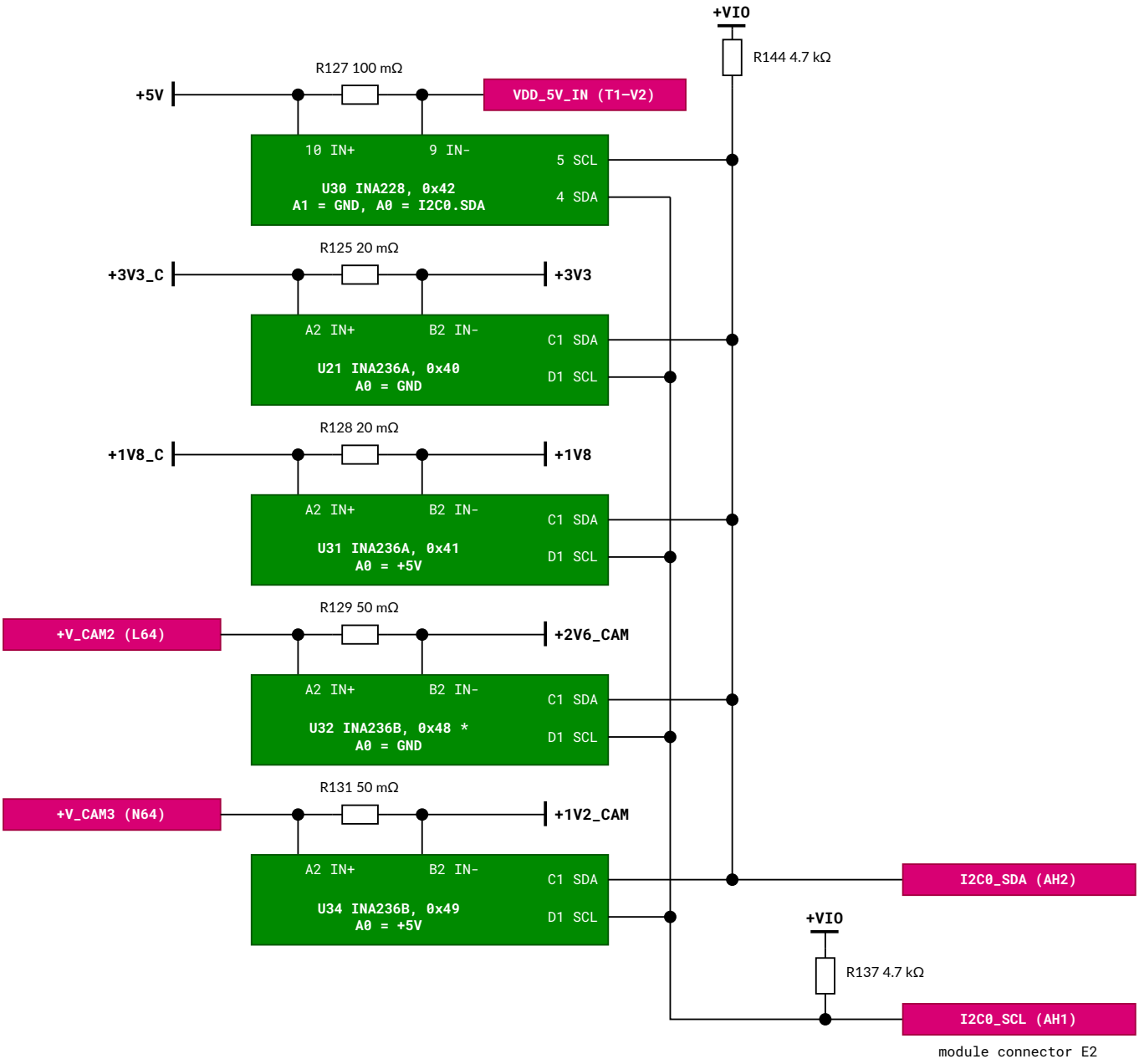
Table 10 Current monitors on the E1M-X EVK (`alp_i2c0`)

- The `+V_CAM2` monitor U32 measures the current from the module's `+V_CAM2` pad (`L64`) into `+2V6_CAM`. The SDK board header (`<alp/boards/alp_e1m_x_evk_routes.h>`) has no address macro for it: it is at `0x48` as built (not readable, see the warning below) and at `0x4B` after the rework.
- U30 (INA228) is not register-compatible with the INA236. On the X-EVK V2 its I^2C pins are swapped in the design and corrected by a hand rework; it answers only on carriers with that rework, so no answer at `0x42` means "part absent", not a fault.
- The alert pins are not connected.

Warning: As built, U32 cannot be read. Its A0 pin (B1) is on `0V`, which puts it at `0x48`, and `0x48` is also the global address of the TAS2563 amplifiers U27 / U28. They answer it while `I2C_GBL_EN` (`MISC_CFG2`, page `0x00`, register `0x05`, bit 1) is set, which is its reset default, and their `SD_N` pins (net `AMP.ENABLE`) are pulled to `+VIO` by R138, so they answer from power-up. A transfer to `0x48` reaches U32 and both amplifiers at once, so no U32 reading at `0x48` can be trusted. Rework: move the U32 A0 strap (pin B1) from `0V` to `I2C0.SCL`; U32 then answers at `0x4B` (INA236B, A0 = SCL), as on the E1M EVK. U32 is a DSBGA package, so its A0 ball is under the part.

These assignments are specific to the E1M-X EVK and differ from the E1M EVK (UG-E1M-001). The SDK drivers are `<alp/chips/ina236.h>` and `<alp/chips/ina228.h>`; the board macros (`XEVK_I2C_ADDR_INA236_*`, `XEVK_I2C_ADDR_INA228_5V`, shunt and full-scale values) are in `<alp/boards/alp_e1m_x_evk_routes.h>`. The `examples/v2n/v2n-power-monitor` example prints a live per-rail power table from Linux on the A55.

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INA236A answers at 0x40–0x43, INA236B at 0x48–0x4B (A0 strap). VS of every monitor = +5V;
ALERT pins not connected. U30 SDA (4) / SCL (5) are swapped in the design (hand rework).
* 0x48 is also the TAS2563 global address (U27 / U28): U32 cannot be read as built.
Rework: U32 A0 (B1) from 0V to I2C0.SCL, address 0x4B.
I2C0 also reaches U12, U13, U14, U35, U41 and U27 / U28 (see the I2C figure).

Figure 20 Per-rail current monitors on the E1M-X EVK

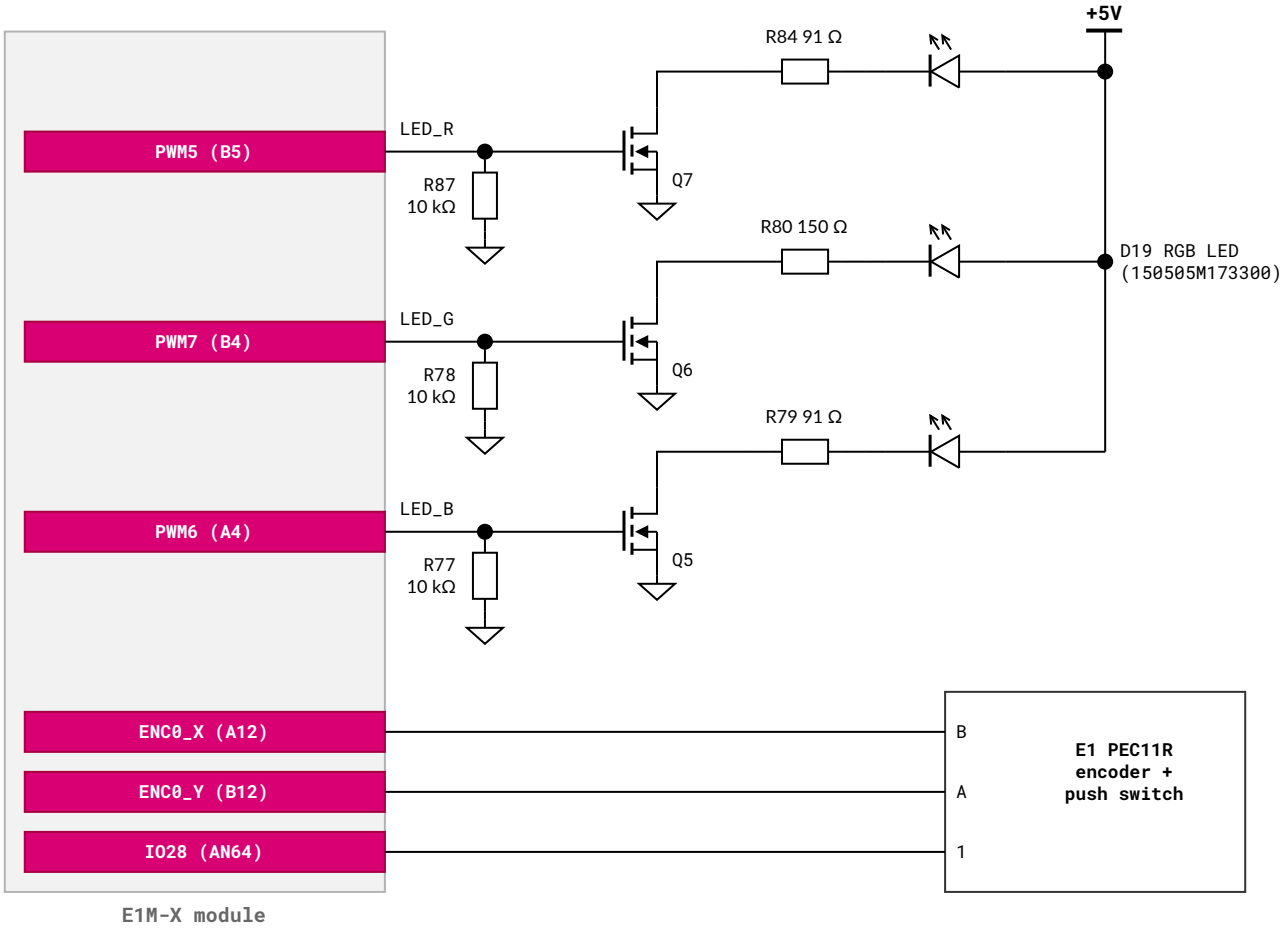
16 User Interface

The user-interface parts of the carrier:

- RGB LED D19 (anodes on +5V), driven by PWM5 (red), PWM7 (green) and PWM6 (blue) through BSS138 transistors Q7, Q6, Q5.
- Rotary encoder E1 (Bourns PEC11R, 24 detents) with push switch: ENC0_X, ENC0_Y and IO28 (ENC_SW), each pulled up to +VIO by 10 kΩ.
- Reset push-button S1 (PORn) and boot DIP switch SW1 (BOOT0–BOOT3); see Boot, Reset, and Debug.
- Status LEDs:

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- D3 (green) — +5V power-good (5V_PG).
- D4 (yellow) — +3V3 power-good (3V3_PG).
- D9 (yellow) — +1V8 power-good (1V8_PG).
- D17 (yellow) — +VIO present (module VIO_OUT up).
- D8 (red) — VBUS present on USB-C J27.
- D26 (green) — M.2 Key M activity (J23 LED pin).



Pull-ups 10 kΩ to +VIO: R104 (ENC0_X), R103 (ENC0_Y), R92 (ENC_SW). E1 C (COM) and switch pin 2 to GND; C109 0.10 µF on ENC_SW.

Status LEDs (anode on the rail; series resistor 1 kΩ unless noted)

D3 green: +5V (Q3, 5V_PG)

D4 yellow: +3V3 (Q10, 3V3_PG)

D9 yellow: +1V8 (Q11, 1V8_PG)

D17 yellow: +VIO (R38 to GND)

D8 red: J27 VBUS (R29)

D26 green: M.2 Key M LED (R151 470 Ω)

Figure 21 RGB LED, encoder and status LEDs

17 Expansion

17.1 mikroBUS

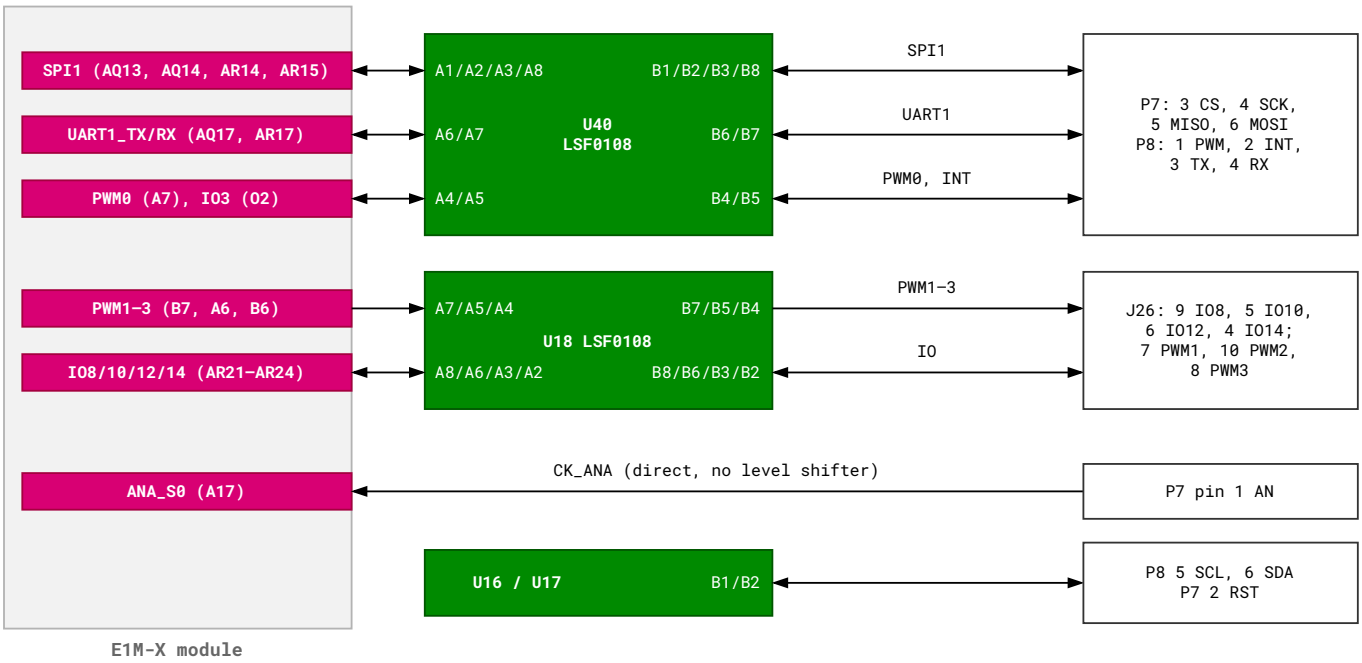
The mikroBUS click-board socket (P7 / P8) exposes, through the LSF0108 level shifter U40 at the +VOUT level set by jumper P9:

- SPI: SPI1_MOSI, SPI1_MISO, SPI1_SCLK, SPI1_CS0.
- UART: UART1_TX, UART1_RX.
- PWM: PWM0; INT: IO3.

- AN: ANA_S0, wired directly (no level shifter).
- I²C and RST: not reachable from the SoM on the X-EVK V2 (see **I²C Bus and Pullups**); the reset shifter U17 has no module-side connection either.
- 3V3 (P7 pin 7) and 5V (P8 pin 7).

Compatible with the full Mikroe click-board catalogue.

The 10-pin 2.54 mm socket J26 carries PWM1–PWM3 and IO8, IO10, IO12, IO14 through the LSF0108 U18, also at +VOUT.



B-side reference (mikroBUS / J26 level) = +VOUT, selected by P9 (+5V, +3V3 or +1V8); A side = +VIO.
Supplies: P7 pin 7 +3V3, P8 pin 7 +5V, pins 8 GND. J26 pin 1 +VOUT, pins 2–3 GND.
P8 I2C pull-ups R146 / R147 4.7 kΩ to +VOUT. U16 (I2C) and U17 (RST) have no module-side
connection on the V2 carrier: their A side carries only pull-ups.

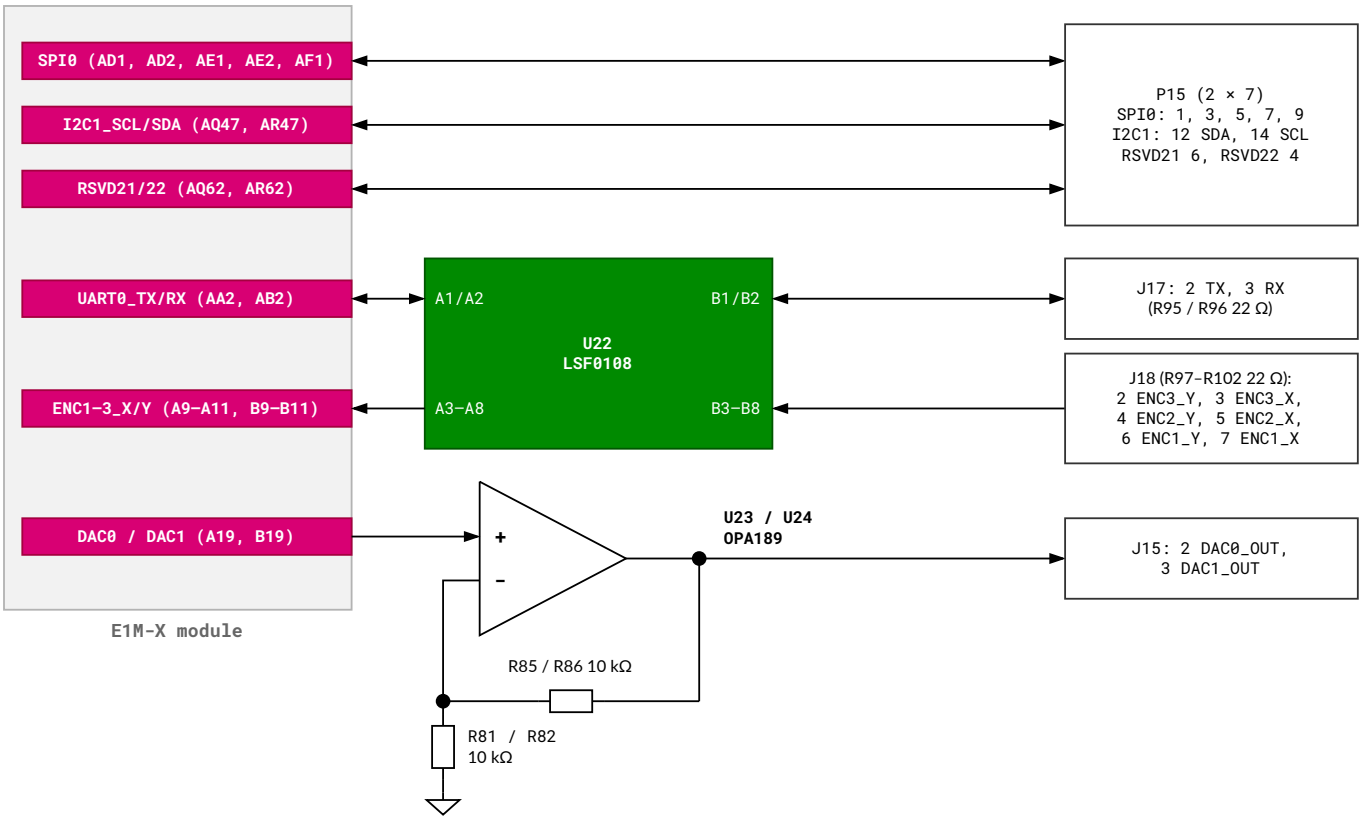
Figure 22 mikroBUS sockets P7 / P8 and socket J26

> **Note:** The E1M-X EVK **does not** carry the Arduino UNO R3 header that the smaller E1M EVK exposes. If Arduino-shield compatibility is required for prototyping, use the E1M EVK or build a custom carrier.

17.2 Expansion Headers

- P15 (2 × 7): SPI0, I2C1 and the RSVD21 / RSVD22 pads, +VIO and GND.
- J17 (4-pin): UART0 through U22, at +VOUT.
- J18 (8-pin): quadrature encoders ENC1–ENC3 through U22, at +VOUT.
- J15 (4-pin): DAC0 / DAC1 buffered by the TI OPA189 amplifiers U23 / U24 (supply +VOUT).
- P4, P5 (2 × 7): the module's RSVD pads, DBG_TXD / DBG_RXD and supply pins. With the current V2N / V2N-M1 modules the row-62 pads AE62 and AL62–AP62 are not connected on the module (see Module Control Pads).
- P16 (I3C): not fitted.

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J15, J17, J18 pin 1 = +VOUT (P9), last pin = GND. U23 / U24 run from +VOUT; feedback R81 / R85 and R82 / R86 (10 kΩ each). P15: pin 2 +VIO, pins 8, 10, 11, 13 GND. P4 / P5 (2 × 7) carry the RSVD pads, +5V, +VIO, +3V3 and DBG_TXD / DBG_RXD (P4 11 / 14). P16 (I3C) is not fitted. P13 carries the M.2 Key E UART only.

Figure 23 Expansion headers

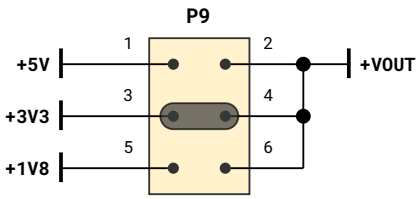
17.3 M.2 Key E (secondary)

See the **M.2 Key E** subsection under **PCIe and M.2 Expansion** above.

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18 Jumper Summary

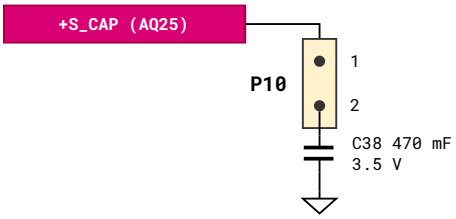
P9: +VOUT level



Shown: 3-4, +VOUT = +3V3

Feeds the mikroBUS / J26 level shifters, J15, J17, J18 and U23 / U24. Fit one shunt only.

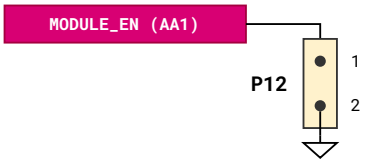
P10: +S_CAP backup store



Fitted: the supercapacitor C38 (FC0V474ZFTBR24) holds up +S_CAP.

Open: +S_CAP floats; keep the RTC trickle charger disabled.

P12: module enable



Normal use: open

Fitted: MODULE_EN low, module disabled.

Other jumpers on the carrier

P1 / P3: Display 1 / 2 panel I/O level (+L1_VIO / +L2_VIO): +1V8, +3V3 or +VIO. See Display.

P2: USB2_20_ID (G2) to GND: fitted = USB2 host. See USB.

P6: SDIO mux select (open: microSD, fitted: M.2 Key E). See microSD.

P11 / P14: J27 USB-C to U47 or the CP2102; CP2102 to DBG UART or UART0. See Debug.

P13: M.2 Key E UART (CTS, RTS, RXD, TXD). P4 / P5 / P15: expansion headers.

Figure 24 Supply and control jumpers P9, P10, P12 and the other carrier jumpers

19 Recommended Bring-Up Checklist

1. Check the boot straps: as shipped R108 (1 kΩ) is fitted and SW1 position 2 is closed, so BOOT1 = 0 and the other straps read 1 through the RZ/V2N internal pull-ups: Mode 1 (eMMC) with a CA55 boot (see Boot Mode Selection). Leave position 2 closed. The SDK's Cortex-M33 flash flow writes the image from the running Linux system, so Mode 3 (SCIF serial download) is not needed for it.
2. Fit P11 on 3-5 and 4-6 (J27 to the CP2102) and P14 on 1-3 and 2-4 (CP2102 to DBG_TX / DBG_RX). Connect J27 to your host; confirm one CP2102 virtual serial port enumerates.
3. Apply 12 V via the barrel jack J10 (preferred) or USB-PD on J11, not both.
4. Confirm D3 (green, +5V), D4 and D9 (yellow, +3V3 / +1V8) and D17 (yellow, +VIO) light.
5. Open the console at 115 200 8N1 and watch for the SoM boot banner.
6. For V2N-M1: after first Linux boot, verify the DX-M1 enumerates — `lspci` lists the DEEPX device.

20 Known Design Notes

- The IT6162 MIPI-DSI → HDMI bridge is not populated on the E1M-X EVK.
- The boot straps are sampled at PORn rising edge; changing them during runtime has no effect until the next reset.
- MODULE_STBY is not connected on the carrier.
- The SW1 option links other than R108 (R93 / R94, R105–R107, R109, R110) are not fitted. In the V2 netlist the +L_VIO supply and the U55 supply (VCC_IN_5V) are open; see the notes in the relevant sections.
- U32 (INA236B, +V_CAM2 monitor) is strapped to 0x48, which the TAS2563 amplifiers U27 / U28 also answer as their global address, so it cannot be read as built; the rework moves its A0 to I2C0.SCL (0x4B, see Current Measurement).
- As assembled, the bypass links R235–R238 are fitted and the transceiver links R227–R234 are not; with a V2N / V2N-M1 module (1.8 V logic-level CAN pads) swap them before connecting a bus (see CAN Bus).

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Note: Sections marked **TBD** will be filled in as the EVK schematic Rev. 1.0 is finalised. Questions or corrections about this guide: email contact@alplab.ai and mention UG-E1M-X-001.

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