E1M-X V2N — RENESAS RZ/V2N VISION-AI SOM

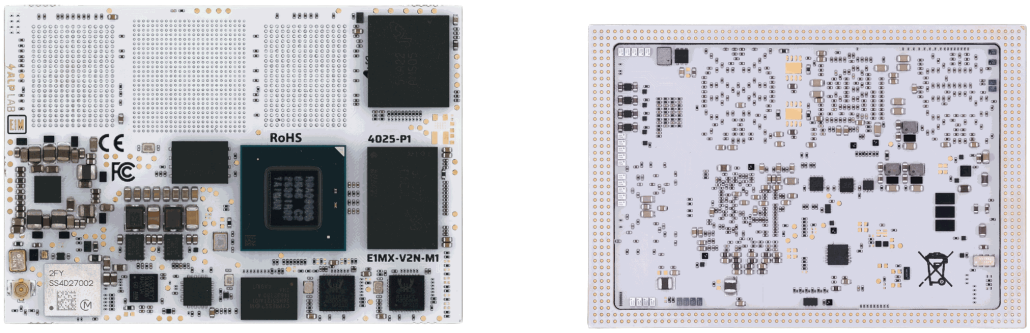


Figure 1 E1M-X V2N module — front (left) and back (right)

The E1M-X V2N module is built on the open E1M™ standard, with a unified pin layout and hardware functionality. This footprint allows users to interchange MPU modules seamlessly while keeping hardware compatible. E1M™ is designed for flexibility, functionality, and longevity in high- and medium-range MCU/MPUs.

Features

- **Renesas RZ/V2N**
  - Quad Arm® Cortex®-A55 (1.8 GHz)
  - Arm Cortex-M33 (200 MHz)
  - Arm Mali™-C55 ISP (Image Signal Processor)
  - Arm Mali™-G31 GPU
  - AI Accelerator DRP-AI3 — 4 dense TOPS
  - H.264 / H.265 codec
- **Dedicated I/O MCU**
  - Arm® Cortex®-M33 (216 MHz)
- **Various memory options**
  - LPDDR4X 32-bit 3.2 GT/s, up to 8 GB
  - eMMC — 4 GB to 256 GB
  - xSPI NOR flash – 512 Mbit, boot-supported
- **MIPI Display output** — 4 lanes
  - 1920 × 1200 RGB888 @ 60 fps
  - 1280 × 1024 RGB888 @ 120 fps
- **H.264 / H.265 codec**
  - H.264 1920 × 1080 × 60 fps
  - H.265 3840 × 2160p × 30 fps
- 2 × CSI-2 camera inputs — 4 lanes, up to 4K @ 30 fps, 4 virtual channels
- 2.4 GHz / 5 GHz / 6 GHz Wi-Fi® + Bluetooth® module
  - 802.11 a/b/g/n/ac/ax, 143 Mbps
  - Bluetooth® 5.4 BR/EDR/LE, 3 Mbps
- 2 × 1 Gbps Ethernet PHY
- 2 × CAN-BUS PHY
- PCIe Express® 3.0 — 2 lanes
- Assembly variants available for cost reduction
- Smallest size in the industry: 45 × 65 mm

Applications

IoT, industrial, robotics, motor drive, drones, mobile PoS, smart speakers, object detection, medical devices, vending machines, smart home, process control, smart appliances, scanners.

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1 General Description

1.1 Highlights

The Alp Lab E1M-X V2N SoM (System-on-Module) is a high-performance, cost-effective solution designed for a range of AI-driven vision applications. Powered by the Renesas RZ/V2N processor, it features an Arm® Quad Cortex®-A55 (1.8 GHz) CPU, an integrated AI accelerator, and a 4K encoder/decoder, making it optimised for vision-based tasks. The E1M-X V2N SoM supports up to two cameras via 2 × 4-lane MIPI CSI-2 connections and offers customisable options such as on-board Wi-Fi / Bluetooth, multiple memory and storage capacities, and PHY configurations.

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1.2 Block Diagram

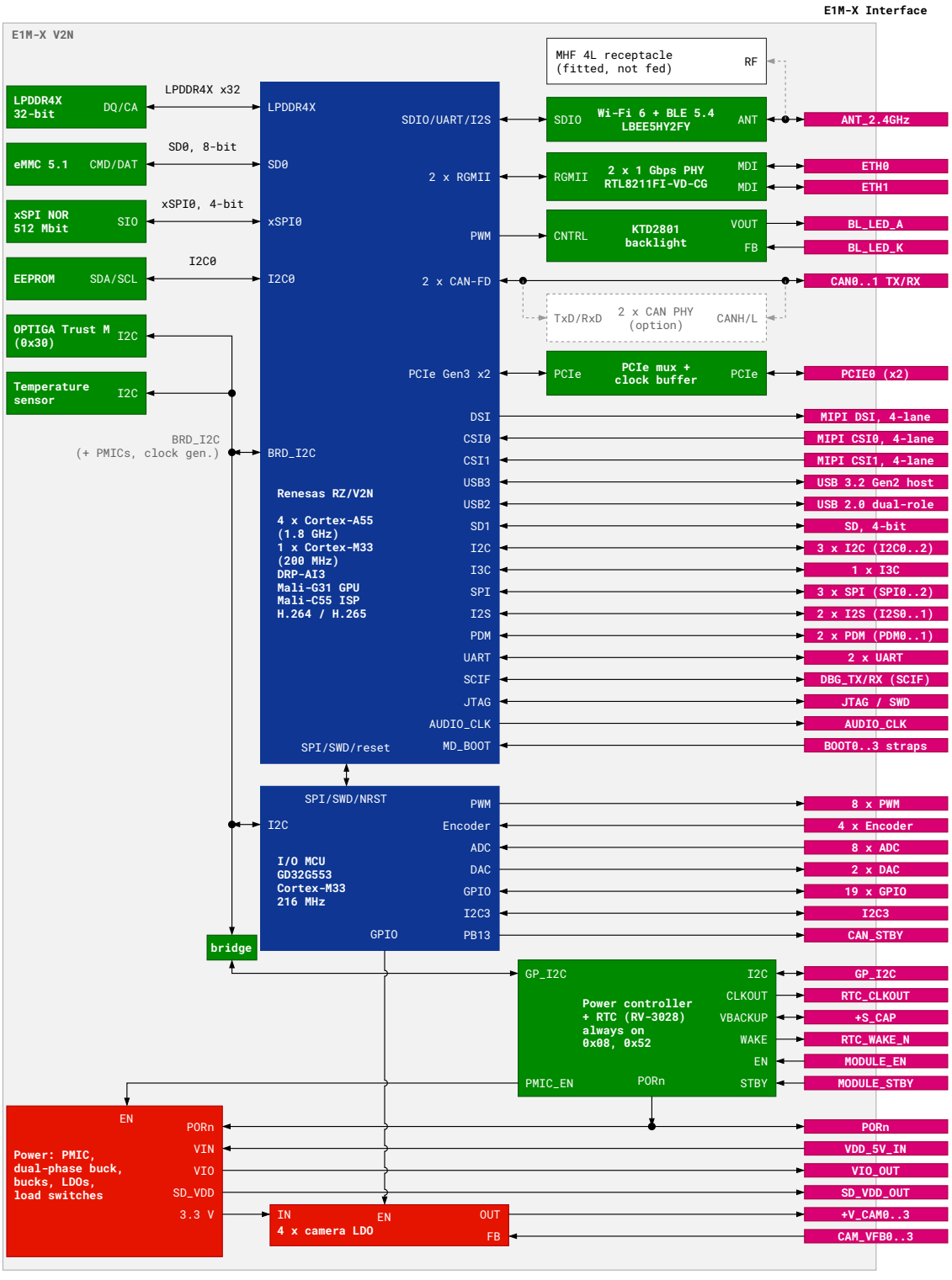


Figure 2 E1M-X V2N Block Diagram

1.3 Module Variants

The E1M-X V2N family ships in three MPN variants that share an identical pin-out and silicon stack; they differ only in the memory tier. See Section 15 for the full ordering matrix and MPN decoder.

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MPN	Renesas part	LPDDR4X	eMMC
E1M-V2N101	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 4 GB
E1M-V2N102	R9A09G056N44GBG#AC0	8 GB	eMMC 5.1, 16 GB
E1M-V2N103	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 16 GB

Table 1 E1M-X V2N Variant Summary

1.4 Renesas RZ/V2N MPU

The RZ/V2N is a vision-AI microprocessor (MPU) with Renesas' proprietary AI accelerator (DRP-AI3) supporting up to 15 TOPS of AI performance. Its CPUs are quad Arm® Cortex®-A55 (1.8 GHz) and Arm Cortex-M33 (200 MHz). The RZ/V2N is equipped with an ISP (Image Signal Processor) and dual-channel MIPI® CSI-2® camera interfaces for supporting dual-camera signal processing, which is crucial for realising vision systems. It is also equipped with high-speed interfaces such as PCIe® and USB 3.2, allowing for the expansion of external devices. The RZ/V2N is an ideal microprocessor for applications requiring both low power consumption and advanced AI inference, such as DMS (Driver Monitoring System), monitoring cameras, mobile robots, and more.

This document should be read together with the V2N datasheet from Renesas.

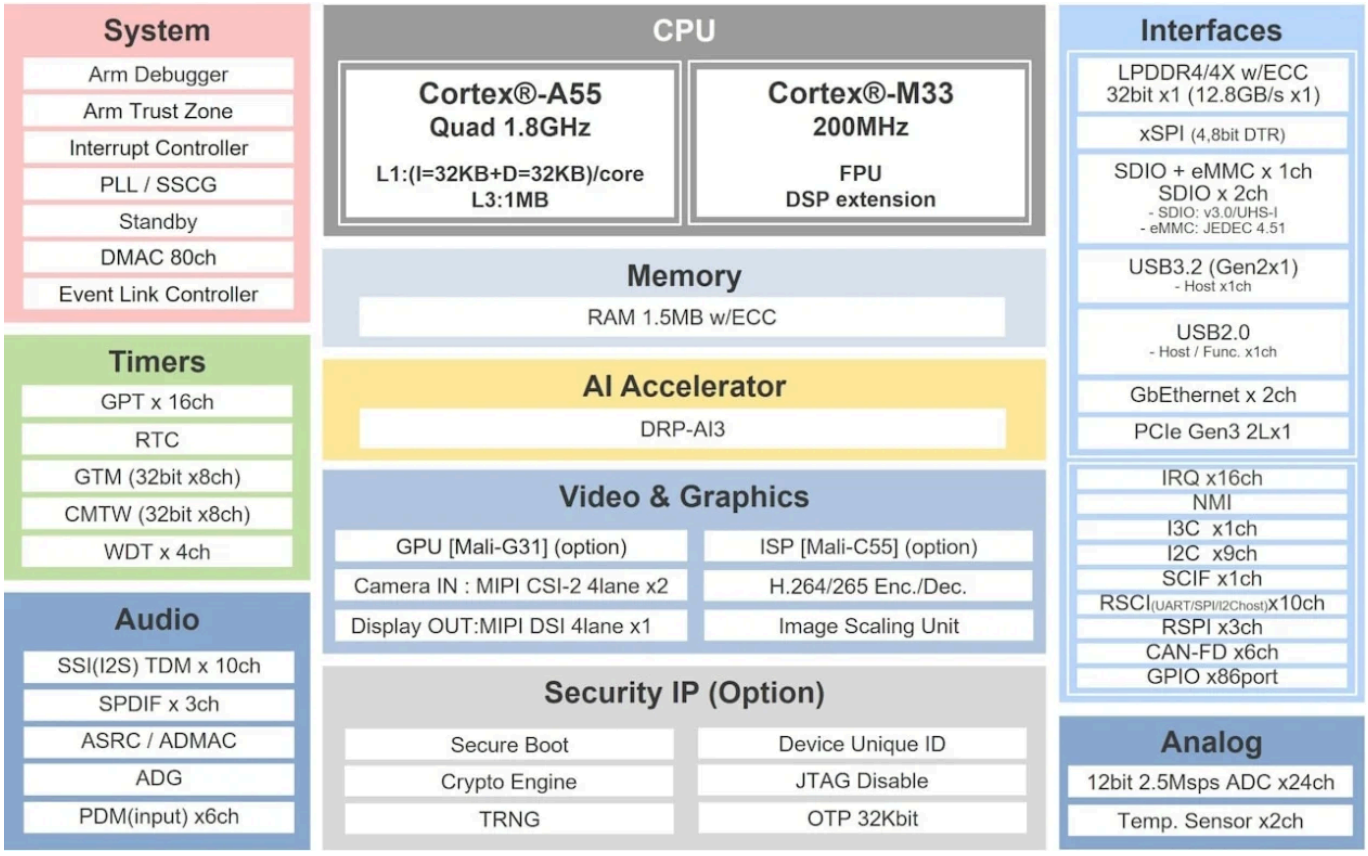


Figure 3 Renesas RZ/V2N MPU block diagram (source: Renesas Electronics)

Blocks marked (option) depend on the RZ/V2N part number; see Ordering Information.

Key MPU features:

- Cortex-A55 (1.8 GHz) × 4 cores
- Cortex-M33 (200 MHz) × 1 core
- AI Accelerator DRP-AI
- Arm Mali™-C55 ISP (option)
- 1.5 MB on-chip SRAM

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- LPDDR4 / LPDDR4X memory interface
- Gigabit Ethernet 2 ch
- USB 2.0 interface 1 ch (Host/Function)
- USB 3.2 (Gen2) interface 1 ch (Host only)
- PCIe interface (Gen3, 2-lane) 1 ch
- MIPI CSI-2 camera interface 2 ch
- CAN interface (CAN FD) 6 ch
- AD converter 24 ch

2 Pin Diagram and List

The E1M-X™ standard defines the primary pin functions; the pin-out below follows that standard. Pins can be reassigned to alternate functions in software, but hardware compatibility with other E1M-X variants will no longer hold because each MCU/MPU has a different pin structure and peripheral mapping.

The pin-out is drawn in the top view (component side up), landscape: 65 mm across and 45 mm down. A1 is the top-left corner pad, 1.0 mm from the left and top edges, at the pin-1 fiducial. The pad letters A–AR are the rows, running top to bottom; the pad numbers 1–64 are the columns, running left to right. A2 is directly to the right of A1 and B1 directly below it. The pad band is two pads deep at the top and bottom edges (rows A, B and AQ, AR) and three pads deep at the left and right edges (columns 1–3 and 62–64). This is the frame of the alplab.ai pinout viewer and of the original E1M-X pinout drawing. The map is split into four quarters so that every pad name stays legible.

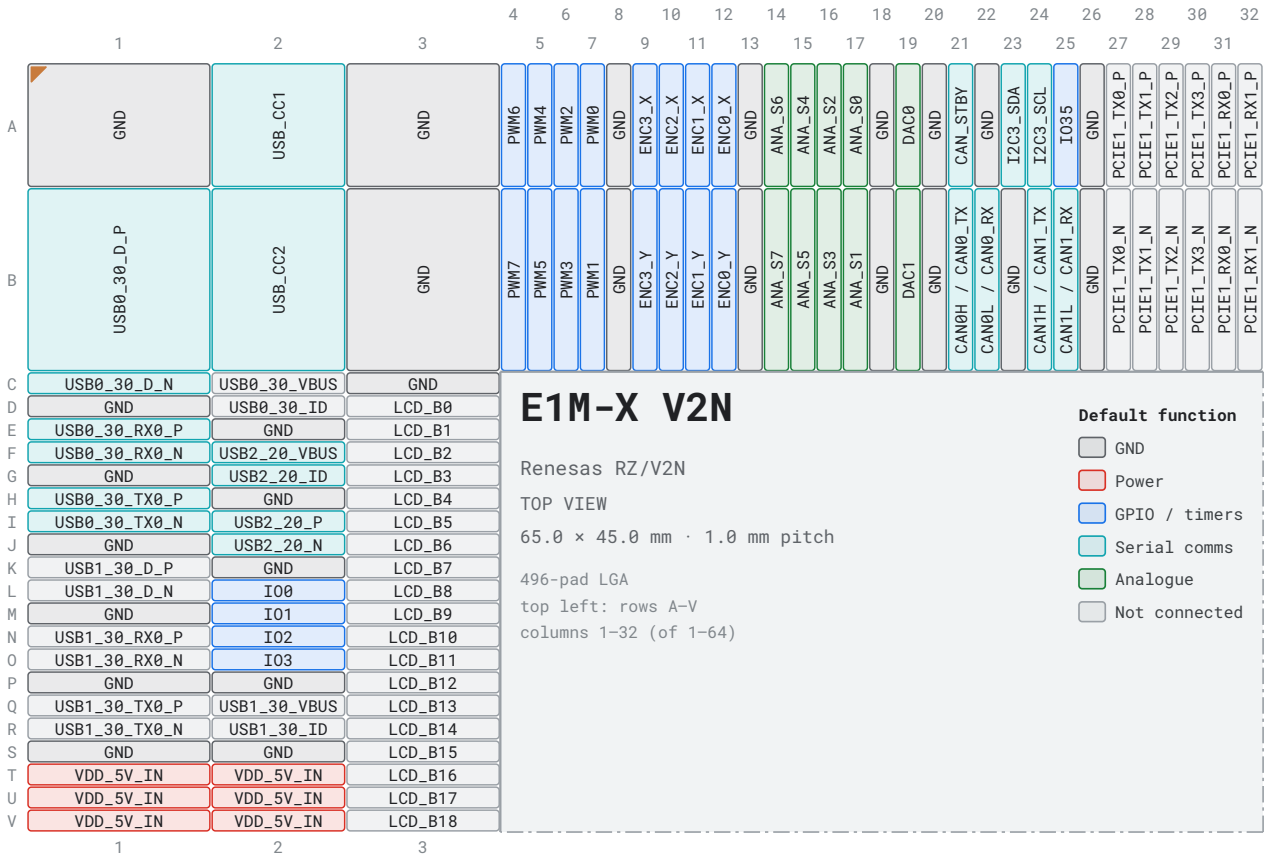


Figure 4 E1M-X V2N Pin-out (top view, 496-pad LGA), top left: rows A–V, columns 1–32

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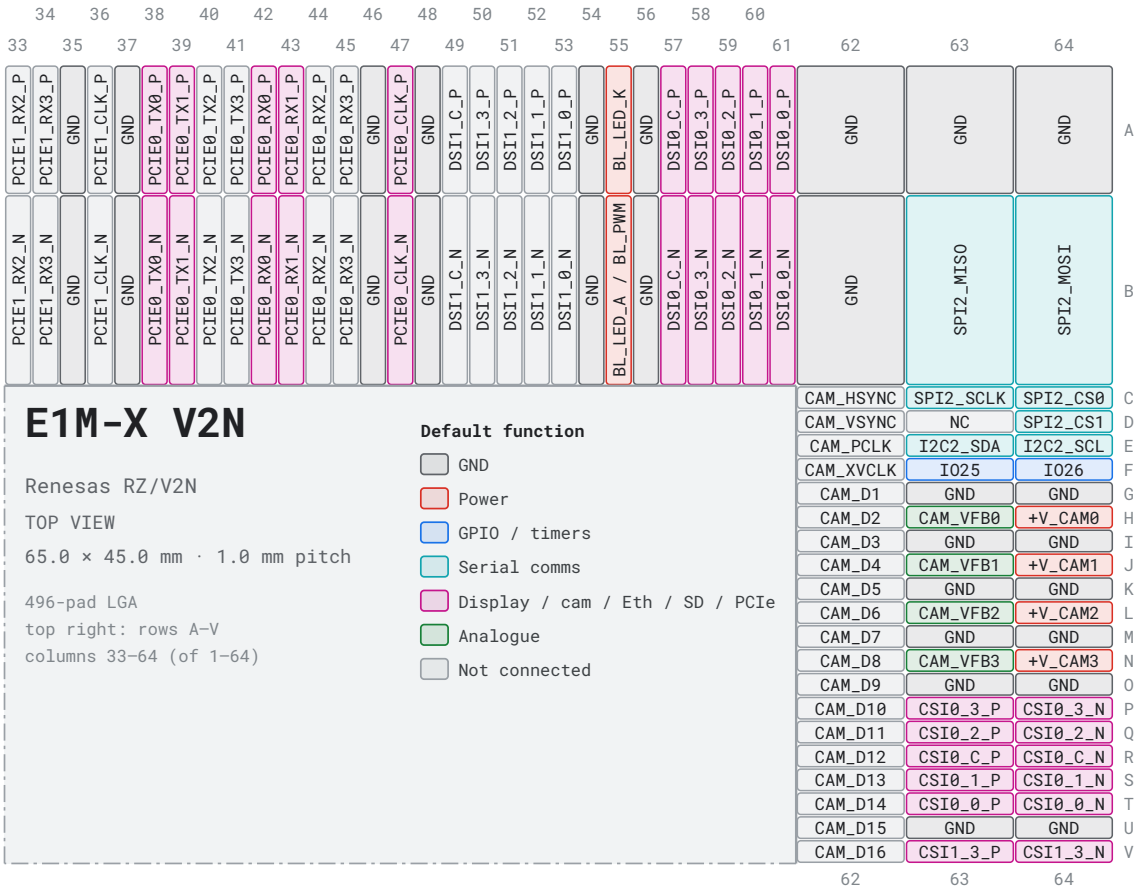


Figure 5 E1M-X V2N Pin-out (top view, 496-pad LGA), top right: rows A–V, columns 33–64

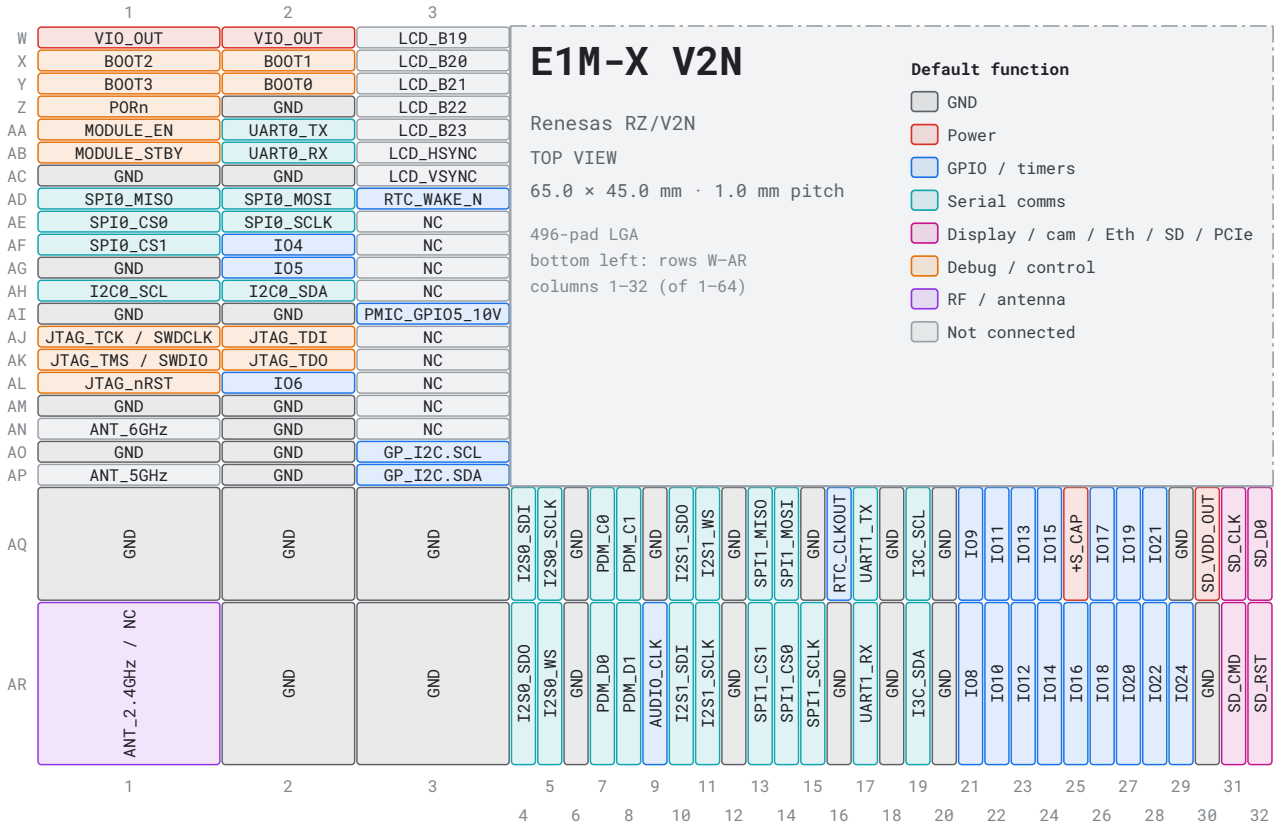


Figure 6 E1M-X V2N Pin-out (top view, 496-pad LGA), bottom left: rows W–AR, columns 1–32

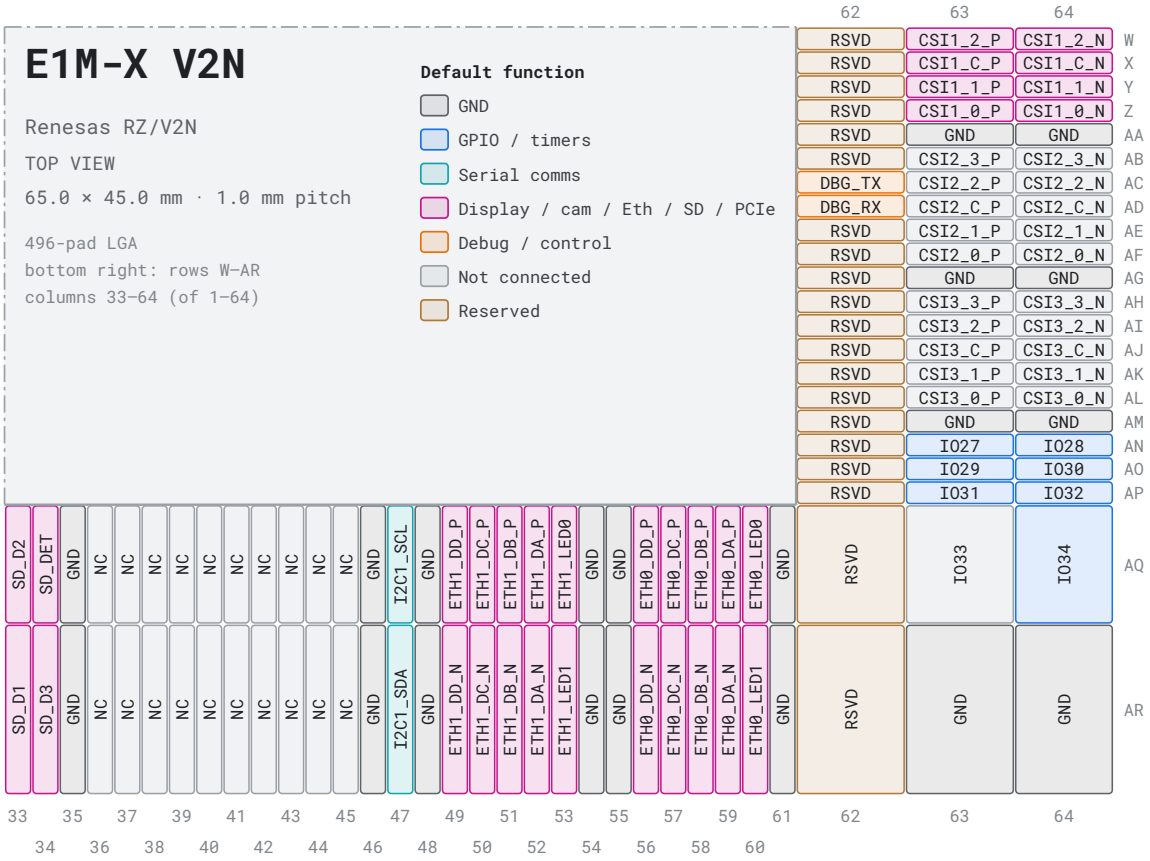


Figure 7 E1M-X V2N Pin-out (top view, 496-pad LGA), bottom right: rows W–AR, columns 33–64

2.1 Power & Control Pins

Pin Number	Pin Name	Description
A13, K63, AQ15, M1, M63, O63, A18, AQ18, P1, A20, AQ20, S1, A22, U63, A26, AA63, AQ29, AC1, AQ6, D1, A35, AG1, AG63, AQ35, A37, AI1, AM1, AM63, AO1, AQ1, A46, AQ46, AR63, A48, AQ48, A8, A54, AQ54, AQ55, A56, AQ61, A62, AQ9, G1, G63, I63, AQ12, J1, A1, A3, A63, AQ3, C3, K64, M64, O64, U64, AA64, AG64, AM64, AR64, G64, I64, A64, AR16, AR18, AR20, AR30, AR6, AR35, AR46, AR48, AR54, AR55, AR61, AR12, AR3, B13, K2, B18, P2, B20, S2, B23, B26, Z2, AC2, B35, AI2, B37, AM2, AN2, AO2, E2, AP2, AQ2, AR2, B46, B48, B8, B54, B56, B62, H2, B3	GND	Connect to ground.
W1, W2	VIO_OUT	+1V8 output for I/O power. Up to TBD mA.
T1, U1, V1, T2, U2, V2	VDD_5V_IN	+5 V main supply input to the module.
AQ25	+S_CAP	RTC backup supply input (external super-capacitor or backup cell). Connected directly to the backup input VBACKUP of the on-module RTC (RV-3028-C7);

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Pin Number	Pin Name	Description
		the module has no backup capacitor fitted. See Section 4.2.
Y2	BOOT0	Boot selection for Renesas RZ/V2N. Carrier strap: 1 kΩ pull-up to VIO_OUT for 1, 1 kΩ pull-down to GND for 0. See Section 4.5.
X2	BOOT1	Boot selection for Renesas RZ/V2N. Carrier strap: 1 kΩ pull-up to VIO_OUT for 1, 1 kΩ pull-down to GND for 0. See Section 4.5.
X1	BOOT2	Connected to the RZ/V2N MD_BOOT3 strap; no pull-up on the module. Fit a 1 kΩ pull-up to VIO_OUT on the carrier (BOOT2 = 1).
Y1	BOOT3	Boot CPU selection. High: RZ/V2N internal CA55 boot. Low: RZ/V2N internal CM33 boot. Carrier strap: 1 kΩ pull-up to VIO_OUT for CA55 boot (BOOT3 = 1), 1 kΩ pull-down to GND for CM33 boot (BOOT3 = 0). On the module also tied to the PMIC GPIO5 through an on-module 0 Ω link, and so to pad AI3 (PMIC_GPIO5_10V); the PMIC GPIO5 is an input (high impedance).
AL1	JTAG_nRST	JTAG / SWD pins for programming and debug.
AJ1	JTAG_TCK / SWDCLK	
AJ2	JTAG_TDI	
AK2	JTAG_TDO	
AK1	JTAG_TMS / SWDIO	
AA1	MODULE_EN	Module enable input. Through an on-module PMX100UNZ clamp (gate +1V8_AON) to the power controller; 1 MΩ pull-up to +1V8_AON on the module. The carrier may use an open-drain output with no pull-up, a switch to GND, or push-pull logic from 1.8 V to 5 V. Pull low to switch the module off; leave floating if not used. See Section 6.
Z1	PORn	RZ/V2N reset. Open drain at 1.8 V: driven by the PMIC reset output and by the power controller, 10 kΩ pull-up to the module 1.8 V rail VDD1G_1P8. The carrier may pull it low to reset the RZ/V2N with the rails up; no carrier pull-up. Leave floating if not used.
AB1	MODULE_STBY	Standby and wake request (low pulse). Through an on-module PMX100UNZ clamp (gate +1V8_AON) to the power controller; 1 MΩ pull-up to +1V8_AON. Same carrier drive options as MODULE_EN. Leave floating if not used. See Section 6.
AD3	RTC_WAKE_N	RTC wake output, active low, open drain (PMX100UNEZ), driven from the RTC interrupt. Valid in every state while 5 V is present. Carrier pull-up to its always-on rail: ≤ 5.5 V, ≥ 10 kΩ. Leave floating if not used.
AI3	PMIC_GPIO5_10V	PMIC GPIO5, the PMIC in-circuit programming path (about 10 V). Joined on the module to BOOT3 (Y1, RZ/V2N BOOTSELCPU) through an on-module 0 Ω link: in normal use AI3 is the same node as BOOT3, so a carrier that drives or straps AI3 also drives BOOT3. Leave floating in normal use; see the warning below.
A2	USB_CC1	USB Type-C Configuration Channel 1.

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Pin Number	Pin Name	Description
B2	USB_CC2	USB Type-C Configuration Channel 2.
AQ30	SD_VDD_OUT	SD-card voltage output. Connect to SD card VDD.
H64	+V_CAM0	CAM0 LDO output. 0.6 V to 3.3 V, 300 mA max (input 3.3 V: the output stays below 3.3 V by the LDO dropout).
J64	+V_CAM1	CAM1 LDO output. 0.6 V to 3.3 V, 300 mA max (input 3.3 V: the output stays below 3.3 V by the LDO dropout).
L64	+V_CAM2	CAM2 LDO output. 0.6 V to 3.3 V, 300 mA max (input 3.3 V: the output stays below 3.3 V by the LDO dropout).
N64	+V_CAM3	CAM3 LDO output. 0.6 V to 3.3 V, 300 mA max (input 3.3 V: the output stays below 3.3 V by the LDO dropout).
H63	CAM_VFB0	Feedback node for +V_CAM0. Place divider close to the module pin.
J63	CAM_VFB1	Feedback node for +V_CAM1. Place divider close to the module pin.
L63	CAM_VFB2	Feedback node for +V_CAM2. Place divider close to the module pin.
N63	CAM_VFB3	Feedback node for +V_CAM3. Place divider close to the module pin.
B55	BL_LED_A / BL_PWM	BL_LED_A: anode of backlight. BL_PWM: connect to backlight driver.
A55	BL_LED_K	Cathode of backlight. Leave floating if BL_PWM is used.

Table 2 E1M-X V2N Power & Control Pins

> **Note:** AD3, AI3, AO3 and AP3 are NC in the E1M-X standard; on E1M-X V2N they carry module signals. A carrier for E1M-X V2N must not route its own nets through these pads.

> **Warning:** PMIC_GPIO5_10V (AI3) is the PMIC in-circuit programming path, which takes about 10 V. Apply 10 V to AI3 (or to the PMIC GPIO5 pin) only with the on-module 0 Ω link to B00T3 removed. With that link fitted, the 10 V reaches the RZ/V2N B00TSELCPU input and destroys the RZ/V2N. In normal use AI3 is electrically the same node as B00T3 (Y1), so a carrier that drives or straps AI3 also drives B00T3.

2.2 Analog Pins

Pin Number	Pin Name	Peripheral	Description
A17	ANA_S0	AIN	Analog input channels, referenced to 1V8.
B17	ANA_S1		
A16	ANA_S2		
B16	ANA_S3		
A15	ANA_S4		
B15	ANA_S5		
A14	ANA_S6		
B14	ANA_S7		

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Pin Number	Pin Name	Peripheral	Description
A19	DAC0	DAC0	Analog output channels, referenced to 1V8.
B19	DAC1	DAC1	
AR1	ANT_2.4GHz / NC		ANT: module antenna output for Wi-Fi 6 and BLE. Route 50 Ω trace. NC: leave floating.

Table 3 E1M-X V2N Analog Pins

2.3 Digital Pins

Pin Number	Pin Name	Peripheral	Description
AR21	IO8	GPIO / SMCU	General purpose I/O, controlled by the secondary MCU on E1M-X. Driven directly by the GD32 pin (1.8 V), no series resistor on the module.
AQ21	IO9		
AR22	IO10		
AQ22	IO11		
AR23	IO12		
AQ23	IO13		
AR24	IO14		
AQ24	IO15		
AR25	IO16		
F63	IO25		
F64	IO26		
AN63	IO27		
AN64	IO28		
AO63	IO29		
AO64	IO30		
AP63	IO31		
AP64	IO32		
AQ64	IO34		
A25	IO35		
AQ16	RTC_CLKOUT	RTC	Real-time clock output.
AC62	DBG_TX	DBG	On-module debug UART transmit.
AD62	DBG_RX	DBG	On-module debug UART receive.
L2	IO0	–	Not connected on E1M-X V2N. Leave floating.
M2	IO1	–	Not connected on E1M-X V2N. Leave floating.
N2	IO2	–	Not connected on E1M-X V2N. Leave floating.
O2	IO3	–	Not connected on E1M-X V2N. Leave floating.
AF2	IO4	–	Not connected on E1M-X V2N. Leave floating.
AG2	IO5	–	Not connected on E1M-X V2N. Leave floating.
AL2	IO6	–	Not connected on E1M-X V2N. Leave floating.
AQ26	IO17	–	Not connected on E1M-X V2N. Leave floating.
AR26	IO18	–	Not connected on E1M-X V2N. Leave floating.
AQ27	IO19	–	Not connected on E1M-X V2N. Leave floating.
AR27	IO20	–	Not connected on E1M-X V2N. Leave floating.

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Pin Number	Pin Name	Peripheral	Description
AQ28	IO21	–	Not connected on E1M-X V2N. Leave floating.
AR28	IO22	–	Not connected on E1M-X V2N. Leave floating.
AR29	IO24	–	Not connected on E1M-X V2N. Leave floating.
AR9	AUDIO_CLK	–	Audio clock output.
AQ7	PDM_C0	PDM0	Digital microphone interface. PDM_C is the clock, PDM_D is the data line.
AR7	PDM_D0		
AQ8	PDM_C1	PDM1	Digital microphone interface.
AR8	PDM_D1		
AQ5	I2S0_SCLK	I2S0	I^2S interface.
AQ4	I2S0_SDI		
AR4	I2S0_SDO		
AR5	I2S0_WS		
AR11	I2S1_SCLK	I2S1	I^2S interface.
AR10	I2S1_SDI		
AQ10	I2S1_SDO		
AQ11	I2S1_WS		
AH1	I2C0_SCL	I2C0	I^2C interface.
AH2	I2C0_SDA		
AQ47	I2C1_SCL	I2C1	I^2C interface.
AR47	I2C1_SDA		
E64	I2C2_SCL	I2C2	I^2C interface.
E63	I2C2_SDA		
A24	I2C3_SCL	I2C3	I^2C interface, controlled by the secondary MCU on E1M-X.
A23	I2C3_SDA		
AO3	GP_I2C.SCL	GP_I2C	Always-on 3.3 V I^2C, open drain, to the power controller (0x08) and the RTC (0x52); also the programming port of the power controller. 4.7 kΩ pull-ups to +3V3_AON on the module. No carrier pull-ups; keep the pads high-impedance whenever module 5 V is absent. See Section 8.4.2.
AP3	GP_I2C.SDA		
AQ19	I3C_SCL	I3C	I^3C interface.
AR19	I3C_SDA		
AE1	SPI0_CS0	SPI0	SPI interface.
AF1	SPI0_CS1		
AD1	SPI0_MISO		
AD2	SPI0_MOSI		
AE2	SPI0_SCLK		
AR14	SPI1_CS0	SPI1	SPI interface.
AR13	SPI1_CS1		
AQ13	SPI1_MISO		
AQ14	SPI1_MOSI		
AR15	SPI1_SCLK		
C64	SPI2_CS0	SPI2	SPI interface.
D64	SPI2_CS1		

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Pin Number	Pin Name	Peripheral	Description
B63	SPI2_MISO		
B64	SPI2_MOSI		
C63	SPI2_SCLK		
AB2	UART0_RX	UART0	UART interface.
AA2	UART0_TX		
AR17	UART1_RX	UART1	UART interface.
AQ17	UART1_TX		
B21	CAN0H / CAN0_TX	CAN0	CAN-BUS interface.
B22	CAN0L / CAN0_RX		
B24	CAN1H / CAN1_TX	CAN1	CAN-BUS interface.
B25	CAN1L / CAN1_RX		
A21	CAN_STBY	CAN	Standby control for CAN-BUS.
A7	PWM0	PWM	PWM output, controlled by the secondary MCU on E1M-X.
B7	PWM1		
A6	PWM2		
B6	PWM3		
A5	PWM4		
B5	PWM5		
A4	PWM6		
B4	PWM7		
A12	ENC0_X	ENC0	Encoder input.
B12	ENC0_Y		
A11	ENC1_X	ENC1	Encoder input.
B11	ENC1_Y		
A10	ENC2_X	ENC2	Encoder input.
B10	ENC2_Y		
A9	ENC3_X	ENC3	Encoder input.
B9	ENC3_Y		
AR56	ETH0_DD_N	ETH0	Ethernet interface. 1 Gbit PHY connection.
AQ56	ETH0_DD_P		
AR57	ETH0_DC_N		
AQ57	ETH0_DC_P		
AR58	ETH0_DB_N		
AQ58	ETH0_DB_P		
AR59	ETH0_DA_N		
AQ59	ETH0_DA_P		
AQ60	ETH0_LED0		
AR60	ETH0_LED1		
AR49	ETH1_DD_N	ETH1	Ethernet interface. 1 Gbit PHY connection.
AQ49	ETH1_DD_P		
AR50	ETH1_DC_N		
AQ50	ETH1_DC_P		
AR51	ETH1_DB_N		
AQ51	ETH1_DB_P		

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Pin Number	Pin Name	Peripheral	Description
AR52	ETH1_DA_N		
AQ52	ETH1_DA_P		
AQ53	ETH1_LED0		
AR53	ETH1_LED1		
AQ31	SD_CLK	SD0	SD card or eMMC interface.
AR31	SD_CMD		
AQ32	SD_D0		
AR33	SD_D1		
AQ33	SD_D2		
AR34	SD_D3		
AQ34	SD_DET		
AR32	SD_RST		
T64	CSI0_0_N	CSI0	MIPI CSI camera interface.
T63	CSI0_0_P		
S64	CSI0_1_N		
S63	CSI0_1_P		
Q64	CSI0_2_N		
Q63	CSI0_2_P		
P64	CSI0_3_N		
P63	CSI0_3_P		
R64	CSI0_C_N		
R63	CSI0_C_P		
Z64	CSI1_0_N	CSI1	MIPI CSI camera interface.
Z63	CSI1_0_P		
Y64	CSI1_1_N		
Y63	CSI1_1_P		
W64	CSI1_2_N		
W63	CSI1_2_P		
V64	CSI1_3_N		
V63	CSI1_3_P		
X64	CSI1_C_N		
X63	CSI1_C_P		
B61	DSI0_0_N	DSI0	MIPI DSI display interface.
A61	DSI0_0_P		
B60	DSI0_1_N		
A60	DSI0_1_P		
B59	DSI0_2_N		
A59	DSI0_2_P		
B58	DSI0_3_N		
A58	DSI0_3_P		
B57	DSI0_C_N		
A57	DSI0_C_P		
B47	PCIE0_CLK_N	PCIE0	PCIe interface. PCIE0_CLK_P/N: reference-clock output from the on-module clock generator (output DIFF1) through the on-

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Pin Number	Pin Name	Peripheral	Description
			module reference-clock buffer; the carrier must not add a second reference-clock source. See Section 8.3.
A47	PCIE0_CLK_P		
B42	PCIE0_RX0_N		
A42	PCIE0_RX0_P		
B43	PCIE0_RX1_N		
A43	PCIE0_RX1_P		
B38	PCIE0_TX0_N		
A38	PCIE0_TX0_P		
B39	PCIE0_TX1_N		
A39	PCIE0_TX1_P		
C1	USB0_30_D_N	USB0	USB 3.0 interface.
B1	USB0_30_D_P		
F1	USB0_30_RX0_N		
E1	USB0_30_RX0_P		
I1	USB0_30_TX0_N		
H1	USB0_30_TX0_P		
G2	USB2_20_ID	USB2	USB 2.0 interface.
J2	USB2_20_N		
I2	USB2_20_P		
F2	USB2_20_VBUS		

Table 4 E1M-X V2N Digital Pins

Note: The pads served by the secondary MCU (GD32, VIO_1V8 I/O) — PWM0–PWM7, ENC0–ENC3 X / Y, the GPIO pads IO8–IO16, IO25–IO32, IO34, IO35, and ANA_S0–ANA_S7, DAC0 / DAC1, I2C3 — connect directly to GD32 pins, with no series resistors on the module. Drive strength and ESD robustness are those of the GD32 pin itself; protect pads that leave the carrier board.

2.4 Not Connected Pins

These pins carry an E1M-X™ standard function that is not implemented on the V2N module. They retain their standard name for cross-variant compatibility and must be left floating.

Pin Number	Pin Name	Description
A27	PCIE1_TX0_P	Leave floating.
A28	PCIE1_TX1_P	Leave floating.
A29	PCIE1_TX2_P	Leave floating.
A30	PCIE1_TX3_P	Leave floating.
A31	PCIE1_RX0_P	Leave floating.
A32	PCIE1_RX1_P	Leave floating.
A33	PCIE1_RX2_P	Leave floating.
A34	PCIE1_RX3_P	Leave floating.
A36	PCIE1_CLK_P	Leave floating.
A40	PCIE0_TX2_P	Leave floating.

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Pin Number	Pin Name	Description
A41	PCIE0_TX3_P	Leave floating.
A44	PCIE0_RX2_P	Leave floating.
A45	PCIE0_RX3_P	Leave floating.
A49	DSI1_C_P	Leave floating.
A50	DSI1_3_P	Leave floating.
A51	DSI1_2_P	Leave floating.
A52	DSI1_1_P	Leave floating.
A53	DSI1_0_P	Leave floating.
AA3	LCD_B23	Leave floating.
AB3	LCD_HSYNC	Leave floating.
AB63	CSI2_3_P	Leave floating.
AB64	CSI2_3_N	Leave floating.
AC3	LCD_VSYNC	Leave floating.
AC63	CSI2_2_P	Leave floating.
AC64	CSI2_2_N	Leave floating.
AD63	CSI2_C_P	Leave floating.
AD64	CSI2_C_N	Leave floating.
AE3	NC	Leave floating.
AE63	CSI2_1_P	Leave floating.
AE64	CSI2_1_N	Leave floating.
AF3	NC	Leave floating.
AF63	CSI2_0_P	Leave floating.
AF64	CSI2_0_N	Leave floating.
AG3	NC	Leave floating.
AH3	NC	Leave floating.
AH63	CSI3_3_P	Leave floating.
AH64	CSI3_3_N	Leave floating.
AI63	CSI3_2_P	Leave floating.
AI64	CSI3_2_N	Leave floating.
AJ3	NC	Leave floating.
AJ63	CSI3_C_P	Leave floating.
AJ64	CSI3_C_N	Leave floating.
AK3	NC	Leave floating.
AK63	CSI3_1_P	Leave floating.
AK64	CSI3_1_N	Leave floating.
AL3	NC	Leave floating.
AL63	CSI3_0_P	Leave floating.
AL64	CSI3_0_N	Leave floating.
AM3	NC	Leave floating.
AN1	ANT_6GHz	Leave floating.
AN3	NC	Leave floating.
AP1	ANT_5GHz	Leave floating.
AQ36	NC	Leave floating.
AQ37	NC	Leave floating.

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Pin Number	Pin Name	Description
AQ38	NC	Leave floating.
AQ39	NC	Leave floating.
AQ40	NC	Leave floating.
AQ41	NC	Leave floating.
AQ42	NC	Leave floating.
AQ43	NC	Leave floating.
AQ44	NC	Leave floating.
AQ45	NC	Leave floating.
AQ63	IO33	Leave floating.
AR36	NC	Leave floating.
AR37	NC	Leave floating.
AR38	NC	Leave floating.
AR39	NC	Leave floating.
AR40	NC	Leave floating.
AR41	NC	Leave floating.
AR42	NC	Leave floating.
AR43	NC	Leave floating.
AR44	NC	Leave floating.
AR45	NC	Leave floating.
B27	PCIE1_TX0_N	Leave floating.
B28	PCIE1_TX1_N	Leave floating.
B29	PCIE1_TX2_N	Leave floating.
B30	PCIE1_TX3_N	Leave floating.
B31	PCIE1_RX0_N	Leave floating.
B32	PCIE1_RX1_N	Leave floating.
B33	PCIE1_RX2_N	Leave floating.
B34	PCIE1_RX3_N	Leave floating.
B36	PCIE1_CLK_N	Leave floating.
B40	PCIE0_TX2_N	Leave floating.
B41	PCIE0_TX3_N	Leave floating.
B44	PCIE0_RX2_N	Leave floating.
B45	PCIE0_RX3_N	Leave floating.
B49	DSI1_C_N	Leave floating.
B50	DSI1_3_N	Leave floating.
B51	DSI1_2_N	Leave floating.
B52	DSI1_1_N	Leave floating.
B53	DSI1_0_N	Leave floating.
C2	USB0_30_VBUS	Leave floating.
C62	CAM_HSYNC	Leave floating.
D2	USB0_30_ID	Leave floating.
D3	LCD_B0	Leave floating.
D62	CAM_VSYNC	Leave floating.

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Pin Number	Pin Name	Description
D63	NC	Leave floating. To be confirmed: in the current design data the pad is tied to GND on the module.
E3	LCD_B1	Leave floating.
E62	CAM_PCLK	Leave floating.
F3	LCD_B2	Leave floating.
F62	CAM_XVCLK	Leave floating.
G3	LCD_B3	Leave floating.
G62	CAM_D1	Leave floating.
H3	LCD_B4	Leave floating.
H62	CAM_D2	Leave floating.
I3	LCD_B5	Leave floating.
I62	CAM_D3	Leave floating.
J3	LCD_B6	Leave floating.
J62	CAM_D4	Leave floating.
K1	USB1_30_D_P	Leave floating.
K3	LCD_B7	Leave floating.
K62	CAM_D5	Leave floating.
L1	USB1_30_D_N	Leave floating.
L3	LCD_B8	Leave floating.
L62	CAM_D6	Leave floating.
M3	LCD_B9	Leave floating.
M62	CAM_D7	Leave floating.
N1	USB1_30_RX0_P	Leave floating.
N3	LCD_B10	Leave floating.
N62	CAM_D8	Leave floating.
O1	USB1_30_RX0_N	Leave floating.
O3	LCD_B11	Leave floating.
O62	CAM_D9	Leave floating.
P3	LCD_B12	Leave floating.
P62	CAM_D10	Leave floating.
Q1	USB1_30_TX0_P	Leave floating.
Q2	USB1_30_VBUS	Leave floating.
Q3	LCD_B13	Leave floating.
Q62	CAM_D11	Leave floating.
R1	USB1_30_TX0_N	Leave floating.
R2	USB1_30_ID	Leave floating.
R3	LCD_B14	Leave floating.
R62	CAM_D12	Leave floating.
S3	LCD_B15	Leave floating.
S62	CAM_D13	Leave floating.
T3	LCD_B16	Leave floating.
T62	CAM_D14	Leave floating.
U3	LCD_B17	Leave floating.

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Pin Number	Pin Name	Description
U62	CAM_D15	Leave floating.
V3	LCD_B18	Leave floating.
V62	CAM_D16	Leave floating.
W3	LCD_B19	Leave floating.
X3	LCD_B20	Leave floating.
Y3	LCD_B21	Leave floating.
Z3	LCD_B22	Leave floating.

Table 5 E1M-X V2N Not-connected Pins

2.5 Reserved Pins

Pin Number	Pin Name	Description
W62, X62, Y62, Z62, AA62, AB62, AF62, AG62, AH62, AI62, AJ62, AK62	RSVD	Do not connect. Used for production purposes.
AE62, AL62, AM62, AN62, AO62, AP62, AQ62, AR62	RSVD	Not connected on the module. Do not connect.

Table 6 E1M-X V2N Reserved Pins

3 Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power-supply voltage	VDDIN to GND	- 0.3	6.0	V
Analog input voltage	V(ANA_Sx)	- 0.3	1.98	V
Digital IO (1V8)		- 0.3	1.98	V

Table 7 E1M-X V2N Absolute Maximum Ratings

> **Warning:** Stresses beyond Absolute Maximum Ratings may cause permanent damage. Operation at these conditions is not implied.

3.2 Recommended Operating Conditions

The module is specified to meet the Electrical Characteristics in Section 3.3 over the conditions below. Operation outside this range is not guaranteed.

Parameter	Symbol	Min	Typ	Max	Unit
Module supply voltage	VDDIN	4.5	5.0	5.5	V
Ambient operating temperature	T_A	- 40	–	+85	°C
Relative humidity (operating, non-condensing)	RH	TBD	–	TBD	%

Table 8 E1M-X V2N Recommended Operating Conditions

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3.3 Electrical Characteristics

Symbol	Description	Min	Nom	Max	Unit
Power supply					
VDDIN	Module power supply	4.5	5.0	5.5	V
I_{DDMAX}	Maximum I_{DD} current			TBD	
SD_VDD_OUT	SD-card supply		3.3		V
Analog inputs					
V(AINx)	Input voltage	0	–	1.8	V
Digital IOs					
V_{OL}	Low-level output voltage				
V_{OH}	High-level output voltage				
V_{IL}	Low-level input voltage				
V_{IH}	High-level input voltage				
Camera LDOs					
+V_CAM0	CAM0 LDO output	0.6	–	3.3	V
+V_CAM1	CAM1 LDO output	0.6	–	3.3	V
+V_CAM2	CAM2 LDO output	0.6	–	3.3	V
+V_CAM3	CAM3 LDO output	0.6	–	3.3	V

Table 9 E1M-X V2N Electrical Characteristics

3.4 ESD & Latch-up Ratings

ESD ratings apply at module-level — i.e. directly to the LGA pads as exposed to a carrier-board assembly process. Customer ESD protection requirements on the carrier board are described in the relevant interface sub-sections.

Parameter	Standard	Min	Max	Unit
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001	–	TBD	V
Charged Device Model (CDM)	ANSI/ESDA/JEDEC JS-002	–	TBD	V
Latch-up	JESD78	–	TBD	mA

Table 10 E1M-X V2N ESD & Latch-up Ratings

3.5 Thermal Characteristics

The E1M-X V2N dissipates heat primarily through the Renesas RZ/V2N SoC. Thermal-resistance figures below are typical for a 45 × 65 mm module mounted on a 4-layer FR4 carrier with a ground-plane heatsink. Carrier-board copper area, airflow, and via stitching all affect the realised thermal performance.

Parameter	Symbol	Typ	Max	Unit
Thermal resistance, junction-to-ambient (still air)	θ_{JA}	TBD	–	°C/W
Thermal resistance, junction-to-board	θ_{JB}	TBD	–	°C/W
Maximum junction temperature	$T_{J,max}$	–	TBD	°C
Power dissipation derating (above +85 °C)	P_D	TBD	–	mW/°C

Table 11 E1M-X V2N Thermal Characteristics

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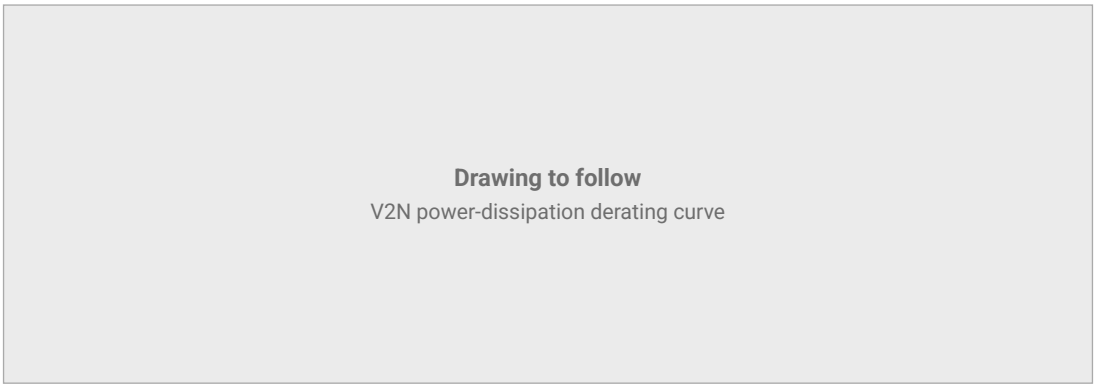


Figure 8 V2N power-dissipation derating curve

4 Power

4.1 Power Architecture

All power rails on the module are generated and managed on-board from a single externally-supplied 5 V input on VDD_5V_IN. No carrier-side rail sequencing is required.

The module power tree is split into two domains:

- **Always-on domain**, alive whenever VDD_5V_IN is present: the always-on 3.3 V LDO (TPS7A0233PYCHR, from VDD_5V_IN, rail +3V3_AON) and the always-on 1.8 V LDO (TPS7A0218PYCHR, from +3V3_AON, rail +1V8_AON), the real-time clock (Micro Crystal RV-3028-C7) with its backup input +S_CAP for a carrier-side backup store (see Section 4.2), and the programmable power controller. The power controller filters MODULE_EN and MODULE_STBY, holds the module power latch, drives the PMIC enable and, together with the PMIC reset output, PORn. The RTC interrupt wakes the module through the power controller and drives the RTC_WAKE_N output (AD3). The RTC and the power controller share the always-on GP_I2C bus (Section 8.4.2).
- **Main domain**: the I^2C-controlled main PMIC and the Renesas DA9292 dual-phase buck regulator (the 0.8 V core rail of the RZ/V2N). The PMIC is enabled only by the power controller. The PMIC releases PORn (Z1) to the RZ/V2N and the reset of the on-module GD32 I/O MCU (Cortex-M33 @ 216 MHz). The GD32 runs from the module 1.8 V rail and switches only the four camera LDOs, not the main rails.

The power controller is the only driver of the PMIC enable, so a module without a programmed power controller never starts. It runs the Alp Lab image v2n_ctl_v1, which is not interchangeable with any E1M-AEN image. It is programmed over GP_I2C (AO3 / AP3) at provisioning with MODULE_EN held low; a new image takes effect after the next 5 V cycle. Its behaviour and its firmware register are described in Section 6.1.

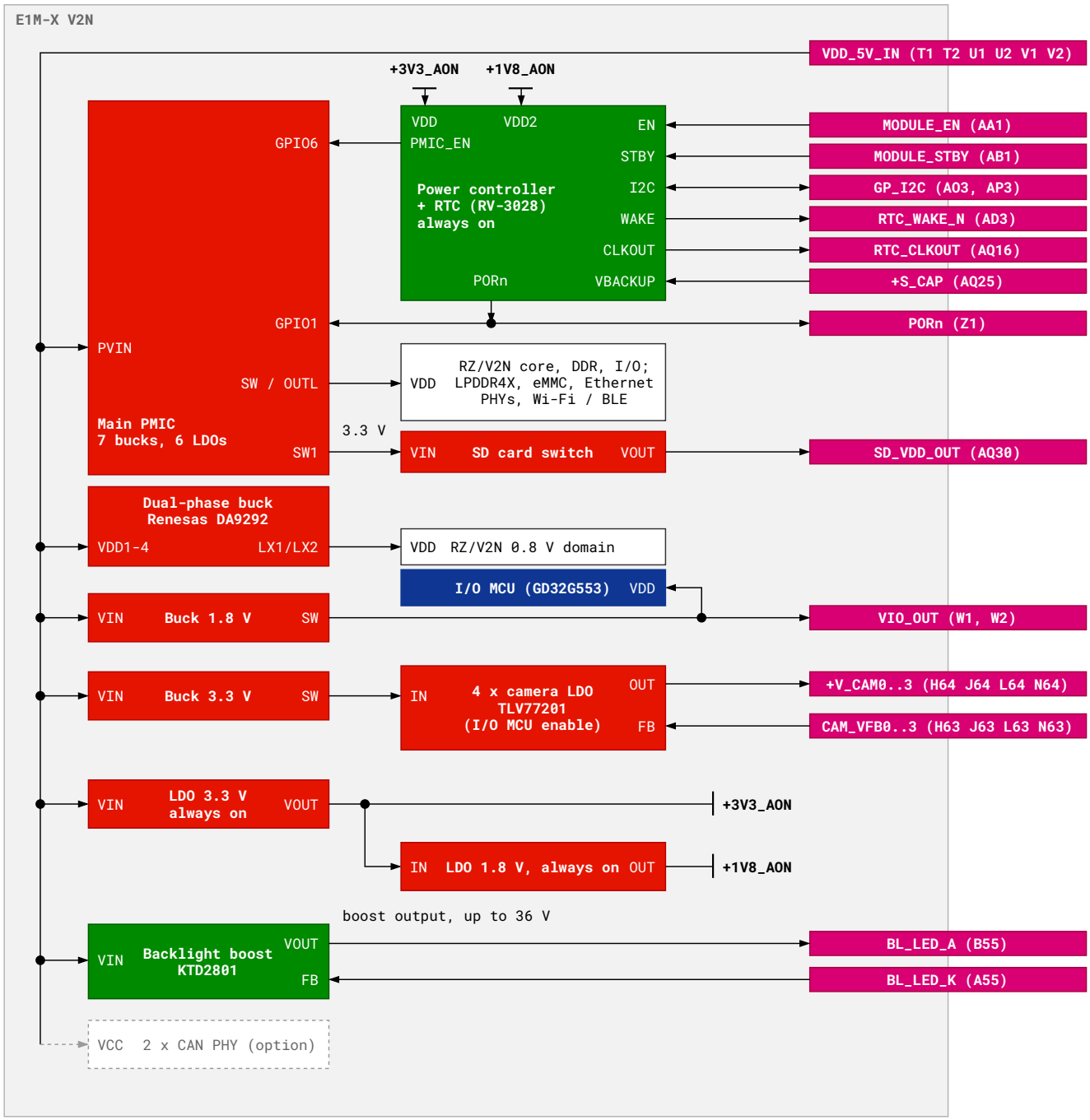
The E1M-X V2N includes all necessary decoupling capacitors. Additional decoupling capacitors on the carrier board may improve performance further.

The module exposes two regulated output rails to the carrier:

Rail	Pins	Voltage	Max current	Purpose
VIO_OUT	W1, W2	1.8 V ± 5%	TBD mA	I/O reference for carrier-side level shifters.
SD_VDD_OUT	AQ30	3.3 V	300 mA	microSD slot supply, switched on by the RZ/V2N. The SD signal level switches between 3.3 V and 1.8 V on the module.

Table 12 Module Output Rails

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MODULE_EN (AA1), MODULE_STBY (AB1): PMX100UNZ clamps, 1 MΩ pull-ups to +1V8_AON; to the power controller.

The power controller is the only driver of the PMIC enable. +3V3_AON and +1V8_AON are on whenever 5 V is present.

PORn (Z1): PMIC reset output and the power controller (open drain), 10 kΩ pull-up to VDD1G_1P8; the carrier may pull it low.

+S_CAP goes directly to the RTC backup input. RTC_WAKE_N: RTC interrupt, open drain.

VIO_OUT also supplies the on-module I/O MCU. The CAN PHYs are not fitted in the standard build.

Figure 9 E1M-X V2N Power Architecture

4.2 RTC Backup

The real-time clock (RV-3028-C7, GP_I2C address 0x52) runs from the always-on 3.3 V rail +3V3_AON, so it keeps running while 5 V is present, with the module on or off. Its backup input VBACKUP connects directly to the +S_CAP pad (AQ25, net VBAT). The module has no backup capacitor fitted: to keep the time while 5 V is absent, fit a super-capacitor or backup cell on the carrier at +S_CAP.

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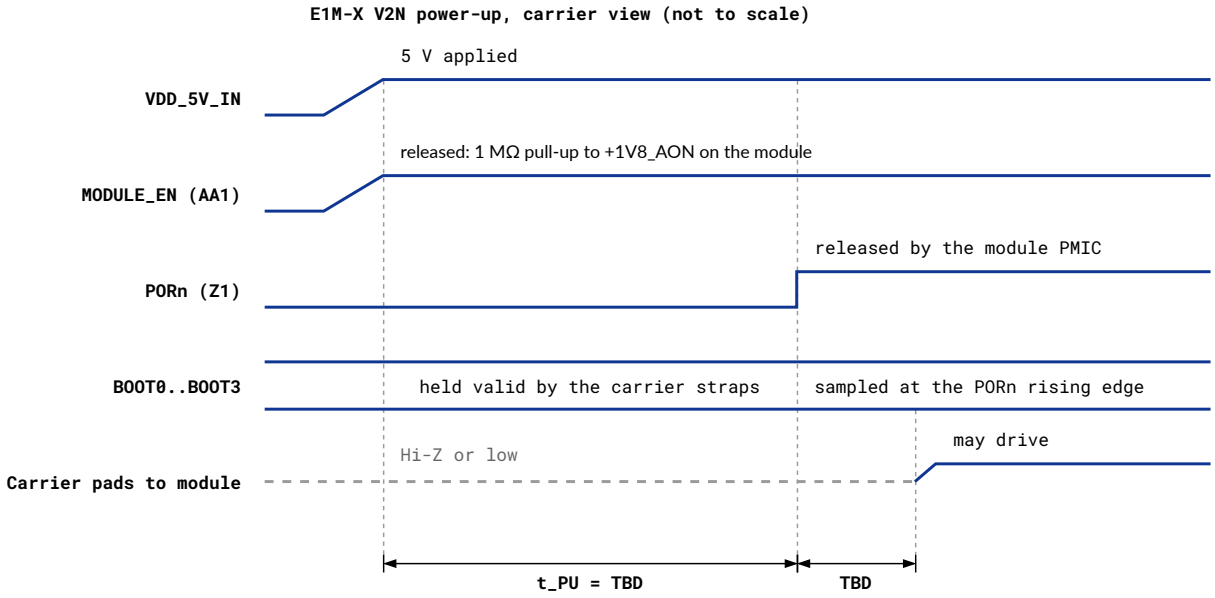
The RTC interrupt RTC_INT_N (100 kΩ pull-up to +3V3_AON) wakes the module through the power controller and drives the RTC_WAKE_N output (AD3). The RTC clock output reaches the RTC_CLKOUT pad (AQ16) through an on-module buffer (SN74AUP1G34YFPR) supplied from VDD1G_1P8, so RTC_CLKOUT is driven only while the module is on.

Warning: With a non-rechargeable backup cell on +S_CAP, firmware must keep the RTC trickle charger disabled.

4.3 Power-Up & Reset Sequence

The on-module PMIC sequences the internal rails; no carrier-side rail sequencing is required. The recommended carrier-side control-signal bring-up order is:

1. Apply 5 V to VDD_5V_IN. The always-on rails +3V3_AON / +1V8_AON, the RTC and the power controller come up.
2. Release MODULE_EN (the 1 MΩ module pull-up to +1V8_AON holds it high). The power controller sets its latch and raises the PMIC enable at once.
3. Leave PORn released (no carrier pull-up).
4. Wait for the on-module power-up to complete. Internal rails stabilise and the PMIC releases PORn to start the RZ/V2N boot ROM within TBD ms of MODULE_EN release. The module exposes no ready-strobe output, so allow this fixed delay before driving signals into the module.
5. Begin communication with the module.



The module sequences its rails; the carrier applies 5 V and leaves MODULE_EN and PORn released. Timing values: TBD.

Figure 10 E1M-X V2N Power-Up Sequence (order; timing values TBD)

For power-down, hold MODULE_EN low (≥ 55 ms powers the module off, Section 6) or use the firmware self-off (Section 6.1), then remove VDD_5V_IN.

Warning: Hold MODULE_EN low at least 150 ms before removing 5 V. Removing 5 V with the module on is for recovery only.

4.4 Power Consumption

Numbers below are typical at T_A = +25 °C, VDDIN = 5.0 V, with Wi-Fi and BLE disabled unless otherwise noted. Active and low-power figures depend on software workload (DRP-AI3 utilisation, Ethernet PHY state, PCIe link state).

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Mode	Description	Min	Typ	Max	Unit
Active					
Active, A55 quad @ 1.8 GHz + DRP-AI3 @ full load	Vision inference workload	–	TBD	TBD	mA
Active, A55 quad @ 1.8 GHz, no AI	General Linux compute	–	TBD	TBD	mA
Active, with Wi-Fi 6 TX @ +20 dBm	Wireless TX peak	–	TBD	TBD	mA
Active, with dual Ethernet linked + PCIe SSD	Full-feature workload	–	TBD	TBD	mA
Low-power					
Idle	Cores halted, peripherals on	–	TBD	–	mA
Sleep	Retention only, RTC running	–	TBD	–	µA
Shutdown (MODULE_EN low)	Module disabled	–	TBD	–	µA

Table 13 E1M-X V2N Power Consumption (typical)

4.5 Boot Settings

E1M-X V2N supports several boot options selected by the BOOT0–BOOT3 strap pins on the carrier.

BOOT1	BOOT0	Boot mode	Device	CA55 boot	CM33 boot
0	0	Mode 0	eSD (3.3 V for execution)	Supported	Not supported
0	1	Mode 1	eMMC (I/O voltage 1.8 V)	Supported	Not supported
1	0	Mode 2	QSPI NOR (I/O voltage 1.8 V)	Supported	Supported
1	1	Mode 3	SCIF download	Supported	Supported

Table 14 E1M-X V2N Boot Options

> **Note:** BOOT2 is fixed at 1. Each strap takes a 1 kΩ pull-up to VIO_OUT for 1 or a 1 kΩ pull-down to GND for 0; an open strap reads 1 (RZ/V2N internal pull-up), but do not rely on it.

5 Boot Modes

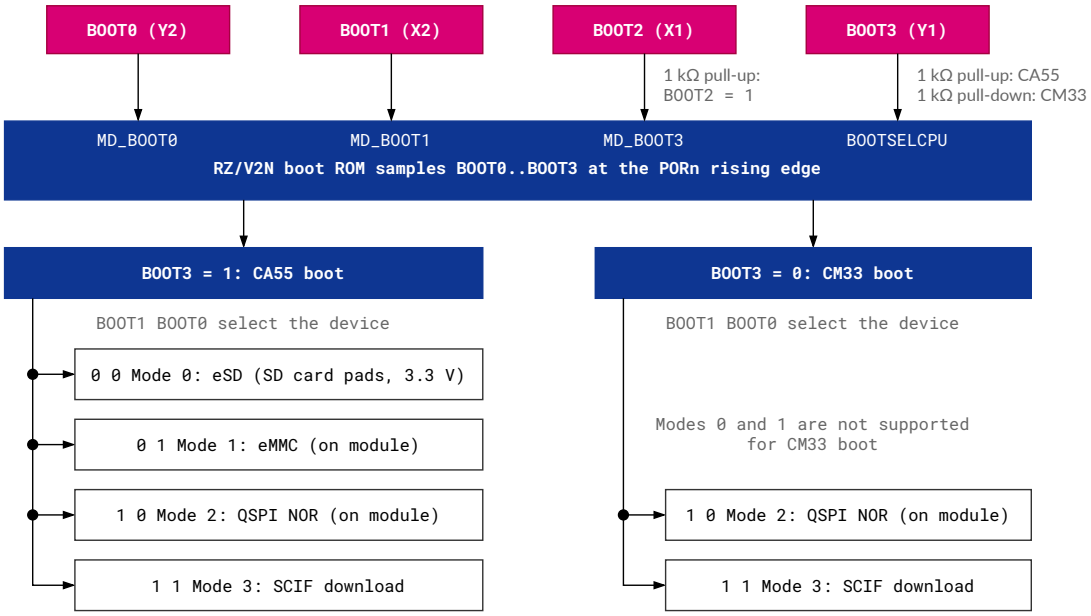
The Renesas RZ/V2N samples the four boot-strap pins (BOOT0–BOOT3) at the rising edge of PORn. BOOT0/BOOT1 select the boot source; BOOT2 is fixed at 1 on the V2N family; BOOT3 selects the boot CPU (high = CA55, low = CM33). See Section 4.5 for the full mapping.

Strap every boot pin (BOOT0–BOOT3) on the carrier with a 1 kΩ resistor: a 1 kΩ pull-up to VIO_OUT for 1, a 1 kΩ pull-down to GND for 0. The RZ/V2N has internal pull-ups on its boot-strap pins, so a strap left open reads 1, but a carrier design must not rely on them.

The carrier-board **MUST** drive BOOT0/BOOT1 (typically via a 2-position DIP switch to VIO_OUT with 1 kΩ pull-downs to GND: closed = 1, open = 0), or hard-strap them with 1 kΩ resistors. The other two strap pins are hard-strapped: a 1 kΩ pull-up from VIO_OUT on BOOT2 (the module has no BOOT2 pull-up), and on BOOT3 a 1 kΩ pull-up from VIO_OUT for CA55 boot or a 1 kΩ pull-down to GND for CM33 boot. On the module BOOT3 is also tied to the PMIC GPIO5 through an on-module 0 Ω link; the PMIC GPIO5 is an input (high impedance) and does not drive the strap. Pad AI3 (PMIC_GPIO5_10V) is the same node: leave it open, and observe the 10 V warning in Section 2.1.

> **Note:** Refer to the Renesas RZ/V2N hardware-reference manual for the internal boot sequence and image-signing requirements. For details on the secure-boot signing flow, see **AN-010: Secure Boot and Code Signing**.

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SCIF download uses the debug UART pads DBG_TX (AC62) / DBG_RX (AD62).
Full mapping: Boot Settings table.
Every strap: 1 kΩ pull-up to VIO_OUT for 1, 1 kΩ pull-down to GND for 0.
An open strap reads 1 (RZ/V2N internal pull-up); do not rely on it.

Figure 11 E1M-X V2N Boot Flow

6 Reset, Module Enable & Power Control

The carrier controls the module with VDD_5V_IN, MODULE_EN, MODULE_STBY and PORn, and reads the RTC wake output RTC_WAKE_N. All other power sequencing is inside the module (Section 4.1).

Pin	Direction	Description
MODULE_EN (AA1)	Input, 1.8 V to 5 V logic	Pull low to switch the module off. Low ≤ 0.5 ms: ignored. Low ≥ 4 ms: the RZ/V2N is reset; the rails stay up. Low ≥ 55 ms: the module powers off. On the module: a PMX100UNZ clamp (gate +1V8_AON) to the power controller, a filtered input (about 1 ms), and a 1 MΩ pull-up to +1V8_AON. The carrier may use an open-drain output with no pull-up, a switch to GND, or push-pull logic from 1.8 V to 5 V. Released, the pad sits at about 1.2–1.5 V (estimate). Leave floating if unused.
MODULE_STBY (AB1)	Input, 1.8 V to 5 V logic	Standby and wake request, pulse-only. Low pulse ≥ 2 ms with the module on: request to firmware (through RTC_ALARM, read by the RZ/V2N PA7 and the GD32 PC14). Low pulse ≥ 2 ms in self-off: the module wakes. Held low: blocks the firmware self-off. Same front end and carrier drive options as MODULE_EN. Leave floating if unused.
PORn (Z1)	Input / output, open drain	RZ/V2N reset, 1.8 V: driven by the PMIC reset output and by the power controller, 10 kΩ pull-up to VDD1G_1P8 on the module. After the power latch clears, PORn goes low about 2 ms later. The carrier may pull it low to reset the RZ/V2N with the rails up; no carrier pull-up. Minimum low-pulse width: TBD µs.
RTC_WAKE_N (AD3)	Output, open drain	Active low, driven from the RTC interrupt RTC_INT_N: a PMX100UNZ inverts it onto RTC_WAKE (10 MΩ pull-up to +3V3_AON), and a PMX100UNEZ drives AD3. Valid in every state while 5 V is present. Carrier pull-up to its always-on rail, ≤ 5.5 V, ≥ 10 kΩ.

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Table 15 Reset, Enable & Power-control Signals (timing: design values of the `v2n_ctl_v1` image; bench validation pending)

Warning: Keep the carrier leakage on `MODULE_EN` and `MODULE_STBY` at ≤ 0.1 µA on each pad, ESD parts included.

Asserting `PORn` from the carrier resets the RZ/V2N only; the rails stay up.

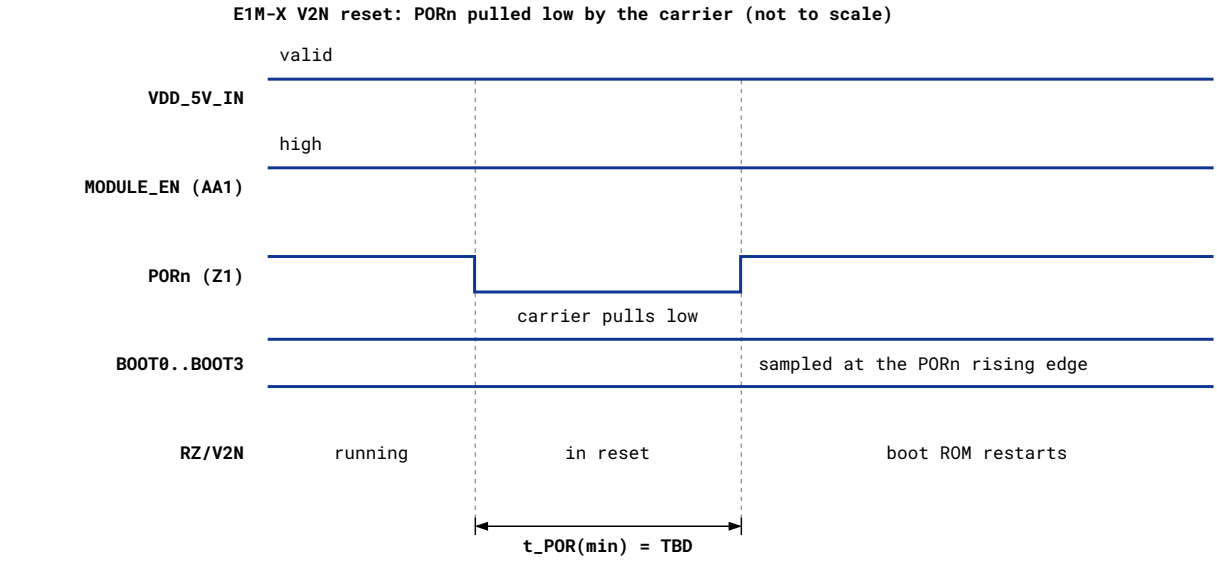


Figure 12 E1M-X V2N Reset Timing (PORn; timing values TBD)

6.1 Power Controller

The programmable power controller (Section 4.1) holds the module power latch and runs the firmware self-off and the wake logic. Behaviour of the `v2n_ctl_v1` image (design values; bench validation pending):

- **On:** `MODULE_EN` released, or an RTC / `MODULE_STBY` wake event, sets the latch; the PMIC enable rises at once and the PMIC releases `PORn` when its rails are up.
- **Off:** `MODULE_EN` held low, or the firmware self-off. `PORn` goes low about 2 ms after the latch clears and the PMIC enable falls about 50 ms after the latch clears. The next start is locked out for about 145–158 ms.
- **Wake and standby events** reach firmware on `RTC_ALARM`, an open-drain output read by the RZ/V2N (PA7) and by the GD32 (PC14).
- **Self-off refusal in hardware:** an OFF request is refused while `RTC_INT_N` is low or `MODULE_STBY` is asserted, so a wake event is never lost.
- **Blank or unprogrammed power controller:** all its outputs are high-impedance and a 100 kΩ pull-down holds the PMIC enable low, so the module stays off.

Register	Function	Use
`0x7A`	`Firmware self-off`	`The RZ/V2N writes the register twice: OFF_ARM, then OFF. Write 0x7A = 0x00 on every boot before the first use of the power controller (a wake from self-off is not a power-on reset of the power controller). The register bit positions are released together with the image.`

Table 16 Power Controller Register (`GP_I2C` address `0x08`)

Only the RZ/V2N addresses the power controller, the RTC and the PMIC. The on-module GD32 can reach `BRD_I2C` but must not address them.

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Warning: Never set the power controller's lock bit, never issue its soft reset, and never write its NVM or register 0xC7 from the application. All outputs of the power controller then go high-impedance and the module powers off uncontrolled.

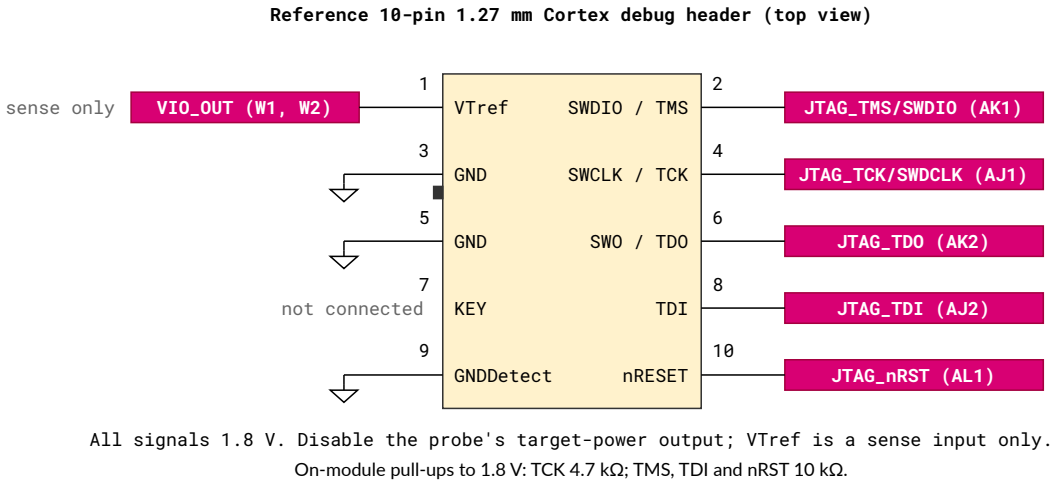
7 JTAG / SWD Debug

The E1M-X V2N exposes a 5-pin JTAG / SWD interface for programming and debug of the RZ/V2N. Signals operate at 1.8 V; carrier-board level shifters are required for 3.3 V debug probes.

Pin	Signal	Description
AL1	JTAG_nRST	Active-low reset to the SoC debug logic.
AJ1	JTAG_TCK / SWDCLK	Test clock (JTAG) or serial-wire clock (SWD).
AJ2	JTAG_TDI	Test data in (JTAG only).
AK2	JTAG_TDO	Test data out (JTAG only).
AK1	JTAG_TMS / SWDIO	Test mode select (JTAG) or serial-wire I/O (SWD).

Table 17 JTAG / SWD Pinout

Note: Alp Lab recommends exposing the JTAG/SWD pins on a 10-pin Cortex-M debug header on the carrier board. The E1M-X EVK populates this header by default. Refer to **UG-E1M-X-001** §5.1 for the reference connector pinout.



All signals 1.8 V. Disable the probe's target-power output; VTref is a sense input only.
On-module pull-ups to 1.8 V: TCK 4.7 kΩ; TMS, TDI and nRST 10 kΩ.

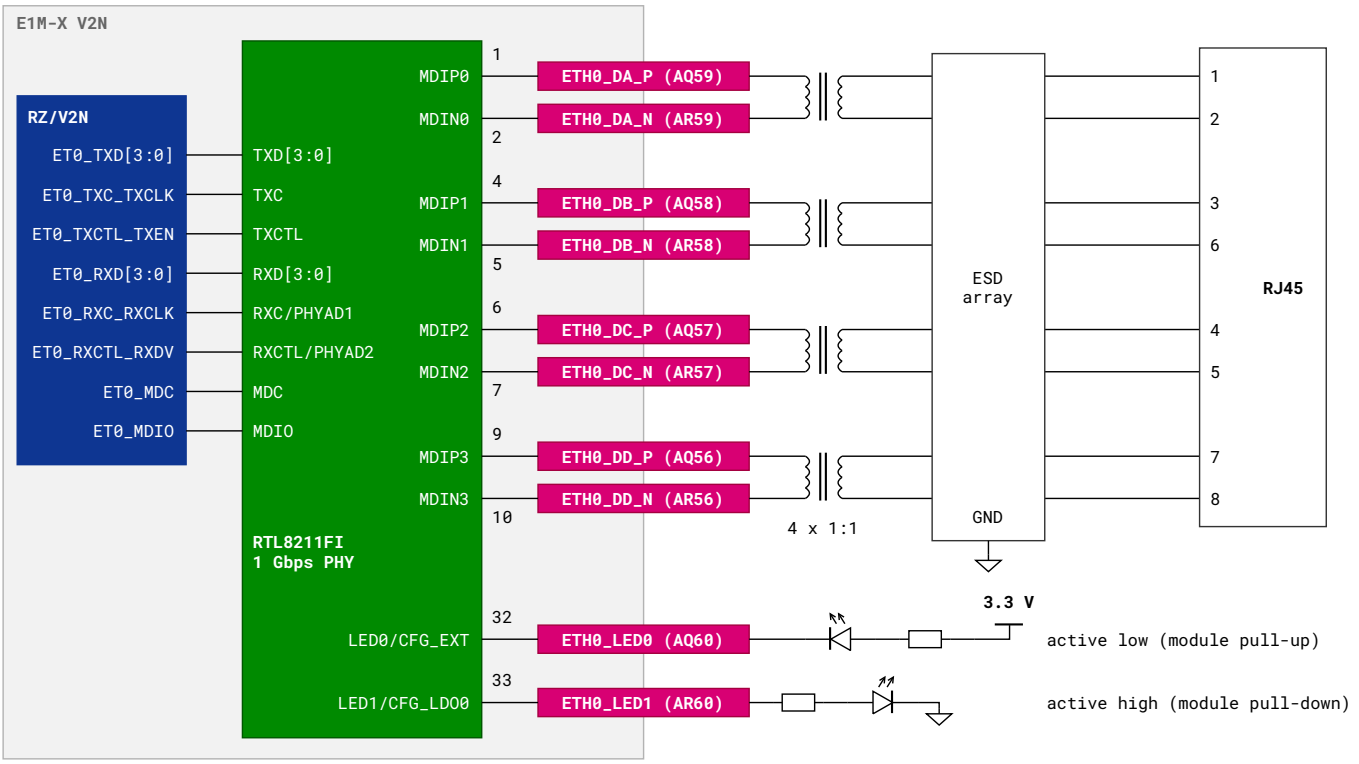
Figure 13 Reference JTAG / SWD Header Pinout

8 Interfaces

8.1 Ethernet

E1M-X V2N has two 1 Gbit Ethernet PHYs: the Realtek RTL8211FI-VD-CG, connected to the RZ/V2N over RGMII. The interfaces do not include on-module EMI or ESD protection; the user must provide external magnetics transformers, connectors, and EMI/ESD protection on the carrier board.

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MDI pairs: 100 Ω differential; transformer centre taps per the magnetics data sheet.
ETH0_LED0 / ETH0_LED1 are PHY strap pins (4.7 kΩ on the module): never pull them the other way.
ETH1: same circuit on ETH1_DA_P/N (AQ52/AR52), DB (AQ51/AR51), DC (AQ50/AR50), DD (AQ49/AR49), ETH1_LED0 (AQ53), ETH1_LED1 (AR53).

Figure 14 E1M-X V2N Ethernet Connection (ETH0; ETH1 is identical)

8.2 USB

E1M-X has one USB 2.0 and one USB 3.2 Gen 2 interface. USB 2.0 supports Host/Function; USB 3.2 is Host-only.

Pin Number	Pin Name	Peripheral	Description
C1	USB0_30_D_N	USB0	Route USB_N and USB_P as a differential pair with 90 Ω impedance.
B1	USB0_30_D_P		
F1	USB0_30_RX0_N		
E1	USB0_30_RX0_P		
I1	USB0_30_TX0_N		
H1	USB0_30_TX0_P		
G2	USB2_20_ID	USB2	Low: Host mode. NC: Device mode.
J2	USB2_20_N		Route USB_N and USB_P as a differential pair with 90 Ω impedance.
I2	USB2_20_P		
F2	USB2_20_VBUS		Connect to USB VBUS 5 V.

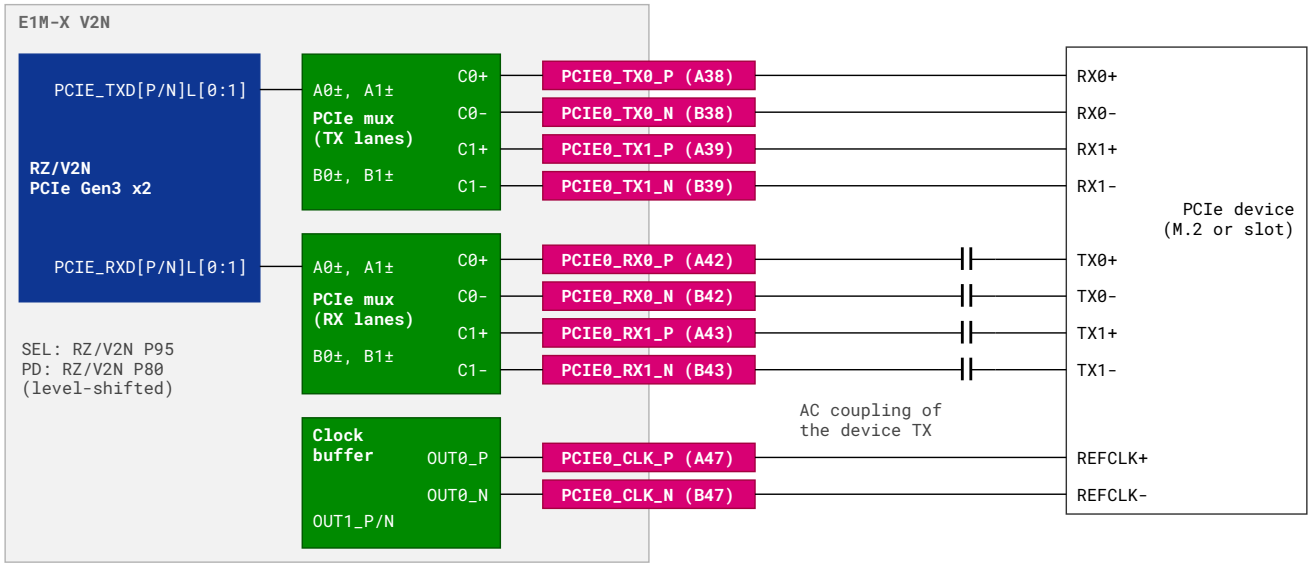
Table 18 E1M-X V2N USB Interface

8.3 PCIe

Renesas RZ/V2N has one PCIe® Gen3 2-lane interface. On the module it reaches the PCIE0 pads through two 2:1 passive differential multiplexers (Diodes PI3DBS12212A), one for the TX lanes and one for the RX lanes. Port A (the common port) of each multiplexer connects to the RZ/V2N, port C to the PCIE0 pads, and port B to the DX-M1 position, which is not fitted on E1M-X V2N. SEL = 0 links port A to port B (the open DX-M1 position); SEL = 1 links port A to port C (the PCIE0 pads). PD = 1 powers both multiplexers down (all switches high impedance). The RZ/V2N drives SEL and PD from GPIOs through a level translator: to

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use the PCIE0 pads, software sets SEL = 1 and PD = 0 on both multiplexers. The PCIe reference clock comes from the on-module clock generator (5L35023B-000NLGI, Section 8.14): the RZ/V2N root complex takes its output DIFF2 on PCIE_REFCLKP0 / PCIE_REFCLKN0 through 33 Ω series resistors, and its DIFF1 clock drives the on-module reference-clock buffer, whose first output drives the PCIE0_CLK_P/N pads (A47 / B47); the buffer's second output goes to the DX-M1 position, which is not fitted. Both clocks come from the same PLL (common clock). The carrier must not add a second reference-clock source for the device on PCIE0.



Module TX lanes are AC-coupled on the module; module RX lanes are not. PCIE0_CLK is a reference-clock output. Port A (common) is the RZ/V2N. SEL = 0: A to B; SEL = 1: A to C (PCIE0 pads); PD = 1: all switches Hi-Z. B0±, B1± and OUT1_P/N go to the DX-M1 position, not fitted on E1M-X V2N (open).
To use the PCIE0 pads, software sets SEL = 1 and PD = 0. No PERST#, CLKREQ# or WAKE# pad on the module.

Figure 15 E1M-X V2N PCIe MUX Connection

8.4 Serial Interfaces

8.4.1 I²C

E1M-X exposes four I²C interfaces. Refer to the Renesas RZ/V2N series datasheet for full details. External pull-ups are required.

> **Note:** The I2C3 interface is connected to the secondary MCU on E1M-X. It is handled by the Alp SDK™ from the main MPU.

8.4.2 On-module I²C Buses

Two I²C buses carry the module's own control devices (7-bit addresses):

Bus	Level and connection	Devices
GP_I2C	3.3 V, always on. Pads AO3 (GP_I2C.SCL) / AP3 (GP_I2C.SDA). 4.7 kΩ pull-ups to +3V3_AON on the module.	Power controller 0x08; RTC (RV-3028-C7) 0x52.
BRD_I2C	1.8 V, on the module only. RZ/V2N P07 (SCL) / P06 (SDA). 1.5 kΩ pull-ups to VDD1G_1P8.	PMIC; clock generator (5L35023B-000NLGI) 0x69; OPTIGA™ Trust M secure element 0x30; temperature sensor (TMP112) 0x40; GD32 I/O MCU 0x70; and, through the level-shifter bridge, 0x08 and 0x52.

Table 19 On-module I²C Buses and Addresses

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While the module runs, two PMX100UNZ level shifters (gate VDD1G_1P8) bridge GP_I2C onto BRD_I2C, so the RZ/V2N reaches the power controller and the RTC on its board bus. With the module off, GP_I2C stays powered from +3V3_AON. Only the RZ/V2N addresses the power controller, the RTC and the PMIC; the GD32 must not.

> **Warning:** Fit no carrier pull-ups on GP_I2C (AO3 / AP3), and keep both pads high-impedance whenever module 5 V is absent.

8.4.3 I^{3}C

E1M-X exposes one I^{3}C interface. Refer to the Renesas RZ/V2N series datasheet for full details. External pull-ups are required.

8.4.4 UART

E1M-X exposes two UART interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.5 SPI

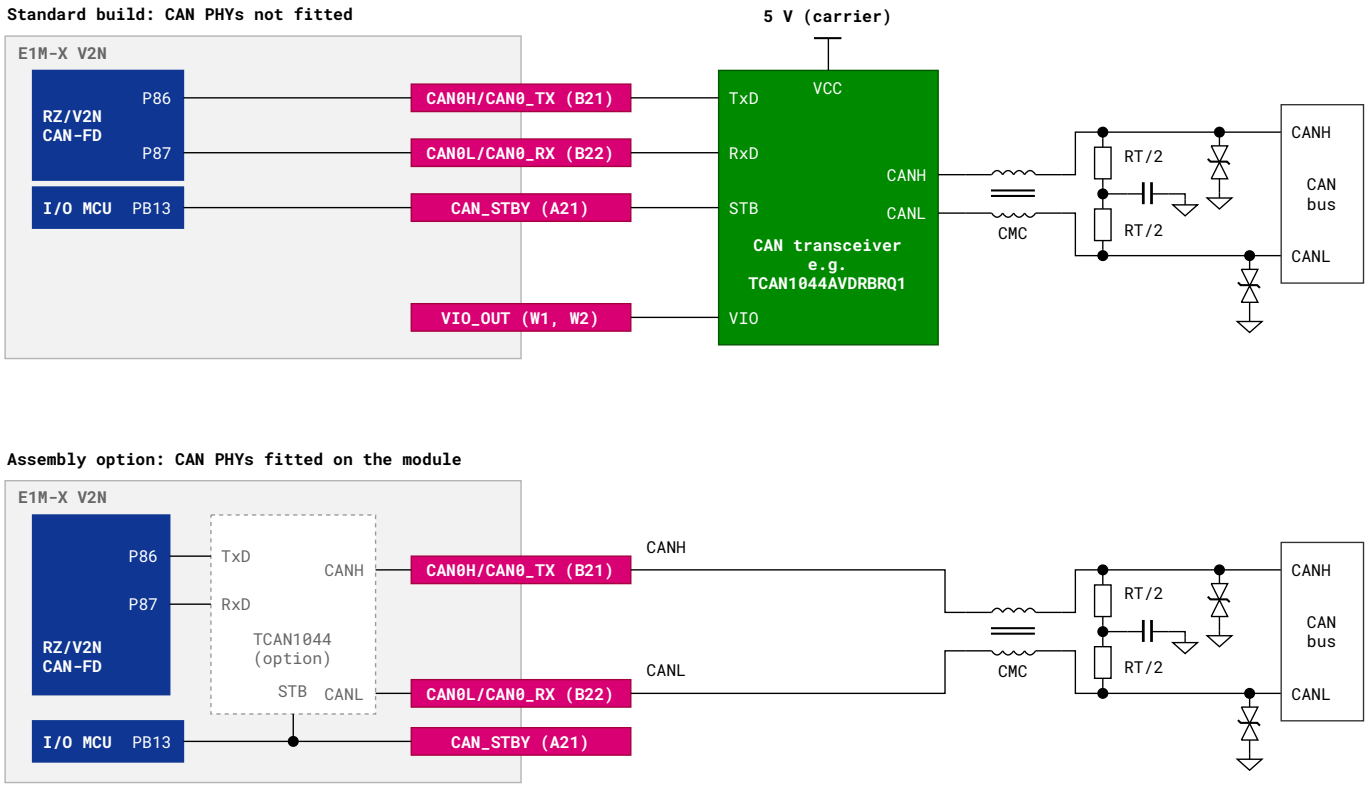
E1M-X exposes three SPI interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.6 I^{2}S

E1M-X exposes two I^{2}S interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.7 CAN Bus

E1M-X includes two optional CAN-BUS PHYs to simplify carrier-board hardware design. When the internal PHY is used, the user must add termination, ESD, and EMI protection components on the carrier board.



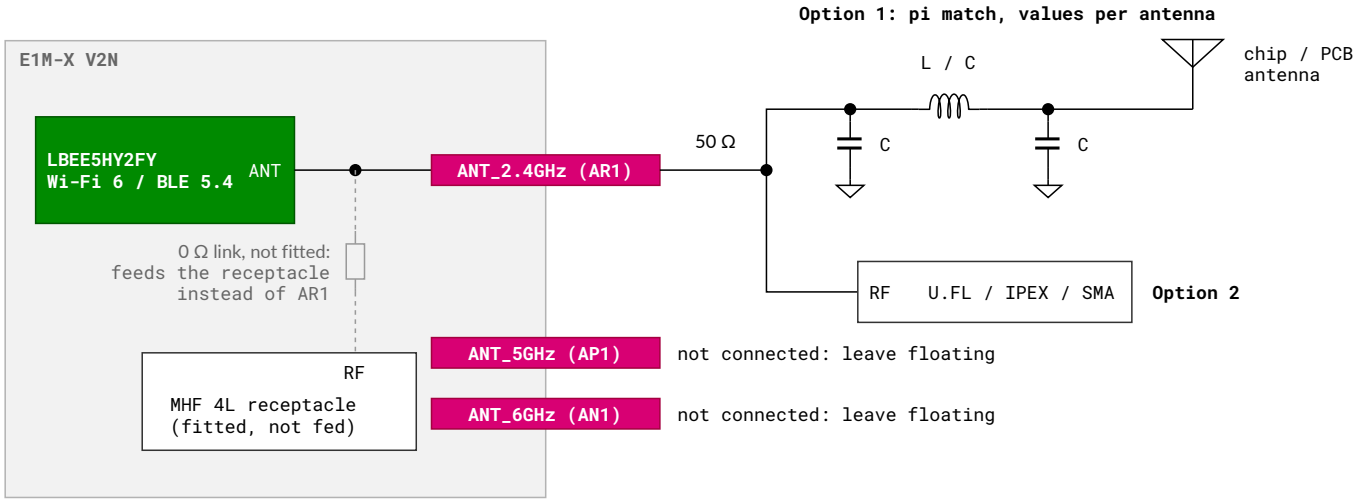
RT = 120 Ω, fitted only at the two ends of the bus (ISO 11898-2). CAN1: same circuit on CAN1H/CAN1_TX (B24), CAN1L/CAN1_RX (B25); CAN_STBY (A21) is shared by both channels. The on-module PHY option runs from VDD_5V_IN, with VIO from the module 1.8 V rail.

Figure 16 E1M-X V2N CAN Connection: Standard Build and CAN PHY Assembly Option

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8.5 Wireless Module & Antenna

E1M-X V2N integrates the Murata LBEE5HY2FY Wi-Fi 6 + BLE 5.4 combo module (based on Infineon CYW55513) on-module per **E1M Spec** §6.5. The radio has a single RF output for all bands, routed to the ANT_2.4GHz pad (AR1); the carrier continues it on a 50 Ω controlled-impedance trace to a U.FL connector or a PCB antenna.



AR1 carries every band of the radio (Wi-Fi 2.4 / 5 / 6 GHz and Bluetooth), fed through an on-module 0 Ω link.
Carrier: option 1 or 2 (one only).
Use only a certified antenna (Regulatory Information).

Figure 17 E1M-X V2N Antenna Connection

8.5.1 RF Characteristics

Symbol	Description	Min	Typ	Max	Unit
Wi-Fi 6 (802.11ax)					
$f_{op,2.4}$	2.4 GHz band operating range	2400	–	2483.5	MHz
$f_{op,5}$	5 GHz band operating range	5150	–	5850	MHz
$f_{op,6}$	6 GHz band operating range	5945	–	7125	MHz
P_{TX}	TX output power (MCS0, 2.4 GHz)	–	TBD	TBD	dBm
P_{RX}	RX sensitivity (MCS0)	TBD	–	–	dBm
η	Max PHY throughput (single stream)	–	143	–	Mbps
Bluetooth LE 5.4					
$f_{op,BLE}$	Operating frequency range	2402	–	2480	MHz
$P_{TX,BLE}$	TX output power	–	TBD	TBD	dBm
$P_{RX,BLE}$	RX sensitivity (1 Mbps)	TBD	–	–	dBm

Table 20 E1M-X V2N Wi-Fi 6 / BLE RF Characteristics

8.5.2 Antenna Options

The E1M-X V2N has **one** antenna pad, ANT_2.4GHz (AR1), which carries every band of the radio (Wi-Fi 2.4 / 5 / 6 GHz and Bluetooth). ANT_5GHz (AP1) and ANT_6GHz (AN1) are not connected. Antenna options:

1. **Carrier-board PCB antenna** — route ANT_2.4GHz as a 50 Ω controlled-impedance trace to a chip / PCB antenna.
2. **Carrier-board RF connector** — extend the 50 Ω trace to a U.FL / IPEX / SMA connector on the carrier.
3. **On-module MHF 4L receptacle** — the receptacle is fitted but not fed: the standard build feeds AR1 only. Feeding the receptacle instead of AR1 is an assembly option (a 0 Ω change on the module). Contact Alp Lab for this variant.

Maximum antenna gain to maintain regulatory compliance is TBD dBi per band.

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8.5.3 Regulatory Information

The on-module combo radio is pre-certified for the regions below. Reusing the module's certifications on the customer's end product requires following the integration guidelines (antenna gain, RF trace, enclosure) from the certification report.

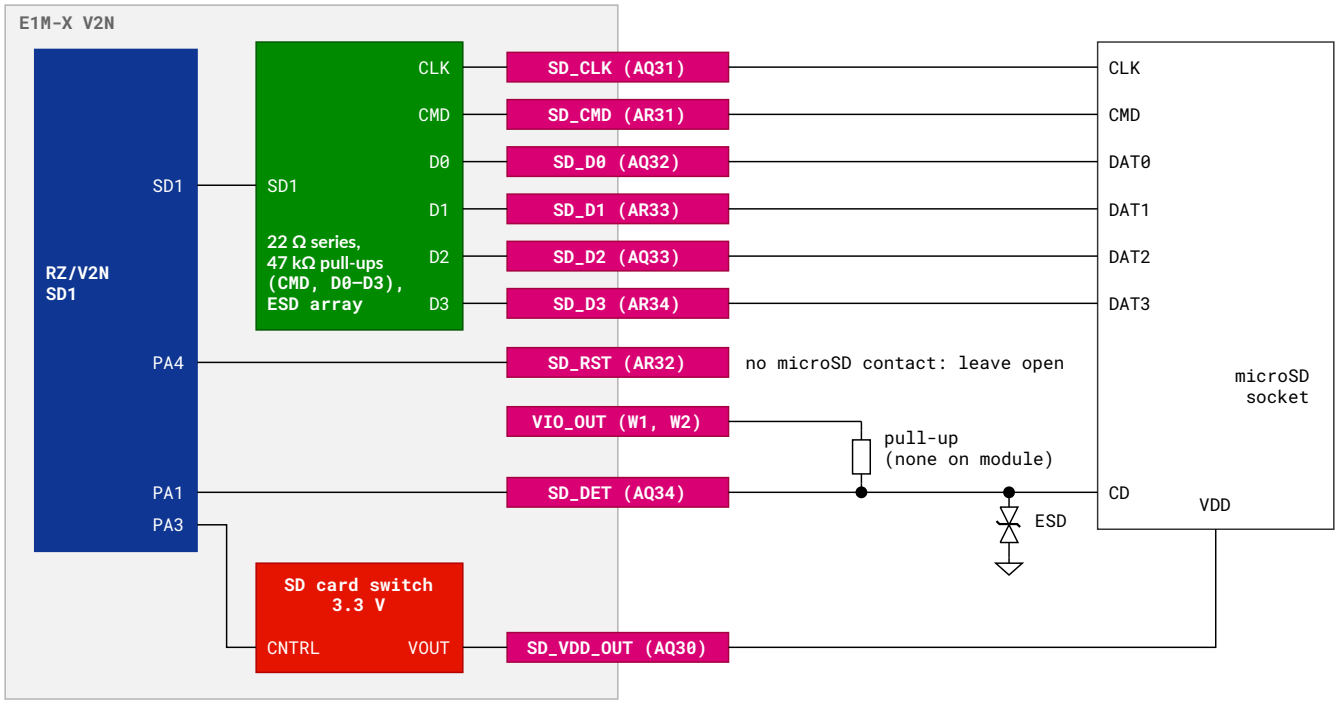
Region	Standard	Certificate ID	Notes
United States	FCC Part 15	TBD	Modular grant pending.
Europe	RED / CE	TBD	–
Canada	ISED RSS-247	TBD	–
Japan	MIC (Japan)	TBD	–

Table 21 Wireless Regulatory Approvals

> **Warning:** Certifications apply only when the module is used with the antenna(s) listed in the certification report. Using an unlisted antenna voids the modular grant and requires re-certification on the customer's end product.

8.6 SD Card

E1M-X supports an external µ SD card over the SDIO interface. The SDIO lines have ESD protection and 22 Ω series resistors on the module, plus 47 kΩ pull-ups on SD_CMD and SD_D0–SD_D3. SD-card power (3.3 V) is supplied by E1M-X via SD_VDD_OUT, switched on by the RZ/V2N; the signal level switches between 3.3 V and 1.8 V on the module. SD_DET has no pull-up on the module.



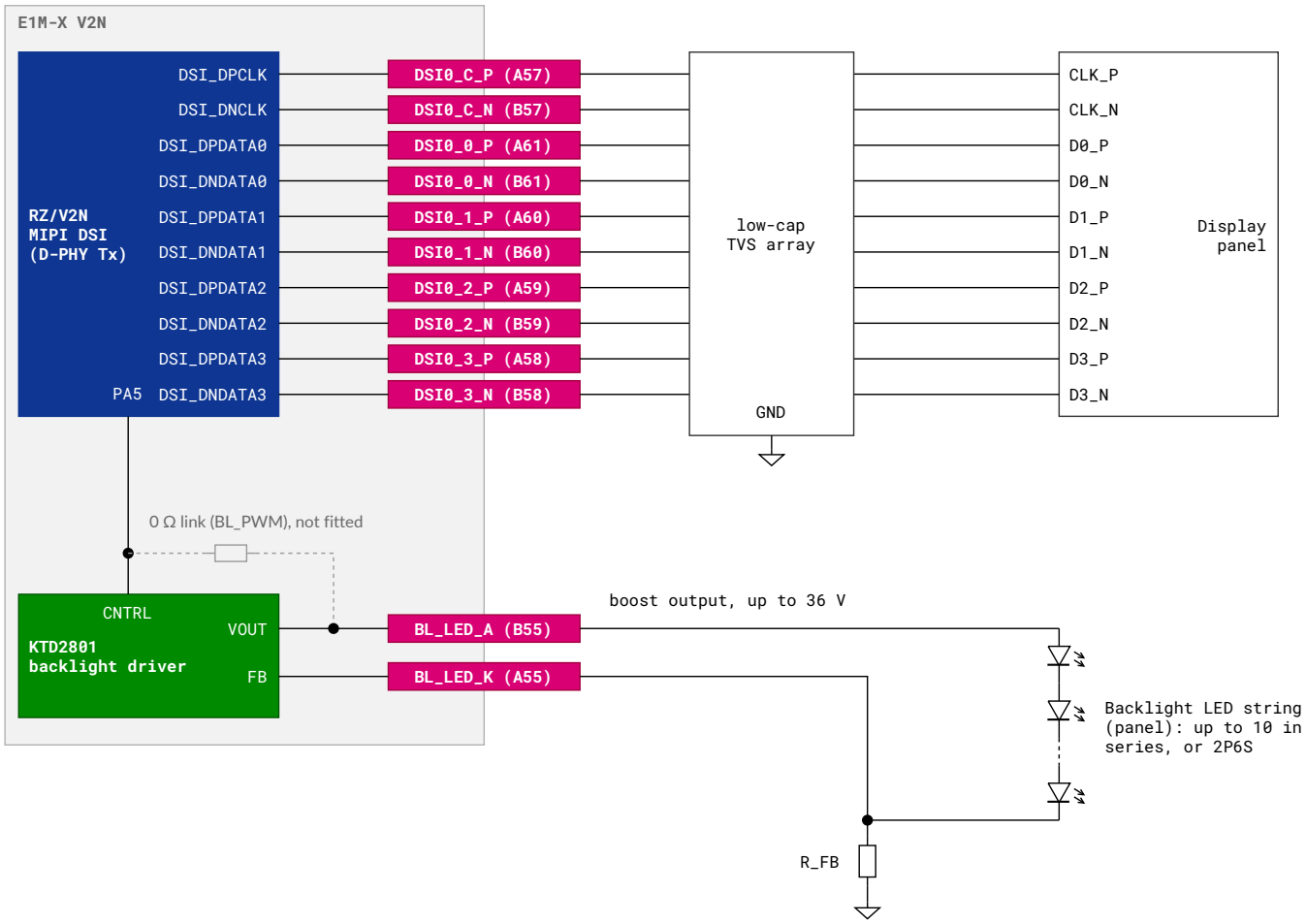
SD_CLK, SD_CMD, SD_D0–SD_D3: connect directly; series resistors, pull-ups and ESD are on the module. SD_VDD_OUT is 3.3 V; the module switches the signal level between 3.3 V and 1.8 V.
SD_RST: leave floating if unused.

Figure 18 E1M-X V2N SD Card Connection

8.7 MIPI DSI Display & Backlight Controller

Renesas RZ/V2N has a 4-lane MIPI DSI interface for an external display, supporting up to FHD resolution. The RZ/V2N also includes an internal 3D GPU (Arm Mali™-G31) that can accelerate display rendering.

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I_LED,max = 200 mV / R_FB (R_FB on the carrier; none on the module).
Assembly option: with the 0 Ω link fitted, BL_LED_A carries BL_PWM and the driver is not fitted.

Figure 19 E1M-X V2N MIPI DSI and Backlight Connection (carrier side)

E1M-X has a backlight boost driver (Kinetic KTD2801ECD-TR, 36 V over-voltage protection) for external screens, controlled directly from the Alp SDK™. The driver is optional; outputs are configured via the BL_LED_A and BL_LED_K pins. The driver supports up to 10 LEDs in series, or 2P6S.

If the backlight driver is not needed, the BL_PWM signal can be brought out on the BL_LED_A pad (B55) to drive an external backlight driver. This is an assembly option (a 0 Ω link on the module, not fitted in the standard build); contact Alp Lab for this variant. The MIPI DSI interface does not include on-module EMI or ESD protection; protect the DSI lanes with a low-capacitance TVS array on the carrier board.

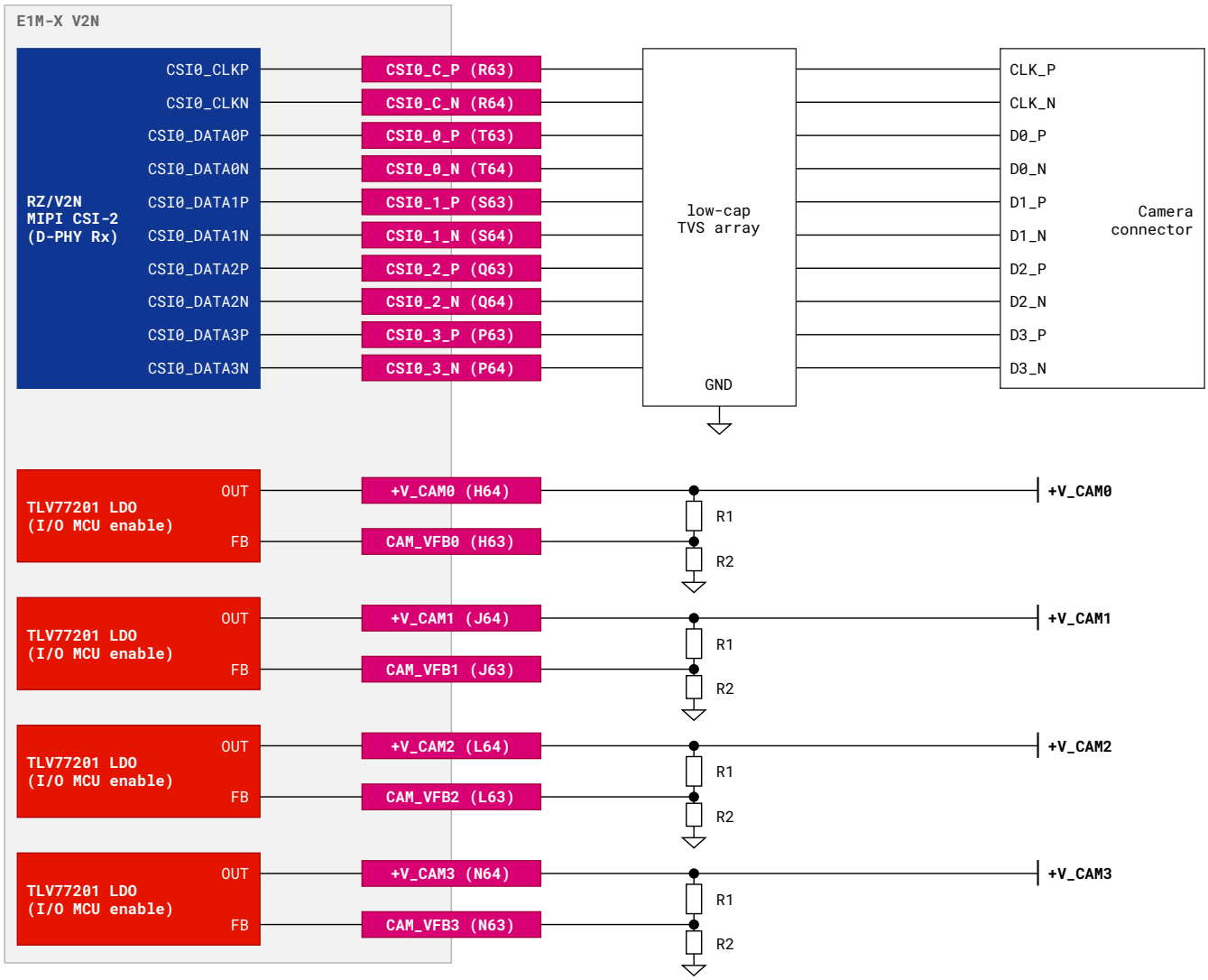
Connect the LED string between BL_LED_A (boost output) and BL_LED_K (driver feedback input), and the feedback resistor R_{FB} from BL_LED_K to GND on the carrier; the module has no R_{FB}. The full-scale LED current is:

$$I_{\mathrm{LED,max}} = 200 \frac{\mathrm{mV}}{R_{\mathrm{FB}}}$$

8.8 MIPI CSI Camera

Renesas RZ/V2N has two 4-lane MIPI CSI interfaces for external cameras. The RZ/V2N also includes an internal ISP (Arm Mali™-C55) that can accelerate image processing.

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V_CAM = 0.6 V × (1 + R1 / R2); R1 + R2 <= V_OUT / (100 × I_FB). Set range 0.6–3.3 V, 300 mA max per LDO. LDO input: 3.3 V camera rail; V_CAM stays below 3.3 V by the LDO dropout (0.745 V at 300 mA).
CSI1: same lane circuit on CSI1_C_P/N (X63/X64), CSI1_0 (Z63/Z64), CSI1_1 (Y63/Y64), CSI1_2 (W63/W64), CSI1_3 (V63/V64). +V_CAM0..3 supply the cameras.

Figure 20 E1M-X V2N MIPI CSI-2 Camera Connection and Camera LDOs (carrier side)

E1M-X supports direct camera implementation via on-board LDOs. Place the feedback resistors as close as possible to the CAM_VFBx pins. The MIPI CSI interface does not include on-module EMI or ESD protection; protect the CSI lanes with a low-capacitance TVS array on the carrier board.

The output voltage is set by the divider:

$$V_{\mathrm{CAM}} = 0.6\ \mathrm{V} \times \left(1 + \frac{R_1}{R_2}\right)$$

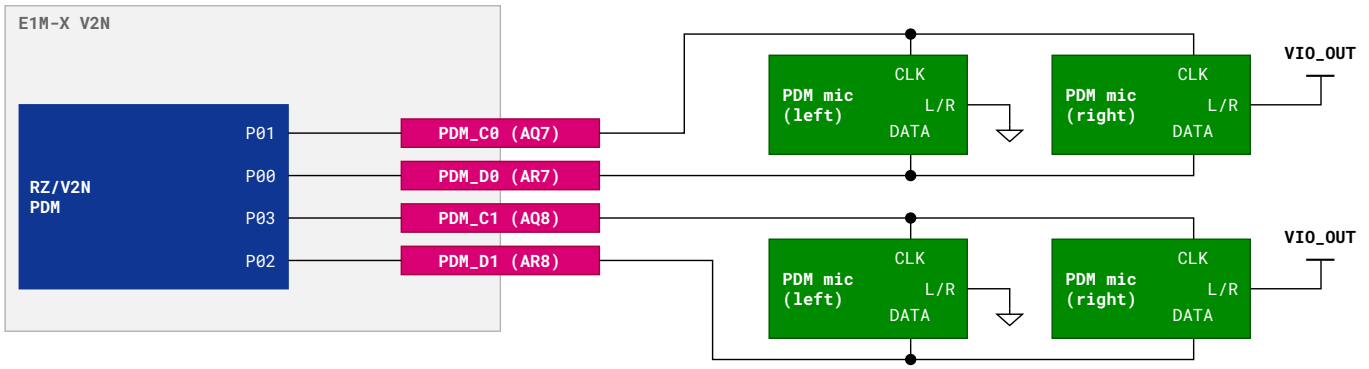
To minimise feedback-pin current error, set the divider current to 100 × the maximum feedback-pin current. The resulting series resistance limit is:

$$R_1 + R_2 \leq \frac{V_{\mathrm{OUT}}}{I_{\mathrm{FB}} \times 100}$$

8.9 Microphone – PDM

E1M-X supports up to 4 digital microphones over 2 PDM interfaces.

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L/R high and the microphone supply: VIO_OUT (W1, W2), so that both match the module I/O level.

Figure 21 E1M-X V2N PDM Microphone Connection (two microphones per data line)

Refer to the E1M-X hardware design guide for full details.

8.10 Analog Inputs

E1M-X has 8 analog input channels (ADC). The analog inputs are connected to the secondary MCU, which has a 12-bit ADC with a 5.3 Msps sampling rate. Analog inputs are referenced to 1V8.

Refer to the secondary-MCU datasheet for electrical characteristics. TBD.

8.11 Analog Outputs

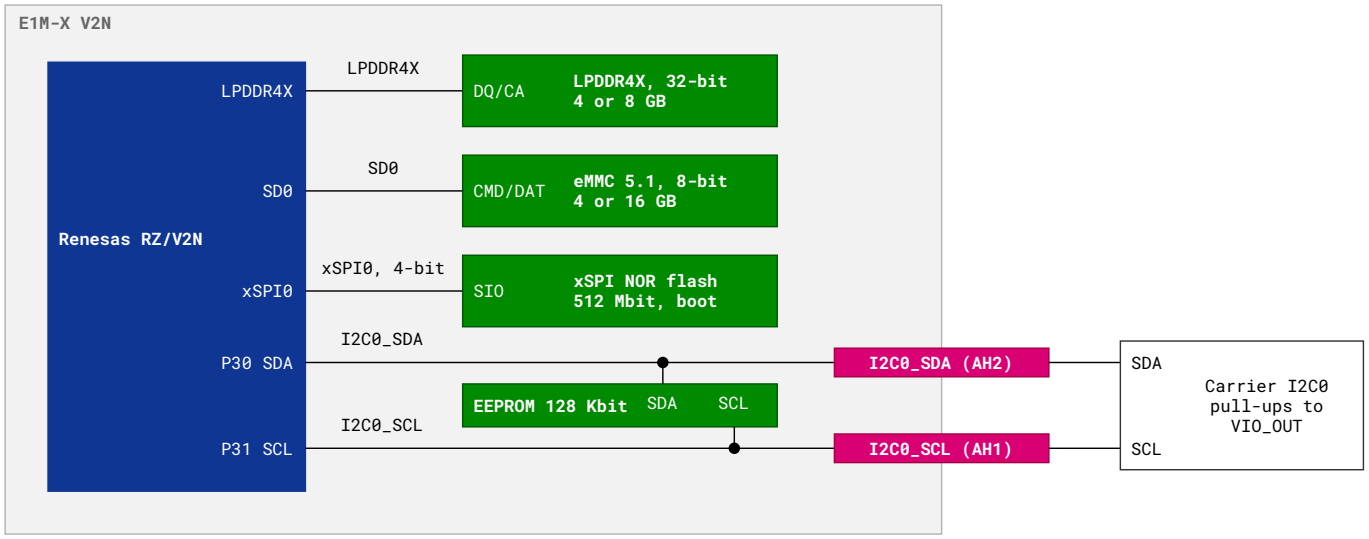
E1M-X has 2 analog output channels (DAC). The analog outputs are connected to the secondary MCU, which has a 12-bit DAC with a 1 kHz sampling rate. Analog outputs are referenced to 1V8.

Refer to the secondary-MCU datasheet for electrical characteristics. TBD.

8.12 Memories

E1M-X offers several memory options:

- **eMMC** — up to 256 GB.
- **LPDDR4X** — up to 8 GB.
- **NOR Flash** — on-module, 512 Mbit (Macronix MX25UW51245G on the RZ/V2N xSPI0, 4-bit), boot-supported.



Memory sizes per MPN (Module Variants). The module has no I2C0 pull-ups.

Figure 22 E1M-X V2N Memory Options

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An optional I²C EEPROM is also available on the board, connected through I2C0 on E1M-X. It can be flashed in production. I2C0 is also accessible on the E1M-X pinout. Refer to the **E1M-X V2N Hardware Design Guide** (HG-V2N-001) for details.

8.13 Secure Element

E1M-X V2N includes an Infineon OPTIGA™ Trust M secure element (SLS32AIA010MLUSON10XTMA2) on the on-module board I²C bus (BRD_I2C) at 7-bit address 0x30, for secure-boot and key-storage applications.

8.14 Clock Tree

The module clocks come from the on-module clock generator (Renesas 5L35023B-000NLGI, BRD_I2C address 0x69) with a 24 MHz crystal, supplied from VDD1G_1P8. Firmware sets the clock generator's crystal load capacitance and output enables over BRD_I2C.

Output	Clock	Destination
REF	24 MHz	RZ/V2N QEXTAL, through 22 Ω.
SE1	32.768 kHz	RZ/V2N RTXIN, through 22 Ω; Wi-Fi / Bluetooth module LPO_IN (WL_32K), through 22 Ω.
SE2	25 MHz (CLK_25M)	Both RTL8211FI-VD-CG Ethernet PHYs, through an on-module buffer (SN74AUP1G34YFPR, supplied from VDD_1V8) and 33 Ω; GD32 oscillator input (OSCIN-PF0), through 22 Ω.
SE3	Audio_CLKB	RZ/V2N P10, through 22 Ω. Output enable OE3 from RZ/V2N P67.
DIFF1	LP-HCSL PCIe reference clock	PCIE0_CLK_P / PCIE0_CLK_N pads (A47 / B47), Section 8.3.
DIFF2	LP-HCSL PCIe reference clock	RZ/V2N PCIE_REFCLKP0 / PCIE_REFCLKN0, through 33 Ω.

Table 22 Clock Generator Outputs

A 22.5792 MHz crystal on the RZ/V2N AUDIO_XTAL / AUDIO_EXTAL clocks the 44.1 kHz audio family.

9 Environmental & Reliability

9.1 Operating & Storage Conditions

Parameter	Symbol	Min	Max	Unit
Ambient operating temperature	T_A	- 40	+85	°C
Storage temperature	T_{STG}	- 40	+125	°C
Relative humidity (operating, non-condensing)	RH	TBD	TBD	%

Table 23 Environmental Conditions

9.2 Reflow Profile

The E1M-X V2N is qualified per IPC/JEDEC J-STD-020 to MSL TBD. The recommended starting profile is the lead-free reflow profile shown in Figure 23: the measured E1M-AEN profile, smoothed, without its zone-boundary kink (an E1M-AEN module, a JTR1000 convection reflow oven, ALPHA OM338 (SAC, Pb-free) solder paste and a VCAM i612D profiler sampling every 0.5 s). On that run the peak package temperature was 240.9–244.3 °C and the time at or above 220 °C 56.5–60.0 s (the measured ranges in the table below); the SAC liquidus is 217 °C. Customers must keep the process within the recommended window in the table below and follow the dry-pack handling instructions in Section 14.2.

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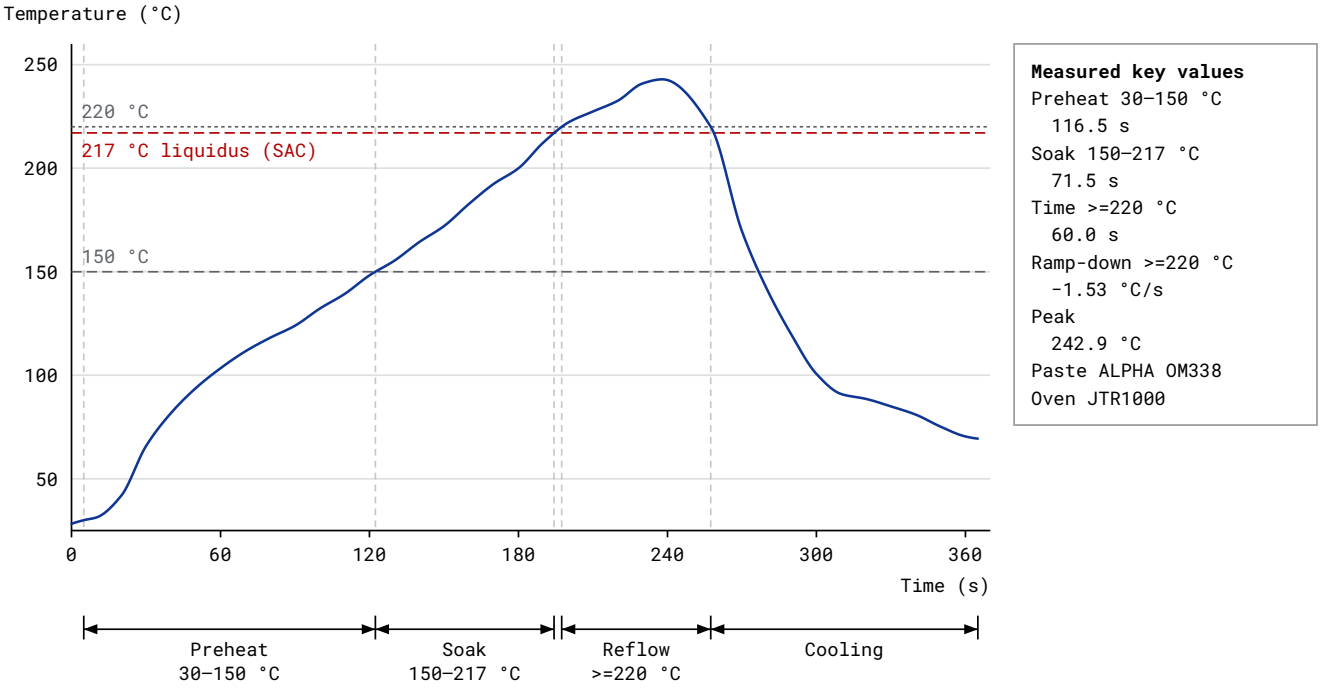


Figure 23 Recommended starting profile: measured E1M-AEN profile, smoothed

Parameter	Window min	Window max	Measured	Unit
Preheat time, 30–150 °C	60	160	116.5–122.0	s
Soak time, 150–217 °C	60	120	70.5–73.5	s
Time at or above 220 °C	45	90	56.5–60.0	s
Ramp-down slope at or above 220 °C	-4	-0.5	-1.53 to -1.66	°C/s
Peak package temperature	230	250	240.9–244.3	°C

Table 24 Reflow Profile Parameters (Pb-free): recommended window and measured values

9.3 Reliability Data

Parameter	Symbol	Value	Unit
Mean Time Between Failures (Telcordia SR-332, T_A = +25 °C)	MTBF	TBD	h
Moisture Sensitivity Level	MSL	TBD	–
Qualified shelf life (in dry-pack)	–	TBD	months

Table 25 Reliability Targets

10 Software & Operating System Support

The E1M-X V2N is supported by the open-source **Alp SDK™**, which provides a unified HAL across all E1M-X variants. Out of the box, the SDK supports:

- **Linux** (Yocto) on the quad Cortex-A55 application cluster. Each SKU has its own Yocto `MACHINE`: `e1m-v2n101-a55`, `e1m-v2n102-a55`, `e1m-v2n103-a55`.

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- **Zephyr RTOS** on the RZ/V2N's internal Cortex-M33 system manager. On `E1M-V2N101` the board target is `alp_e1m_v2n101_m33_sm/r9a09g056n48gbg/cm33`; the Zephyr M33 board trees for `E1M-V2N102` and `E1M-V2N103` are not yet built.

The on-module GD32 I/O-MCU is **not** a customer application target. It runs bridge firmware that Alp Lab programs in production; applications on the RZ/V2N reach the peripherals it owns through the bridge driver (`<alp/chips/gd32g553.h>`), and field updates of the bridge firmware arrive over the bridge link (`update_channel: alp_ota_spi_bridge`). Customer reflashing of the GD32 is supported only to recover a bricked module, with Alp Lab-supplied binaries.

Target / Runtime	Zephyr	Linux (Yocto)
RZ/V2N Cortex-A55 (4 × 1.8 GHz)	–	Yes
RZ/V2N internal M33 (200 MHz)	Yes (E1M-V2N101)	–
GD32 I/O-MCU (Cortex-M33 @ 216 MHz)	Alp Lab bridge firmware	–

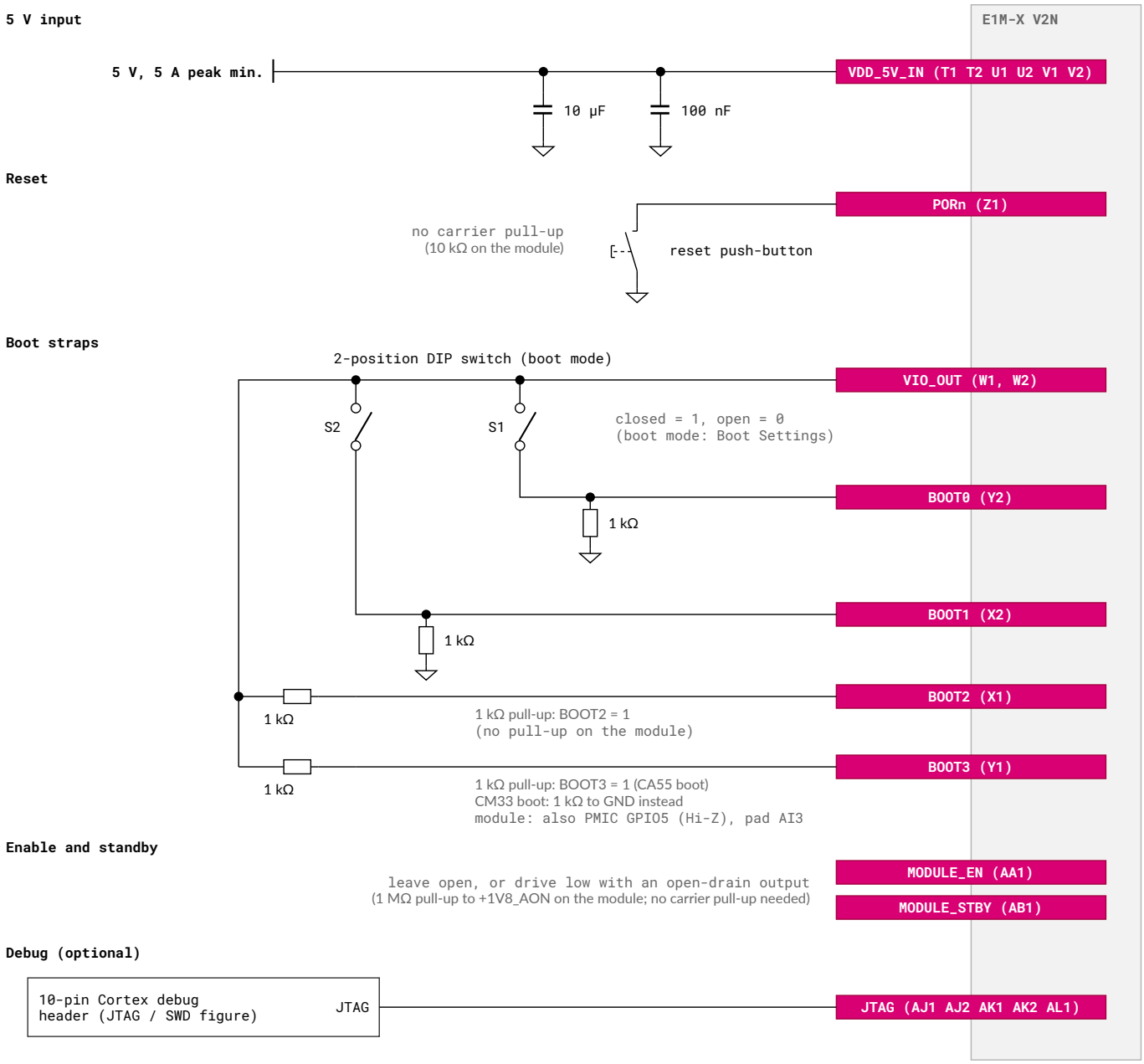
Table 26 Software Support Matrix

> **Note:** See the Alp SDK™ repository (`docs/firmware-quickstart.md` and `docs/soms/v2n.md`) for the per-target board strings and bring-up instructions. For deeper integration patterns, see the Application Notes (AN-001 through AN-010).

11 Reference Schematic

The minimum carrier-board design below brings up an E1M-X V2N with a single 5 V input, reset push-button, boot-mode DIP switch, and JTAG/SWD debug header. All other interfaces (Ethernet, USB, MIPI, PCIe, camera, display) are optional and described per-interface in Section 8.

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All GND pads to the carrier GND plane. The BOOT pads are sampled at the PORn rising edge. Every BOOT strap: 1 kΩ to VIO_OUT for 1, 1 kΩ to GND for 0. An open strap reads 1 (RZ/V2N internal pull-up); do not rely on it. JTAG pads: JTAG_TCK/SWDCLK (AJ1), JTAG_TDI (AJ2), JTAG_TMS/SWDIO (AK1), JTAG_TDO (AK2), JTAG_nRST (AL1).

Figure 24 E1M-X V2N Minimum Reference Circuit (power and control)

Required external components:

- 5 V power source (>= 5 A peak) to VDD_5V_IN (T1, T2, U1, U2, V1, V2).
- Bulk decoupling: 1 × 10 µF + 1 × 100 nF close to VDD_5V_IN.
- Boot-mode 2-position DIP switch from VIO_OUT to BOOT0, BOOT1, with a 1 kΩ pull-down to GND on each line (closed = 1, open = 0).
- 1 kΩ pull-up from VIO_OUT to BOOT2 (X1).
- 1 kΩ pull-up from VIO_OUT to BOOT3 (Y1) for CA55 boot (a 1 kΩ pull-down to GND instead for CM33 boot). On the module BOOT3 is also tied to the PMIC GPIO5 (an input, high impedance) through an on-module 0 Ω link, and so to pad AI3; leave AI3 open.
- MODULE_EN (AA1) and MODULE_STBY (AB1) open, or driven low by an open-drain output (no carrier pull-up needed). GP_I2C (AO3 / AP3) without carrier pull-ups.

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- Reset push-button between PORn (Z1) and GND.
- 10-pin Cortex SWD/JTAG header on JTAG_* pads (optional, for development).

Do not leave a boot strap open: the RZ/V2N internal pull-ups read an open strap as 1, but the carrier sets every strap with its own 1 kΩ resistor.

Optional carrier-board components are described per interface in Section 8, and in detail in **HG-V2N-001**.

12 Compliance & Certifications

12.1 Environmental Compliance

Standard	Description	Status
RoHS 3 (EU 2015/863)	Restriction of hazardous substances	Compliant
REACH (EC 1907/2006)	Substances of very high concern	Compliant
Halogen-free (IEC 61249-2-21)	Br + Cl content limits	TBD
Conflict minerals (Dodd-Frank §1502)	Tin, tungsten, tantalum, gold sourcing	TBD

Table 27 Environmental Compliance

12.2 Wireless Certifications

See Section 8.5.3 for the per-region wireless certification IDs.

12.3 Functional Safety & Industry-specific Compliance

The E1M-X V2N is not currently certified for safety-critical applications (IEC 61508, ISO 26262, IEC 62304, etc.). Contact Alp Lab for the most recent qualification status.

13 Mechanical & Footprint Dimensions

All dimensions are in mm unless otherwise noted.

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13.1 Module Dimensions

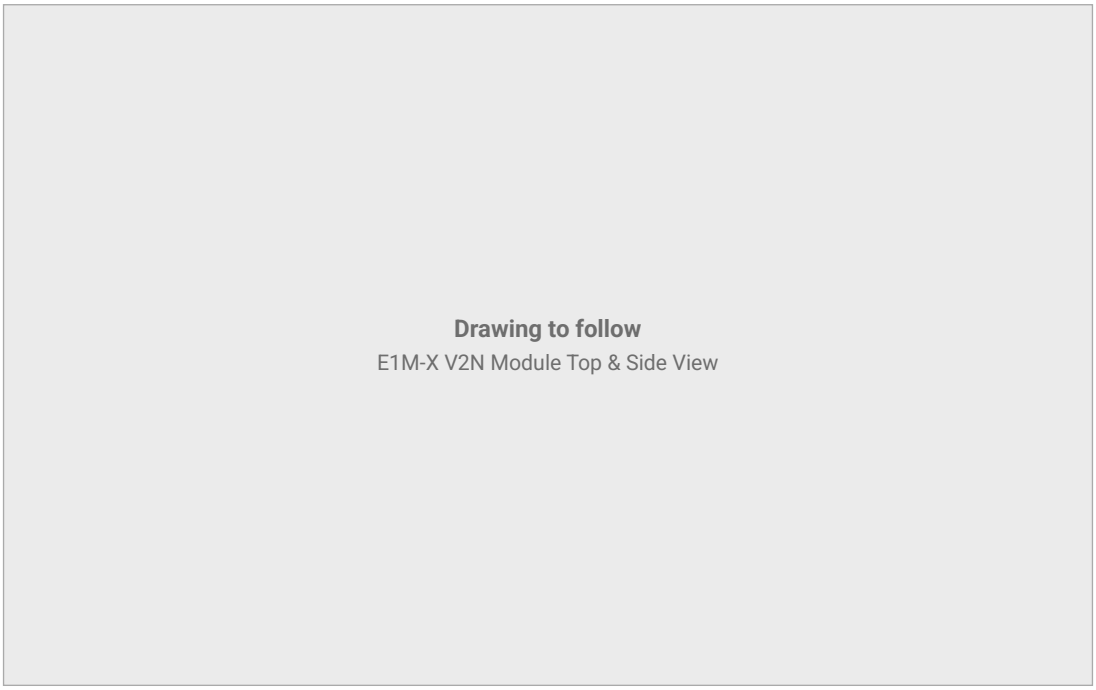


Figure 25 E1M-X V2N Module Top & Side View

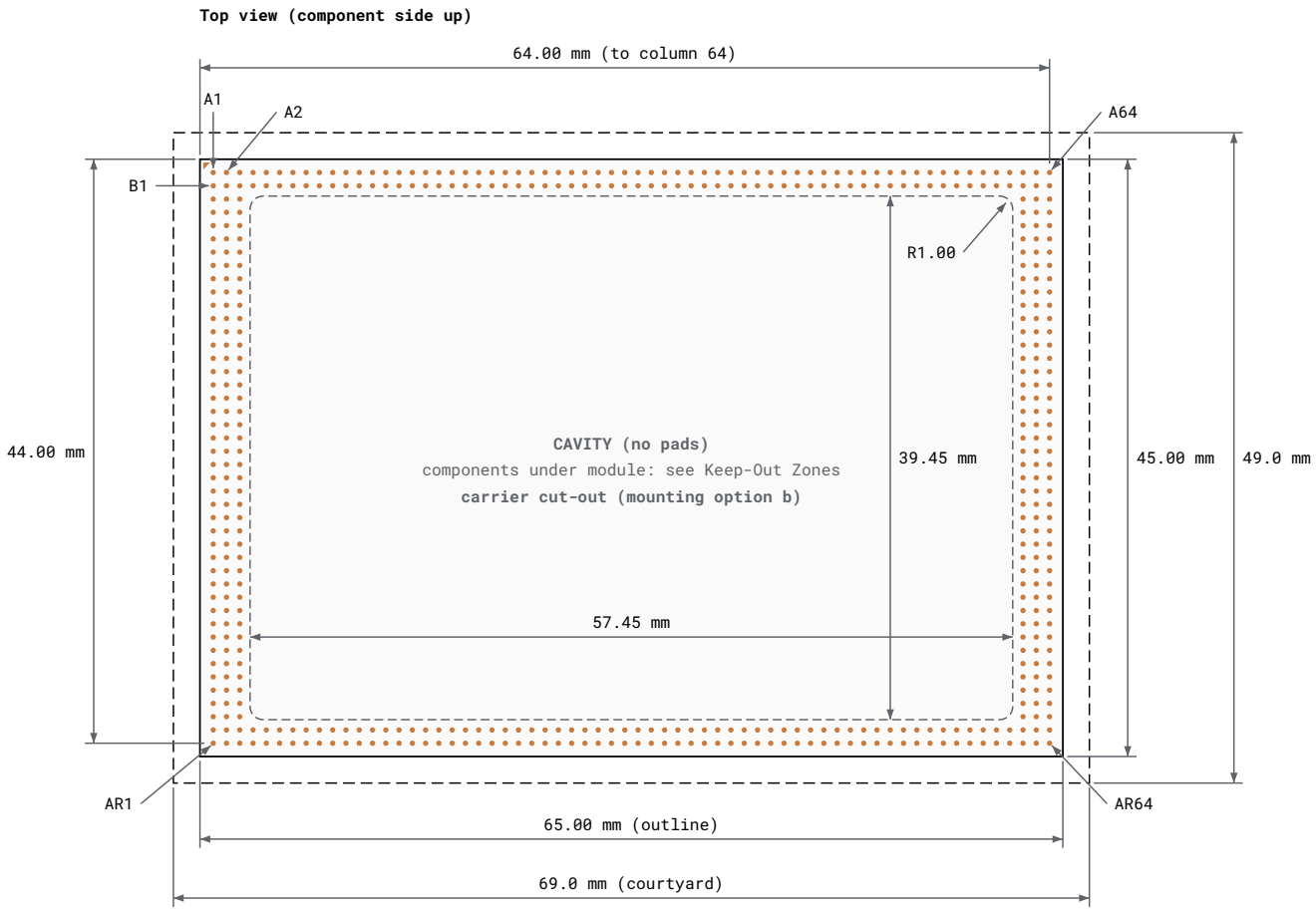
Parameter	Symbol	Min	Max	Unit
Module length	L	64.9	65.1	mm
Module width	W	44.9	45.1	mm
Module height (PCB + tallest component)	H	–	TBD	mm
Module mass	m	–	TBD	g

Table 28 E1M-X V2N Mechanical Dimensions

13.2 Recommended PCB Land Pattern

The recommended carrier-board land pattern follows IPC-7351 nominal density for LGA packages.

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Pad A1 next to the 0.52 mm triangular pin-1 fiducial, centred 1.00 mm from the left and top edges.
Rows A–AR top to bottom, columns 1–64 left to right; 496 pads on a 1.00 mm grid.
Courtyard: 2.0 mm clearance around the module outline, 69.0 mm across x 49.0 mm down.
Dimensions per E1M-STD §5.1.2 (E1M-X footprint) and §5.1.3 (carrier land pattern).

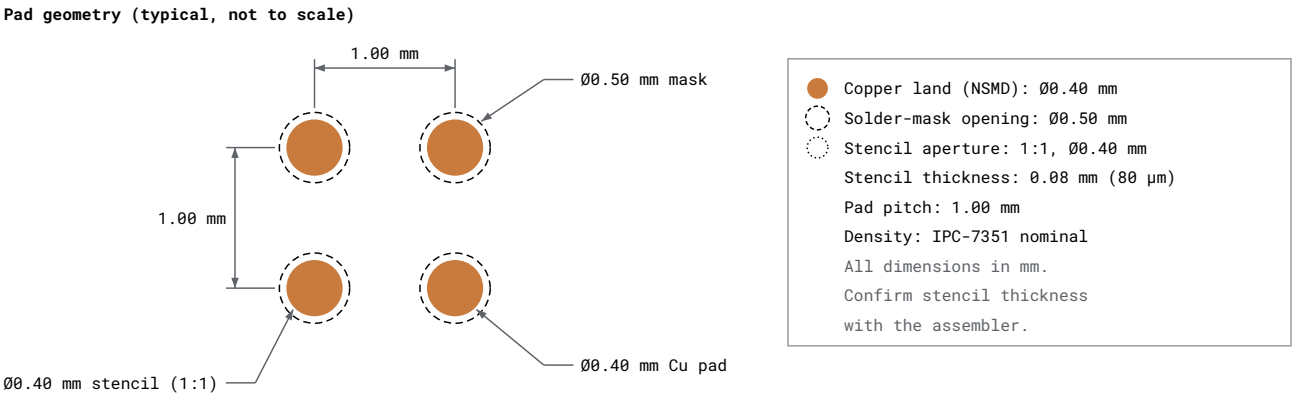


Figure 26 E1M-X V2N Recommended Land Pattern (top view; values per E1M-STD §5.1.2 and §5.1.3)

Parameter	Symbol	Value	Unit
Pad pitch (signal grid)	p	1.00	mm
Pad size (signal)	–	Ø0.40 (round, NSMD)	mm
Solder-mask opening	–	Ø0.50 (NSMD)	mm
Stencil aperture	–	1:1, Ø0.40	mm
Stencil material	–	Nano-coated steel mesh	–

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Parameter	Symbol	Value	Unit
Stencil thickness (recommended)	t	80	µm
Courtyard	–	2.0 mm clearance around the module outline, 69.0 × 49.0	mm

Table 29 Land Pattern Parameters

13.3 Keep-Out Zones

The E1M-X V2N carries components on its bottom side, in the central cavity inside the pad band. A module **shall not** be placed directly on a carrier board. Mount it in one of two ways (Figure 27):

1. **On a spacer PCB:** a spacer PCB between the module and the carrier raises the module so that its bottom-side components clear the carrier (E1M-STD §5.2). The spacer is soldered on both faces: the module LGA pads to the spacer, and the spacer to the carrier.
2. **Over a carrier cut-out:** a through cut-out in the carrier the size of the module's central cavity, 57.45 mm across × 39.45 mm down with R1.00 corners, its left edge 3.775 mm from the left outline edge and its top edge 2.775 mm from the top outline edge (E1M-STD §5.1.2). The bottom-side components sit in the cut-out.

With either option the carrier **shall** have no components inside the cavity outline (57.45 mm across × 39.45 mm down, R1.00 corners, 3.775 mm from the left and 2.775 mm from the top outline edge). The spacer-PCB thickness and the maximum bottom-side component height are TBD; E1M-STD §5.2 does not specify them. RF traces (especially the antenna feed) must be routed away from high-current digital paths.

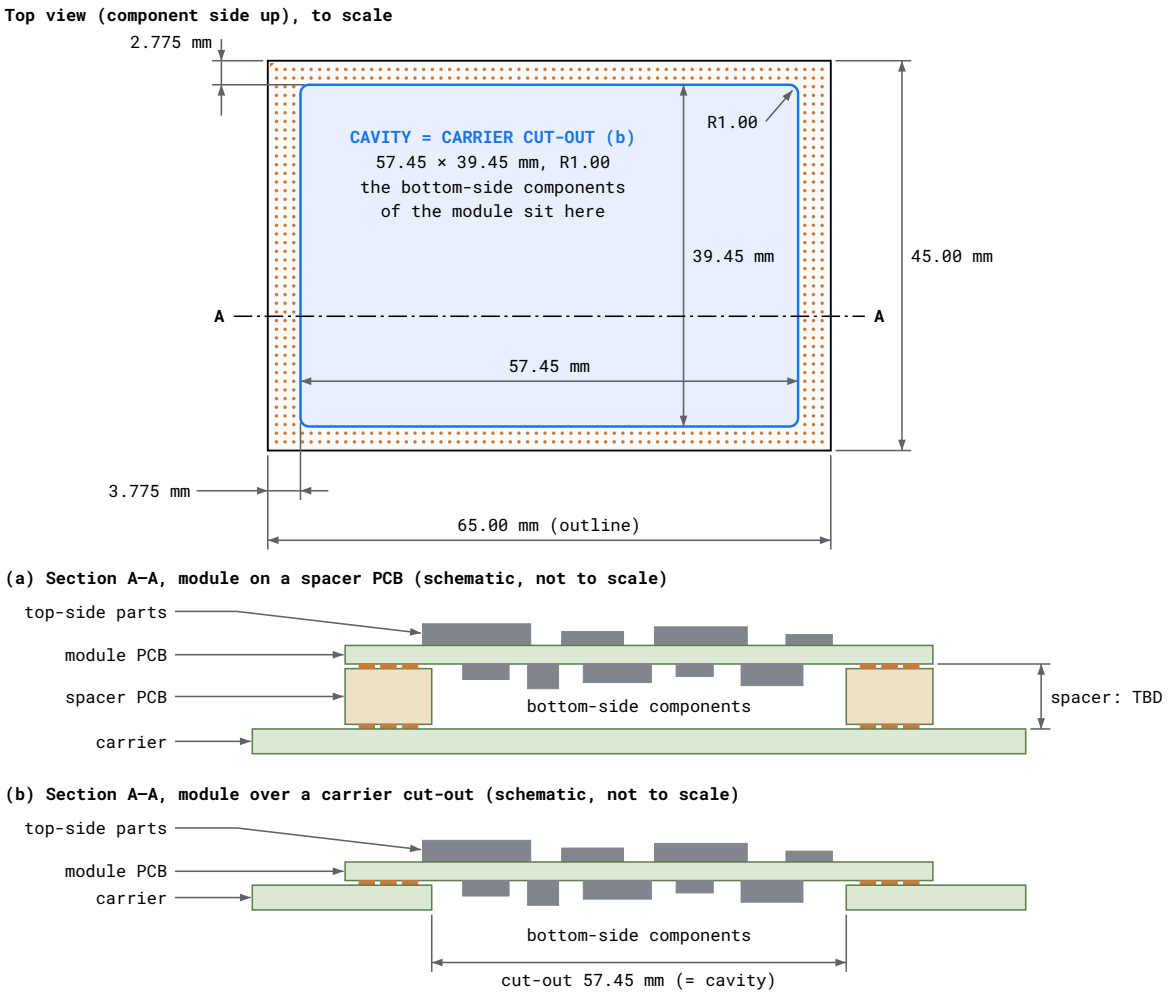


Figure 27 E1M-X V2N mounting: cavity = carrier cut-out (top view); section A–A, spacer PCB / cut-out

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13.4 Module Marking

Each module is laser-marked on the top side with:

- Manufacturer logo (Alp Lab)
- Full MPN (e.g. `E1M-V2N101`)
- Production date code (YYWW)
- Serial number (10 characters)
- FCC ID, ISED IC, MIC marks (where applicable)
- Wi-Fi MAC address (last 4 digits)

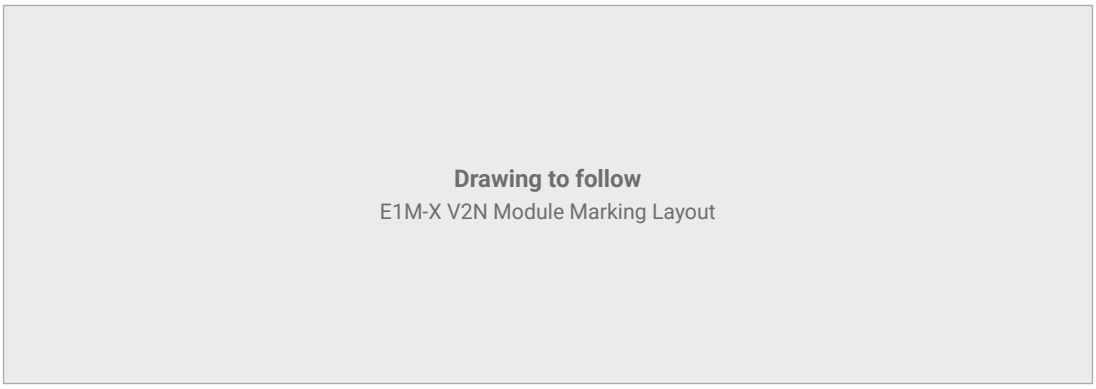


Figure 28 E1M-X V2N Module Marking Layout

14 Packaging

14.1 Tray

A JEDEC-compliant tray is available for low-volume or prototyping orders.

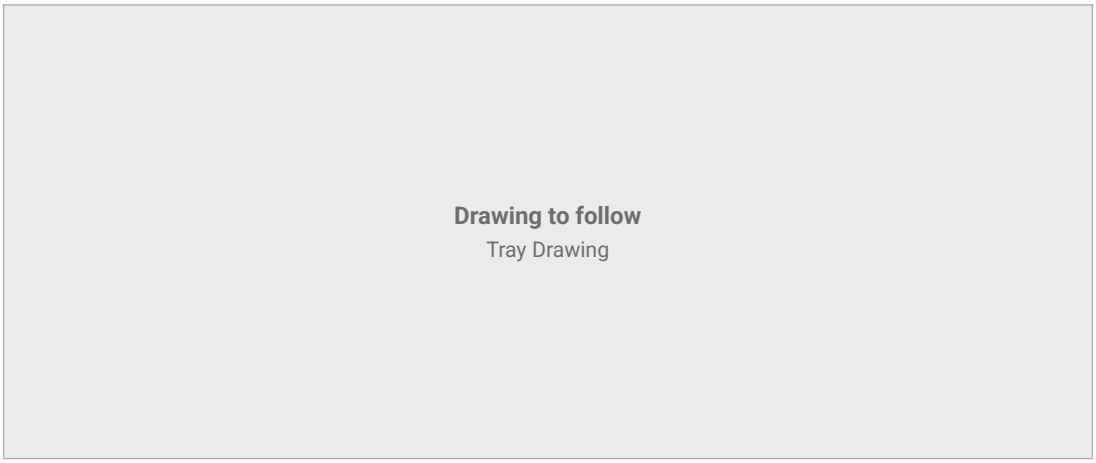


Figure 29 Tray Drawing

14.2 MSL & Handling

The E1M-X V2N is classified to Moisture Sensitivity Level (MSL) TBD per IPC/JEDEC J-STD-020. Modules are shipped in dry-pack with desiccant and a humidity-indicator card.

After opening the dry-pack:

- Floor life: TBD hours at <= 30 °C / <= 60% RH.
- If floor life is exceeded before reflow, bake at TBD °C for TBD h before assembly.

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Refer to IPC/JEDEC J-STD-033 for full moisture/reflow handling procedures.

15 Ordering Information

15.1 MPN Decoder

Field	Example	Description
Family	E1M	Edge-1 AI Module standard footprint.
Form factor	-V	Implied 45 × 65 mm E1M-X (V prefix on the SoC family code).
Product line	V2N	Renesas RZ/V2N (without DeepX DX-M1). Sibling line V2M adds the DX-M1.
Variant code	101	Three-digit code identifying the memory configuration: 101 = 4 GB LPDDR4X + 4 GB eMMC, 102 = 8 GB LPDDR4X + 16 GB eMMC, 103 = 4 GB LPDDR4X + 16 GB eMMC. It is not a hardware-revision field.

Table 30 E1M-X V2N MPN Convention

Note: The module hardware revision is not encoded in the MPN. It is recorded in the on-module identity EEPROM and read by the Alp SDK™ at run time.

Note: Example: **E1M-V2N101** = E1M-X form factor, RZ/V2N SoC, variant 101 (4 GB LPDDR4X + 4 GB eMMC).

15.2 Ordering Matrix

MPN	CPU	LPDDR4X	eMMC	AP cores	RT cores	AI	Temp. (°C)
E1M-V2N101	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 4 GB	A55 4 × 1.8 GHz	V2N M33 1 × 200 MHz I/O MCU M33 1 × 216 MHz	V2N: 4 TOPS	-40 to +85
E1M-V2N102		8 GB	eMMC 5.1, 16 GB				
E1M-V2N103		4 GB	eMMC 5.1, 16 GB				

Table 31 Ordering Information

All configurations above include:

- 2.4 GHz / 5 GHz / 6 GHz Wi-Fi® + Bluetooth® 5.4 combo module
- 2 × 1 Gbit Ethernet PHY
- 1 × display backlight driver
- 4 × LDOs for external cameras
- NOR Flash (512 Mbit)
- I/O MCU Cortex-M33 (216 MHz)
- Secure element (Infineon OPTIGA™ Trust M)
- EEPROM
- RTC
- Temperature sensor

RoHS-compliant. Contact Alp Lab for custom assembly variants (lead finish, ball material, etc.).

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16 References & Related Documents

Ref.	Title	Source
[1]	Renesas RZ/V2N Hardware Reference Manual	Renesas Electronics
[2]	Renesas RZ/V2N Series Datasheet	Renesas Electronics
[3]	E1M™ Specification	E1M-STD-1.0 / github.com/alplabai/e1m-spec
[4]	E1M-X V2N Hardware Design Guide	Alp Lab (HG-V2N-001)
[5]	E1M-X EVK User Guide	Alp Lab (UG-E1M-X-001)
[6]	E1M-X EVK Getting Started Guide	Alp Lab (QS-E1M-X-EVK-001)
[7]	Alp SDK™ Documentation	github.com/alplabai/alp-sdk
[8]	IPC/JEDEC J-STD-020 – Reflow Profile	JEDEC
[9]	IPC/JEDEC J-STD-033 – Moisture/Reflow Handling	JEDEC

Table 32 Related Documents

17 Revision History

Revision	Changes	Date
0.1	• Initial draft (docx port).	December 2025
0.2	• SoM-typical sections added: Module Variants, Recommended Operating Conditions, ESD & Latch-up, Thermal Characteristics, Power Architecture / Power-Up Sequence / Power Consumption, Boot Modes (top-level), Reset & Module Enable, JTAG / SWD Debug, Wireless RF/Antenna/Regulatory subsections, Environmental & Reliability, Software & OS Support, Reference Schematic, Compliance & Certifications, Mechanical & Footprint subsections, Packaging subsections, MPN Decoder, References, Legal Notices.	May 2026
0.3	• Pin-out drawing added: top-view, colour-coded 496-pad E1M-X diagram generated from the pin tables. • On-module interface ESD/EMI protection removed except on the SDIO / SD-card interface; carrier board must now provide ESD/EMI protection on Ethernet, MIPI DSI, and MIPI CSI. • Reflow profile populated (Pb-free, ALPHA OM338, peak 241–244 °C) with a parameters table. • SMT stencil specified (nano-coated steel mesh, 80 µm).	June 2026
0.4	• Cover page: replaced the block-diagram placeholder with front/back product photos of the E1M-X V2N module.	July 2026
0.5	• Cover photos swapped to transparent-background versions.	July 2026
0.6	• Corrected the Alp SDK and E1M Specification repository links: the alpDevs GitHub organisation does not exist, so every link 404'd; the canonical organisation is alplabai.	July 2026
0.7	• Recommended Operating Conditions: removed the Junction operating temperature (T_J) row; the module is specified over the ambient range (- 40 °C to +85 °C). • Power-Up & Reset Sequence: clarified that the on-module GD32 supervisor sequences the internal rails and no carrier-side rail sequencing is required, separate from the carrier-side control-signal bring-up steps.	July 2026
0.8	• Module Variants and Ordering Matrix: added E1M-V2N103 (32 Gbit LPDDR4X + 128 Gbit eMMC 5.1, same silicon and pin-out as E1M-V2N101/E1M-V2N102). • Software & OS Support: replaced the board targets and runtime matrix with what Alp SDK™ v0.17.0 ships – Linux (Yocto) on the A55 cluster per SKU MACHINE, Zephyr on the RZ/V2N Cortex-M33 system manager (alp_e1m_v2n101_m33_sm/r9a09g056n48gbg/cm33 on E1M-V2N101). Bare-metal and Zephyr-SMP support on the A55 is no longer claimed.	October 2026

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Revision	Changes	Date
	• The GD32 I/O-MCU is no longer listed as a customer application target: it runs Alp Lab-programmed bridge firmware, updated in the field over the bridge link; customer reflashing is for bricked-module recovery only. • MPN Decoder: replaced the memory-tier digit + two-digit hardware-revision reading, which E1M-V2N103 contradicts, with a three-digit variant code for the memory configuration; the hardware revision is held in the on-module identity EEPROM, not in the MPN.	
0.9	• New figures drawn from the module netlist: block diagram, power architecture, power-up sequence, boot flow, reset timing, JTAG / SWD header, Ethernet, CAN, antenna, SD card, MIPI DSI + backlight, MIPI CSI-2 + camera LDOs, PDM, memory options and minimum reference circuit. • Corrections from the netlist: the Ethernet PHY is the RTL8211FI-VD-CG (was RTL8211FDI); the main PMIC is the Qorvo ACT88760, next to the Renesas DA9292 buck; the NOR flash is 512 Mbit (was 128 Mbit / TBD); the SD pull-ups are 47 kΩ (was 1 MΩ) and SD_VDD_OUT is a switched 3.3 V card supply, the signal level switching on the module (was 1.8 / 3.3 V auto); one antenna pad (AR1) carries all bands and feeding the MHF 4L receptacle is an assembly option (was three pads, one per band); MODULE_STBY is pulled up to VDD_5V_IN and goes to the PMIC and RTC (was 1V8 / GD32); BOOT2 (X1) reaches the RZ/V2N MD_BOOT3 strap, has no pull-up on the module and needs a 1 kΩ carrier pull-up to VIO_OUT (was not connected; pin table, Boot Modes, Reference Schematic, minimum reference circuit and boot flow figures); IO0–IO6, IO17–IO22 and IO24 are not connected on E1M-X V2N (was GPIO). • Backlight: LED current corrected to $I_{LED,max}$ = 200 mV / R_{FB} (was 95 mV), per the KTD2801 feedback reference. • Power Architecture and Power-Up & Reset Sequence: the ACT88760 PMIC sequences the rails and releases PORn and the GD32 reset (was the GD32 supervisor); the GD32 switches only the camera LDOs. • BOOT3 (Y1): noted that it is tied on the module to the PMIC GPIO5 through a 0 Ω link (pad AO3). The PMIC GPIO5 is an input (high impedance); the carrier fits a 1 kΩ pull-up to VIO_OUT for CA55 boot (pin table, Boot Modes, Reference Schematic, minimum reference circuit and boot flow figures). • Boot straps: every strap (BOOT0–BOOT3) takes a 1 kΩ carrier resistor, a pull-up to VIO_OUT for 1 or a pull-down to GND for 0 (BOOT3: 1 kΩ pull-down for a Cortex-M33 boot). The BOOT0 / BOOT1 DIP-switch pull-downs are 1 kΩ (was 10 kΩ). The RZ/V2N internal pull-ups read an open strap as 1; carrier designs must not rely on them (pin table, Boot Settings, Boot Modes, Reference Schematic, minimum reference circuit and boot flow figures). • Wireless: the on-module MHF 4L receptacle is fitted but not fed; AR1 is the only RF feed in the standard build, and feeding the receptacle is an assembly option. • Backlight: BL_PWM on the BL_LED_A pad (B55) is an assembly option, not fitted in the standard build. • PCIe: described the two on-module PCIe multiplexers (port A, the common port, to the RZ/V2N; port C to the PCIE0 pads; port B to the DX-M1 position, not fitted on E1M-X V2N; SEL = 1 selects the PCIE0 pads, PD = 1 powers down) and added the PCIe connection figure. • Camera LDOs: noted that the TLV77201 input is the 3.3 V camera rail, so +V_CAMx stays below 3.3 V by the LDO dropout. • Pin Diagram: the pin-out is redrawn in the top view, landscape (65 mm across, 45 mm down), in the frame of the alplab.ai pinout viewer: pad letters A–AR are the rows, top to bottom, pad numbers 1–64 the columns, left to right; A1 is top left, A2 right of A1, B1 below A1. Split into four quarters so that every pad name prints at 6 pt or more. The pad numbers in the pin tables are unchanged. • Pin Diagram: the module is drawn as a plain rectangle with four square corners. A1 is marked by the triangular pin-1 fiducial. • Reflow profile figure redrawn in the house style; all values unchanged. • Security: the secure element is an Infineon OPTIGA Trust M (SLS32AIA010MLUSON10XTMA2) on BRD_I2C at 0x30, not a TPM (new Secure	October 2026

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Revision	Changes	Date
	Element section, block diagram, Ordering Matrix). General Description: the module is built on the open E1M standard (was “open-source” form factor). • Recommended PCB Land Pattern: the land-pattern drawing replaces the placeholder (top view, A1 top left, corner pads A1, A64, AR1, AR64 marked, pad geometry detail), and the parameter table is filled from E1M-STD §5.1.2 / §5.1.3: 1.00 mm pitch, Ø0.40 mm round NSMD pads, Ø0.50 mm solder-mask opening, 1:1 Ø0.40 mm stencil aperture. The “Pad size (GND ring)” row is removed: E1M-X has one pad size. • Recommended PCB Land Pattern: new Courtyard row (2.0 mm clearance around the module outline everywhere, 69.0 × 49.0 mm) in the parameter table; the courtyard is drawn dashed and dimensioned on the land pattern, and the central cavity is labelled as the carrier cut-out (mounting option b). • Pin-1 fiducial: drawn in copper, the colour of the pads (was black), as a right triangle with its right angle towards the A1 corner, inside the module outline and clear of it: to scale in the land-pattern drawing (0.25 mm inset, 0.52 mm legs, E1M-STD §5.1.2); in the pad map in the outer corner of the A1 cell. The separate A1 label in the pad-map centre is removed. • Keep-Out Zones: the “clear of components taller than TBD mm” rule and the placeholder figure are replaced by the mounting rule: the module carries bottom-side components in its central cavity and is not placed directly on a carrier; it is mounted on a spacer PCB, or over a through cut-out in the carrier the size of the cavity (57.45 mm across × 39.45 mm down, R1.00, 3.775 / 2.775 mm from the left / top outline edges). New mounting figure: cavity dimensioned on the module outline (top view, to scale) and section A–A on a spacer PCB and over a carrier cut-out. The spacer is soldered on both faces, and under both options the carrier has no components inside the cavity outline. Spacer thickness and bottom-side component height remain TBD (E1M-STD §5.2). • Packaging: removed the Tape & Reel section (placeholder drawing and specification table) and the EIA-481 tape-and-reel reference; tape and reel is not offered. Tray packaging is unchanged. • Ordering Matrix: the CPU part number R9A09G056N44GBG#AC0 prints on one line (it ran into the LPDDR4X column), and the CPU, AP-core, RT-core, AI and temperature values span the rows of all three MPNs (the E1M-V2N102 / E1M-V2N103 cells were empty). • Renesas RZ/V2N MPU: the Renesas RZ/V2N block diagram (source: Renesas Electronics) replaces the placeholder figure; a note states that blocks marked (option) depend on the RZ/V2N part number.	
0.10	• Block diagram labels as in the pin tables and the text: Ethernet pads ETH0 / ETH1 (was Ethernet 0 / Ethernet 1); PCIe pads PCIE0 (x2) (was PCIe x2); antenna pad ANT_2.4GHz (was Antenna); Ethernet PHY RTL8211FI-VD-CG (was RTL8211FI); secure element named OPTIGA Trust M at 0x30 on BRD_I2C (was Secure element, and the RZ/V2N pin I2C). • Block diagram: MODULE_EN and MODULE_STBY drawn as two pads (was MODULE_EN/STBY), with a note that MODULE_STBY also drives the RTC event input; CAM_VFB0..3 feedback pads added to the camera LDOs; the GD32 enable of the four camera LDOs drawn (GPIO to EN); white figure background for dark pages.	October 2026
0.11	• Release history: every entry formatted as a bullet list.	October 2026
0.12	• Layout: the Block Diagram heading is kept on the same page as its figure.	October 2026
0.13	• Contact: contact@alplab.ai is the only contact address. • Memory sizes given in GB (Ordering Information, MPN decoder, Ordering Matrix and the Memories figure): 101 = 4 GB LPDDR4X + 4 GB eMMC, 102 = 8 GB + 16 GB, 103 = 4 GB + 16 GB.	October 2026
0.14	• Reflow profile: figure redrawn from the measured E1M-AEN JTR1000 run (three thermocouples CH3, CH4, CH5 at their true time and temperature scale, with the 150 °C, 217 °C liquidus and 220 °C lines, the phase spans and a parameter box of the measured ranges); the text and caption state that it is the E1M-AEN measured profile, used as the recommended starting profile. • Reflow parameters (text, figure and table): measured time at or above 220 °C 56.5–60.0 s (was “about 60 s” above 217 °C), peak 240.9–244.3 °C (was 241–	October 2026

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Revision	Changes	Date
	244 °C), soak 150–217 °C 70.5–73.5 s (was 70–74 s), preheat 30–150 °C 116.5–122.0 s, cooling slope from 220 °C −1.53 to −1.66 °C/s (was about −1.6 °C/s), over the three thermocouples. • Reflow parameters table: recommended window from the profiler report beside the measured values: preheat 30–150 °C 60–160 s (new), soak 150–217 °C 60–120 s (unchanged), at or above 220 °C 45–90 s (was "time above liquidus (≥217 °C)" 45–90 s), cooling from 220 °C −4 to −0.5 °C/s (was average ramp-down T_P to T_L min −1.6 °C/s), peak 230–250 °C (was 241–244 °C); the ramp-up (max 3 °C/s) and time 25 °C to peak (max 8 min) rows removed (not in the measurement report).	
0.15	• Reflow profile figure: one measured curve (was three traces), with its phase spans and values (preheat 30–150 °C 116.5 s, soak 150–217 °C 71.5 s, at or above 220 °C 60.0 s, cooling from 220 °C −1.53 °C/s, peak 242.9 °C) and no legend; caption "Recommended starting profile: measured reflow profile of the E1M-AEN". • Reflow parameters table: the measured column is headed "Measured" (the ranges are unchanged).	October 2026
0.16	• Table of Contents: each entry links to its section; the front-matter lists are set tighter. • Page 1: the Applications section is back on the first page (smaller module photos); the Features and Applications headings are unnumbered. • Reflow figure: measured E1M-AEN profile, smoothed, without its zone-boundary kink (was the measured trace with that kink); caption "Recommended starting profile: measured E1M-AEN profile, smoothed". • Reflow parameters: the ramp-down slope (−1.53 to −1.66 °C/s) is the slope at or above 220 °C, from the peak down to 220 °C (was labelled "cooling from 220 °C").	October 2026
0.17	• Ordering Information: the sibling-line accelerator is named DeepX DX-M1 (was DeepX M1).	October 2026
0.18	• Hardware revision R3 (netlist export 15). Pin tables: AD3 is RTC_WAKE_N (open drain), AI3 is PMIC_GPIO5_10V (PMIC GPIO5, joined to BOOT3 through an on-module 0 Ω link) and AO3 / AP3 are GP_I2C.SCL / GP_I2C.SDA (3.3 V open drain, 4.7 kΩ pull-ups to +3V3_AON on the module); all four removed from the Not-connected Pins table (were NC). • New hardware-damage warning: 10 V on AI3 only with the on-module 0 Ω link to BOOT3 removed, else the 10 V reaches the RZ/V2N BOOTSELCPU input and destroys the RZ/V2N. • BOOT3 (Y1): the pad it shares through the 0 Ω link to the PMIC GPIO5 is AI3 (was "pad AO3"); pin table, Boot Modes and Reference Schematic. • Reserved Pins: AE62, AL62–AR62 are listed as not connected on the module. • Not-connected Pins: D63 carries a to-be-confirmed note (tied to GND in the current design data). • MODULE_EN (AA1) and MODULE_STBY (AB1): PMX100UNZ clamps, 1 MΩ pull-ups to +1V8_AON, carrier drive by open drain, switch or 1.8 V to 5 V push-pull (was a pull-up to VDD / 100 kΩ to VDD_5V_IN), with the MODULE_EN / MODULE_STBY timing. • PORn (Z1): open drain at 1.8 V, driven by the PMIC reset output and the power controller, 10 kΩ pull-up to VDD1G_1P8, no carrier pull-up. • Power Architecture: always-on domain with the always-on 3.3 V and 1.8 V regulators (+3V3_AON, +1V8_AON), the RTC with its +S_CAP backup input, and the programmable power controller (image v2n_ctl_v1): it filters MODULE_EN / MODULE_STBY, holds the power latch, and is the only driver of the PMIC enable and, with the PMIC, of PORn. • Reset, Module Enable & Power Control (was Reset & Module Enable): signals table with the MODULE_EN, MODULE_STBY, PORn and RTC_WAKE_N timing and the carrier leakage limit; Power Controller section with the power-on / power-off behaviour and timing (design values), the self-off through power-controller register 0x7A (OFF_ARM, then OFF), the boot-time write 0x7A =	November 2026

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Revision	Changes	Date
	0x00, and the warning never to set the lock bit, issue the soft reset, or write the NVM or register 0xC7. • Power-Up & Reset Sequence: steps follow the power controller; power-down by MODULE_EN low or self-off, with the rule to hold MODULE_EN low at least 150 ms before removing 5 V (was "no controlled power-down sequence"). • PCIe: the reference clock comes from the on-module clock generator; the RZ/V2N uses DIFF2, the PCIE0_CLK pads carry DIFF1, and the carrier must not add a second reference-clock source (was "a clock buffer drives the PCIE0_CLK output"). • New On-module I^2C Buses section: GP_I2C (power controller 0x08, RTC 0x52) and BRD_I2C (clock generator 0x69, OPTIGA Trust M 0x30, TMP112 0x40, GD32 0x70), the level-shifter bridge between them, and the warning against carrier pull-ups on GP_I2C. • New RTC Backup section: RV-3028-C7 on GP_I2C from +3V3_AON; +S_CAP (AQ25) goes directly to the RTC backup input, with no backup capacitor on the module; +S_CAP pin-table entry updated; with a non-rechargeable backup cell, firmware keeps the RTC trickle charger disabled. • New Clock Tree section: clock generator outputs REF, SE1 (also WL_32K to the Wi-Fi module), SE2, SE3, DIFF1, DIFF2, and the 22.5792 MHz audio crystal. • Digital Pins: the GD32-served pads have no series resistors on the module. • Power & Control Pins: note that AD3, AI3, AO3 and AP3 are NC in the E1M-X standard but carry module signals on E1M-X V2N. • Part numbers given as full order codes: always-on LDOs TPS7A0233PYCHR and TPS7A0218PYCHR, clock buffers SN74AUP1G34YFPR, clock generator 5L35023B-000NLGI. • Figures: pin-out map (AD3, AI3, AO3 and AP3 named), block diagram, power architecture, power-up sequence and minimum reference circuit redrawn for the always-on domain, GP_I2C, RTC_WAKE_N and the new MODULE_EN / MODULE_STBY front end; in the block diagram and the power architecture the RTC and the power controller are one block, "Power controller + RTC". • Minimum reference circuit: boot DIP switch redrawn, S1 / S2 from VIO_OUT to BOOT0 / BOOT1 with the 1 kΩ pull-downs. • PCIe: the PCIE0_CLK pads are driven from DIFF1 through the on-module reference-clock buffer, which is fitted on E1M-X V2N. • On-module parts named by function; component designators removed, also in the Release History rows.	
0.19	• Clock Tree table: the semicolons after the 22 Ω and 33 Ω resistor values are printed again in the SE1 and SE2 rows.	November 2026

Table 33 Revision History

18 Legal Notices

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- Web: alplab.ai
- Email: contact@alplab.ai
- Repository: github.com/alplabai

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