ALP LAB

E1M-X V2N HW Design Guide

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Release History

Revision	Changes	Date
0.1	• Initial draft.	May 2026
0.2	• Interface ESD/EMI protection moved to the carrier board (Ethernet, MIPI CSI, MIPI DSI); on-module protection retained only on the SD-card interface.	June 2026
0.3	• Added `E1M-V2N103` (32 Gbit LPDDR4X + 128 Gbit eMMC 5.1) to the supported variants and the pre-power check. • Software Support: replaced the non-existent `alp_e1m_v2n_m33_io` / `alp_e1m_v2n_m33_rt` / `alp_e1m_v2n_a55` board targets with what Alp SDK™ v0.17.0 ships (per-SKU Yocto `MACHINE` on the A55, `alp_e1m_v2n101_m33_sm/r9a09g056n48gbg/cm33` on the Cortex-M33); the GD32 supervisor is Alp Lab-programmed bridge firmware, not a customer build target. • Basic Validation: removed the retired `west alp-list-peripherals` command.	October 2026

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Revision	Changes	Date
0.4	• Figures: replaced the nine placeholder figures with drawings from the module netlist and the E1M-X development board netlist: module block diagram, 5 V buck converter, power-OR and eFuse, carrier reference block diagram, Ethernet to magnetics, RF feed, MIPI CSI-2 and MIPI DSI routing (with the backlight), CAN transceiver, termination and connector. • CAN-Bus: added that the E1M-X development board, as assembled, ties J24 / J25 straight to B21 / B22 / B24 / B25 (R235– R238 fitted, R227– R234 not fitted); with a V2N module, swap them before connecting a bus. • Ethernet: the `ETH0_LED0` / `ETH0_LED1` strap levels and the LED polarity check. • PCIe: the on-module PCIe multiplexer is held in power-down at reset; software enables it and selects the `PCIE0` pads through `P80` / `P95`. • CAN-Bus: the on-module CAN transceivers (TI `TCAN1044AVDRBRQ1`) are not fitted on the V2N module; `CAN0H/CAN0_TX` (B21), `CAN0L/CAN0_RX` (B22), `CAN1H/CAN1_TX` (B24) and `CAN1L/CAN1_RX` (B25) carry the 1.8 V CAN-FD TX / RX logic signals, so the carrier must add the transceivers. Replaced the rule that the carrier shall not add a transceiver, and corrected the key characteristics, the carrier overview and the design checklist. • Ethernet PHY corrected to Realtek `RTL8211FI-VD-CG` (was `RTL8211FDI`). • Wi-Fi: `ANT_2.4GHz` (AR1) is the only antenna pad and the only feed of the Wi-Fi / BLE module (through on-module 0 Ω links); `ANT_5GHz` (AP1) and `ANT_6GHz` (AN1) are not connected on the module. The on-module I-PEX MHF 4L connector is fitted but not fed (its 0 Ω link is not fitted); the two 0.1 µF parts to GND on the RF path are not fitted. The RF feed figure shows this path. • Boot: carrier strap on `BOOT3` (Y1), a 1 kΩ pull-up to `VIO_OUT` for a Cortex-A55 boot (the PMIC GPIO5 on the same net is an input); `BOOT2` (X1) takes a 1 kΩ pull-up to `VIO_OUT` on the carrier, as the module has no `BOOT2` pull-up. The carrier reference block diagram and the design checklist show both straps. A closed `BOOT0` / `BOOT1` DIP switch ties the line to `VIO_OUT` (was: the SoC pulls it high). • Boot straps: every strap (`BOOT0`–`BOOT3`) takes a 1 kΩ carrier resistor, a pull-up to `VIO_OUT` for 1 or a pull-down to `GND` for 0 (`BOOT3`: 1 kΩ pull-down for a Cortex-M33 boot). The `BOOT0` / `BOOT1` DIP-switch pull-downs are 1 kΩ (was 10 kΩ). The RZ/V2N internal pull-ups read an open strap as 1; carrier designs must not rely on them (Boot, carrier reference block diagram, design checklist). • MIPI DSI: one 4-lane interface (`DSI0`); the `DSI1` pads are not connected. Backlight feedback voltage corrected to 200 mV (was 95 mV), with the `BL_LED_A` boost-voltage note. • USB: `USB_CC1` / `USB_CC2` are not connected on the module. PCIe: `PCIE0_TX0` / `PCIE0_TX1` are AC-coupled on the module. SPI NOR flash corrected to 512 Mbit (was 128 Mbit). Power management names the on-module PMIC and regulator. • Mechanical Information and Design Checklist: a module is never placed directly on a carrier; it is mounted on a spacer PCB (soldered on both faces: module to spacer, spacer to carrier) or over a carrier cut-out the size of the central cavity (57.45 mm across × 39.45 mm down, R1.00, 3.775 / 2.775 mm from the left / top outline edges), as its bottom-side components sit in the cavity; under both options the carrier has no components inside the cavity outline. • Dimensions: the height-class statement (standard height, E1M Spec §5.2.1) is replaced by the mounting rule (a module is mounted on a spacer PCB or over a carrier cut-out the size of the cavity) and the 2.0 mm courtyard (69.0 × 49.0 mm).	October 2026
0.5	• Document status: the title page now reads Preliminary, matching the running header (it read Draft).	October 2026
0.6	• Release history: every entry formatted as a bullet list.	October 2026
0.7	• Memory sizes given in GB (supported-variants table, memory list, pre-power check): `101` = 4 GB LPDDR4X + 4 GB eMMC, `102` = 8 GB + 16 GB, `103` = 4 GB + 16 GB.	October 2026
0.8	• Table of Contents: each entry links to its section; the front-matter lists are set tighter.	October 2026
0.9	• Product name on page 1 links to the product page on alplab.ai.	November 2026

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Revision	Changes	Date
0.10	• Hardware revision R3 (module netlist export 15). • PCIe: the reference clock is generated on the module. PCIE0_CLK_P/N (A47 / B47) carry output DIFF1 of the on-module clock generator through the on-module reference-clock buffer, and the RZ/V2N uses DIFF2 of the same PLL; the carrier must not add a second reference-clock source (was “carrier-board reference clock optional”). • New section Power Control, Reset and Wake: carrier rules for MODULE_EN (AA1), MODULE_STBY (AB1), PORn (Z1), RTC_WAKE_N (AD3), GP_I2C.SCL / GP_I2C.SDA (AO3 / AP3, no carrier pull-ups), PMIC_GPIO5_10V (AI3) and +S_CAP (AQ25); AK3–AM3 are not connected on E1M-X V2N; AD3, AI3, AO3 and AP3 are NC in the E1M-X standard and carry no carrier nets. • New hardware-damage warning: 10 V on AI3 only with the on-module 0 Ω link to BOOT3 removed. New warnings: no carrier pull-ups on GP_I2C; never set the power controller’s lock bit, issue its soft reset, or write its NVM or register 0xC7; hold MODULE_EN low at least 150 ms before removing 5 V. • Power: the on-module PMIC sequences the rails and is enabled by the programmable power controller (was: the GD32 supervisor sequences the rails); the PMIC is named by function. MODULE_EN note corrected (1 MΩ pull-up to +1V8_AON through an on-module clamp; was “pulled up to 5 V”). • Boot: BOOT3 (Y1) is also pad AI3 (PMIC_GPIO5_10V) through the on-module 0 Ω link; leave AI3 open. • Digital Communication: GP_I2C is the exception to the carrier pull-up rule. • Design Checklist: rows for the MODULE_EN / MODULE_STBY leakage limit and the 150 ms MODULE_EN rule, AI3, GP_I2C, RTC_WAKE_N and the module-signal pads AD3 / AI3 / AO3 / AP3. • PCB flatness: no longer attributed to the regulator (was “Renesas DA9292 PMIC requirements”). • Figures: module block diagram shows the power controller + RTC, RTC_WAKE_N and GP_I2C (was “GD32 supervisor sequencing”); carrier reference block diagram lists MODULE_STBY and RTC_WAKE_N; RF feed figure names the on-module parts by function. • On-module parts named by function; component designators removed, also in the Release History rows.	November 2026

Table 1 Release History

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1 Introduction

1.1 Purpose of This Document

This guide provides practical guidance for developers and system integrators using the **E1M-X V2N System-on-Module (SoM)**.

It covers:

- Hardware integration and carrier-board design
- Power architecture and system bring-up
- Interface usage and pin functional intent
- Common pitfalls during first implementation

This guide complements:

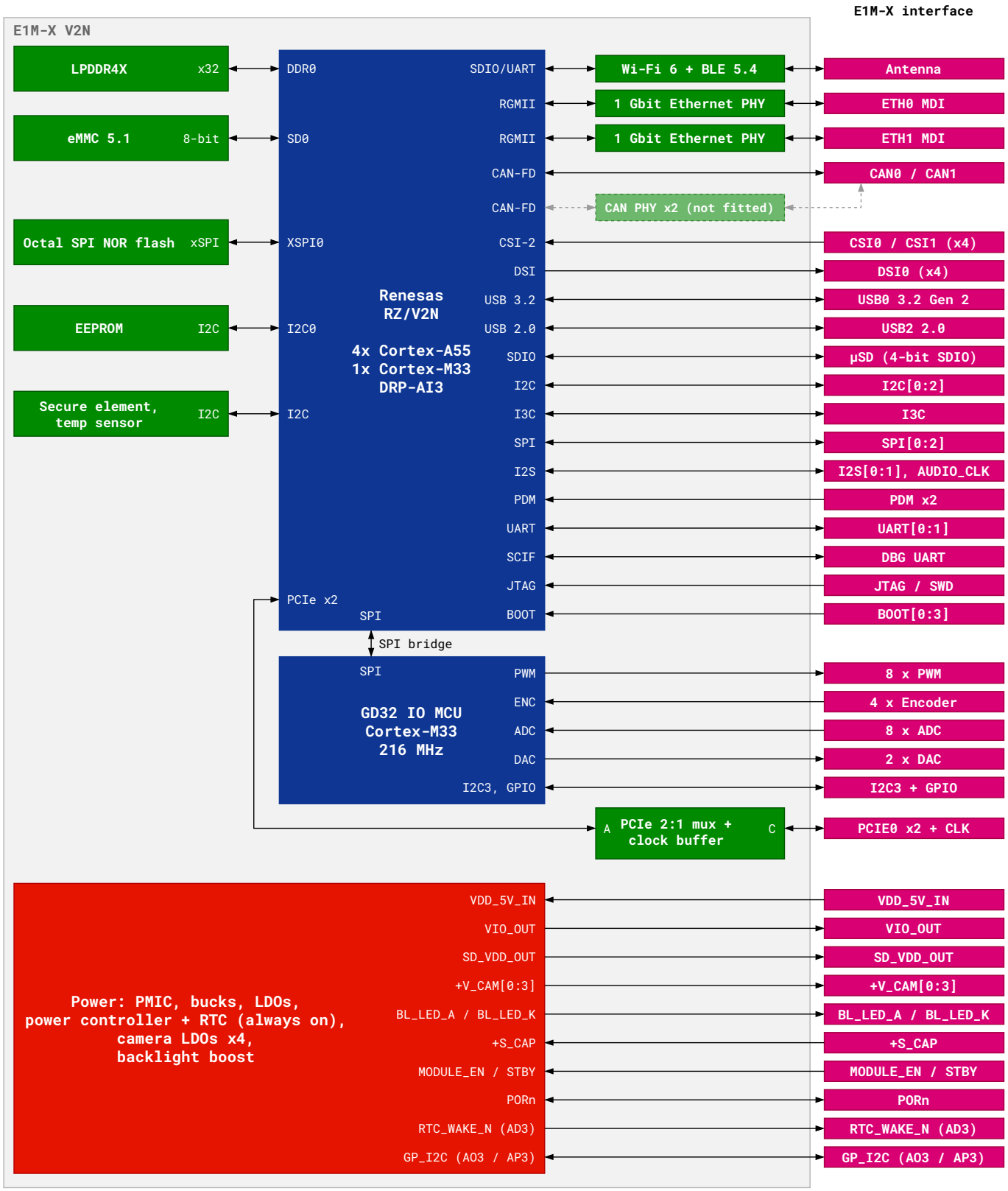
- The **E1M-X V2N Datasheet** (DS-V2N-001)
- The **Renesas RZ/V2N** hardware reference manual and PCB design guidelines
- The **E1M Specification** (E1M-STD-1.0) for form-factor and pinout requirements
- The **Alp SDK™** documentation

1.2 Product Overview

The **E1M-X V2N** is a compact **45 × 65 mm Edge-AI System-on-Module** based on the **Renesas RZ/V2N** vision-AI MPU. It targets industrial vision, robotics, automotive driver-monitoring, and high-throughput AI inference applications.

The module follows the **E1M-X™ open-standard pin layout**, enabling drop-in compatibility with other E1M-X-conformant SoMs without redesigning the carrier board.

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Dashed: not fitted (on-module CAN PHYs); 0 Ω links put the 1.8 V CAN-FD TX / RX logic signals on the CAN pads instead. Memory sizes per SKU. Arrowheads mark the receiving end (both ends: bidirectional). The power controller is the only driver of the PMIC enable; it and the RTC sit on the always-on GP_I2C. PCIe x2 reaches the PCIE0 pads through the on-module PCIe mux. The mux is held in power-down (PD pulled high) and SEL is pulled low on the module: software drives P80 (PD) and P95 (SEL); SEL high selects the PCIE0 pads (A-C). PCIE0_CLK: clock generator DIFF1 through the reference-clock buffer.

Figure 1 E1M-X V2N Block Diagram

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Key characteristics:

- Unified E1M-X pinout, hardware-compatible with future RZ/V2N successors
- Quad Cortex-A55 @ 1.8 GHz + Cortex-M33 @ 200 MHz application + real-time cluster
- DRP-AI3 AI accelerator (4 TOPS)
- Arm Mali-C55 ISP + Mali-G31 GPU
- On-module 1 Gbit Ethernet PHYs (× 2) and Wi-Fi 6 + BLE 5.4 combo; 2 × CAN-FD on the pads (logic level, the carrier adds the transceivers)
- On-module power management (main PMIC, Renesas DA9292 regulator, programmable power controller and always-on RTC) plus GD32 supervisor MCU
- Single external **5 V supply**
- Long-term lifecycle orientation

2 Supported SoC Variants

SKU	Renesas Part	LPDDR4X	eMMC
E1M-V2N101	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 4 GB
E1M-V2N102	R9A09G056N44GBG#AC0	8 GB	eMMC 5.1, 16 GB
E1M-V2N103	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 16 GB

Table 2 V2N-family SKUs

All three SKUs share identical pinouts and silicon outside of the memory tier; carrier boards designed against one SKU work unmodified with the others.

3 Mechanical Information

3.1 Dimensions

- **Size:** 45 × 65 mm
- **Form factor:** Connectorless, solder-down LGA SoM
- **Courtyard:** 2.0 mm clearance around the module outline, 69.0 × 49.0 mm
- **Mounting:** never directly on the carrier. The module carries components on its bottom side, in the central cavity inside the pad band; mount it on a spacer PCB (soldered on both faces: module LGA to spacer, spacer to carrier), or over a through cut-out in the carrier the size of the cavity: 57.45 mm across × 39.45 mm down, R1.00 corners, 3.775 mm from the left and 2.775 mm from the top outline edge. With either option the carrier has no components inside the cavity outline. Spacer thickness and bottom-side component height: TBD.

For the full mechanical drawing including land pattern, keep-out zones and the mounting figure, see the **E1M-X V2N Datasheet** (DS-V2N-001), Mechanical & Footprint Dimensions.

3.2 Handling and Assembly

- ESD-sensitive device. Use grounded handling equipment.
- Avoid mechanical stress after soldering.
- Follow IPC J-STD-020 reflow profile (see DS-V2N-001 §11.2).
- Maintain PCB flatness under the module; warpage > TBD µm may compromise BGA solder joints under the SoC.

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4 Power Architecture

4.1 Power Input

- **Input voltage:** 5 V DC, single rail on VDD_5V_IN
- All regulators, the PMIC, and sequencing are on-module
- No additional power rails must be supplied by the carrier

Warning: Do **not** attempt to power individual rails (VIO_OUT, SD_VDD_OUT, etc.) externally. These pads are **outputs** from the module; sourcing them externally will fight the on-module regulator and may damage the PMIC.

4.2 Power Design Guidelines

- Place bulk capacitance (≥ 10 µF) near the 5 V input
- Use a solid ground plane covering the entire SoM footprint
- Keep high-current paths (Ethernet PHY supplies, M.2 SSD slot supplies on the carrier) short and wide
- Do not power external loads from VIO_OUT unless validated; the rail is sized for level-shifters and small pull-ups only
- Nominal input voltage: 5.0 V; recommended tolerance: ±5%
- Connect **every** GND pad on the SoM to a low-impedance plane (105 pads on E1M-X)
- No external sequencing required: the on-module PMIC sequences the rails, and the on-module programmable power controller is the only driver of the PMIC enable (Section 4.3)

4.3 Power Control, Reset and Wake

An always-on domain runs from VDD_5V_IN whenever 5 V is present: the always-on rails +3V3_AON and +1V8_AON, the on-module RTC and the programmable power controller. The power controller filters MODULE_EN and MODULE_STBY, holds the module power latch and is the only driver of the PMIC enable; with the PMIC reset output it drives PORn. The RTC interrupt wakes the module through the power controller and drives RTC_WAKE_N. The RTC and the power controller share the always-on GP_I2C bus. Timing below is the design value of the power-controller image (bench validation pending); see the **E1M-X V2N Datasheet** (DS-V2N-001), Reset, Module Enable & Power Control.

Pad	Carrier rule
MODULE_EN (AA1)	Module enable, through an on-module PMX100UNZ clamp (gate +1V8_AON) with a 1 MΩ pull-up to +1V8_AON. Drive with an open-drain output (no pull-up), a switch to GND, or push-pull logic from 1.8 V to 5 V. Low ≤ 0.5 ms: ignored. Low ≥ 4 ms: the RZ/V2N is reset, the rails stay up. Low ≥ 55 ms: the module powers off. Released, the pad sits at about 1.2–1.5 V (estimate). Leave floating if not used.
MODULE_STBY (AB1)	Standby and wake request, pulse-only. Same front end and drive options as MODULE_EN. A low pulse ≥ 2 ms is a request to firmware with the module on, and wakes the module from self-off. Held low, it blocks the firmware self-off. Leave floating if not used.
PORn (Z1)	RZ/V2N reset, open drain at 1.8 V, 10 kΩ pull-up to VDD1G_1P8 on the module. The carrier may pull it low (push-button or open-drain output) to reset the RZ/V2N with the rails up. No carrier pull-up.
RTC_WAKE_N (AD3)	RTC wake output, active low, open drain, valid in every state while 5 V is present. Carrier pull-up to its always-on rail: ≤ 5.5 V, ≥ 10 kΩ. Leave floating if not used.
GP_I2C.SCL / GP_I2C.SDA (AO3 / AP3)	Always-on 3.3 V I^2C, open drain: the power controller (0x08, also its programming port) and the RTC (0x52). 4.7 kΩ pull-ups to +3V3_AON on the module. No carrier pull-ups; keep both pads high-impedance whenever module 5 V is absent. Bring the pads to a test point or header for provisioning; leave them floating otherwise.

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Pad	Carrier rule
PMIC_GPIO5_10V (AI3)	PMIC in-circuit programming path (about 10 V). On the module it is the same node as B00T3 (Y1) through an on-module 0 Ω link, so a carrier that drives or straps AI3 also drives B00T3. Leave AI3 floating; set the boot CPU on B00T3 only.
+S_CAP (AQ25)	RTC backup input. The module has no backup capacitor fitted: to keep the time while 5 V is absent, fit a super-capacitor or backup cell on the carrier.
AK3, AL3, AM3	Not connected on E1M-X V2N. Leave floating.

Table 3 Carrier rules for the power, reset and wake pads

Note: AD3, AI3, AO3 and AP3 are NC in the E1M-X standard; on E1M-X V2N they carry module signals. A carrier for E1M-X V2N must not route its own nets through these pads.

Warning: Hardware-damage hazard. PMIC_GPIO5_10V (AI3) takes about 10 V for PMIC in-circuit programming. Apply 10 V to AI3 only with the on-module 0 Ω link to B00T3 removed. With that link fitted, the 10 V reaches the RZ/V2N B00TSELCPU input and destroys the RZ/V2N.

Warning: Fit no carrier pull-ups on GP_I2C (AO3 / AP3), and keep both pads high-impedance whenever module 5 V is absent.

Warning: Never set the power controller's lock bit, never issue its soft reset, and never write its NVM or register 0xC7 from the application. All outputs of the power controller then go high-impedance and the module powers off uncontrolled.

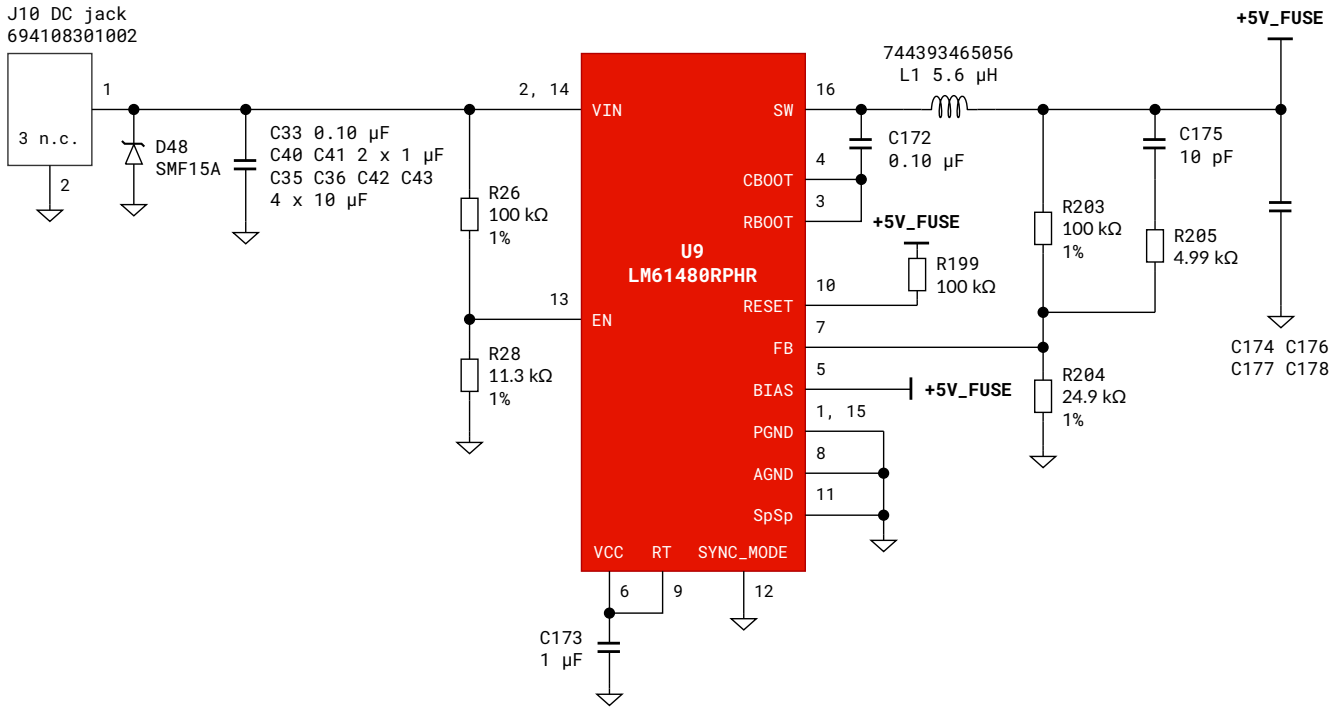
The power controller is programmed over GP_I2C at provisioning with MODULE_EN held low; a new image takes effect after the next 5 V cycle. Keep the carrier leakage on MODULE_EN and MODULE_STBY at ≤ 0.1 µA on each pad, ESD parts included.

Warning: Hold MODULE_EN low at least 150 ms before removing 5 V. Removing 5 V with the module on is for recovery only.

4.4 Carrier-Board 5 V Generation

A buck converter is the recommended way to generate the 5 V rail from the carrier-board input voltage. Choose a converter rated for transients up to **5 A** to cover worst-case AI + dual-Ethernet + M.2 SSD activity simultaneously.

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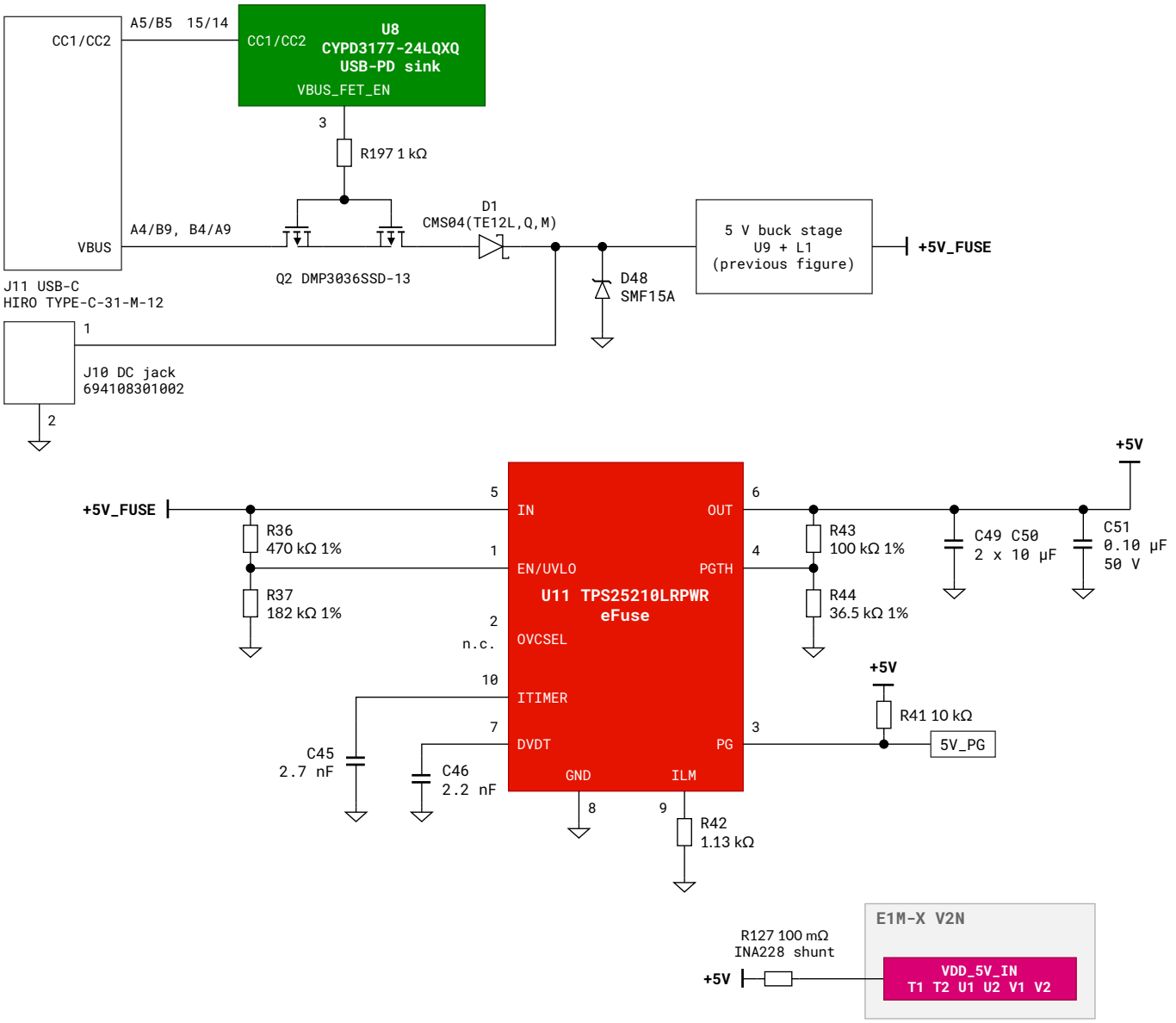


E1M-X development board. Capacitors drawn as one symbol are in parallel. Output: C174 0.10 µF, C176 / C177 10 µF, C178 100 µF 10 V polymer (875105242010). +5V_FUSE feeds the U11 eFuse (next figure). The U9 VIN node (J10 pin 1) is also fed from the USB-PD sink through D1 (next figure). RESET is pulled up and not used further.

Figure 2 5 V buck-converter reference circuit (E1M-X development board)

Power-OR'ing using diodes or eFuses is supported. When multiplexed (e.g. between barrel jack and USB-PD on a carrier), use a unidirectional eFuse to avoid back-feeding the inactive source.

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E1M-X development board. J10 feeds the U9 VIN node directly; the USB-C path enters through D1, so J10 cannot back-feed the USB-C VBUS. U8 switches Q2 (back-to-back P-MOSFETs) through R197; Q2 gate network R16 10 kΩ, R21 49.9 kΩ, D2 SZ1SMA5925BT3G, C39 / C48 1 µF not drawn. 5V_PG enables the carrier rails.

Figure 3 eFuse / power-OR reference circuit (E1M-X development board)

5 Memory and Boot Architecture

5.1 Internal Memory (SoC-Dependent)

- **On-chip SRAM:** 1.5 MB (RZ/V2N)
- **LPDDR4X DRAM:** 32-bit, 3.2 GT/s, up to 8 GB (per SKU)

5.2 On-Module Memory

- **eMMC 5.1** up to 16 GB (per SKU)
- **Octal SPI NOR flash:** 512 Mbit, boot-supported
- **I²C EEPROM:** optional, accessible via `I2C0` for production-time configuration storage

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Note: Contact Alp Lab for custom memory configurations (alternate eMMC sizes, NAND replacing NOR, expanded EEPROM).

5.3 Boot

The RZ/V2N samples four boot-strap pins at PORn release:

- BOOT0, BOOT1 select the boot device (eSD / eMMC / QSPI NOR / SCIF download).
- BOOT2 (X1) is fixed at 1 on the V2N family: pull it up to VIO_OUT with 1 kΩ on the carrier. The module has no BOOT2 pull-up.
- BOOT3 (Y1) selects the boot CPU (high = CA55, low = CM33). For a Cortex-A55 boot, pull it up to VIO_OUT with 1 kΩ on the carrier; for a Cortex-M33 boot, pull it down to GND with 1 kΩ. On the module the same net also reaches GPIO5 of the PMIC through an on-module 0 Ω link, and so pad AI3 (PMIC_GPIO5_10V); the PMIC GPIO5 is an input (high impedance), so the carrier strap sets the level. Leave AI3 open (Section 4.3).

Strap every boot pin (BOOT0–BOOT3) on the carrier with a 1 kΩ resistor: a 1 kΩ pull-up to VIO_OUT for 1, a 1 kΩ pull-down to GND for 0. The RZ/V2N has internal pull-ups on its boot-strap pins, so a strap left open reads 1, but a carrier design must not rely on them.

See the **E1M-X V2N Datasheet** (DS-V2N-001) §4.1 for the full boot-mode truth table and DIP-switch interpretation on the reference EVK.

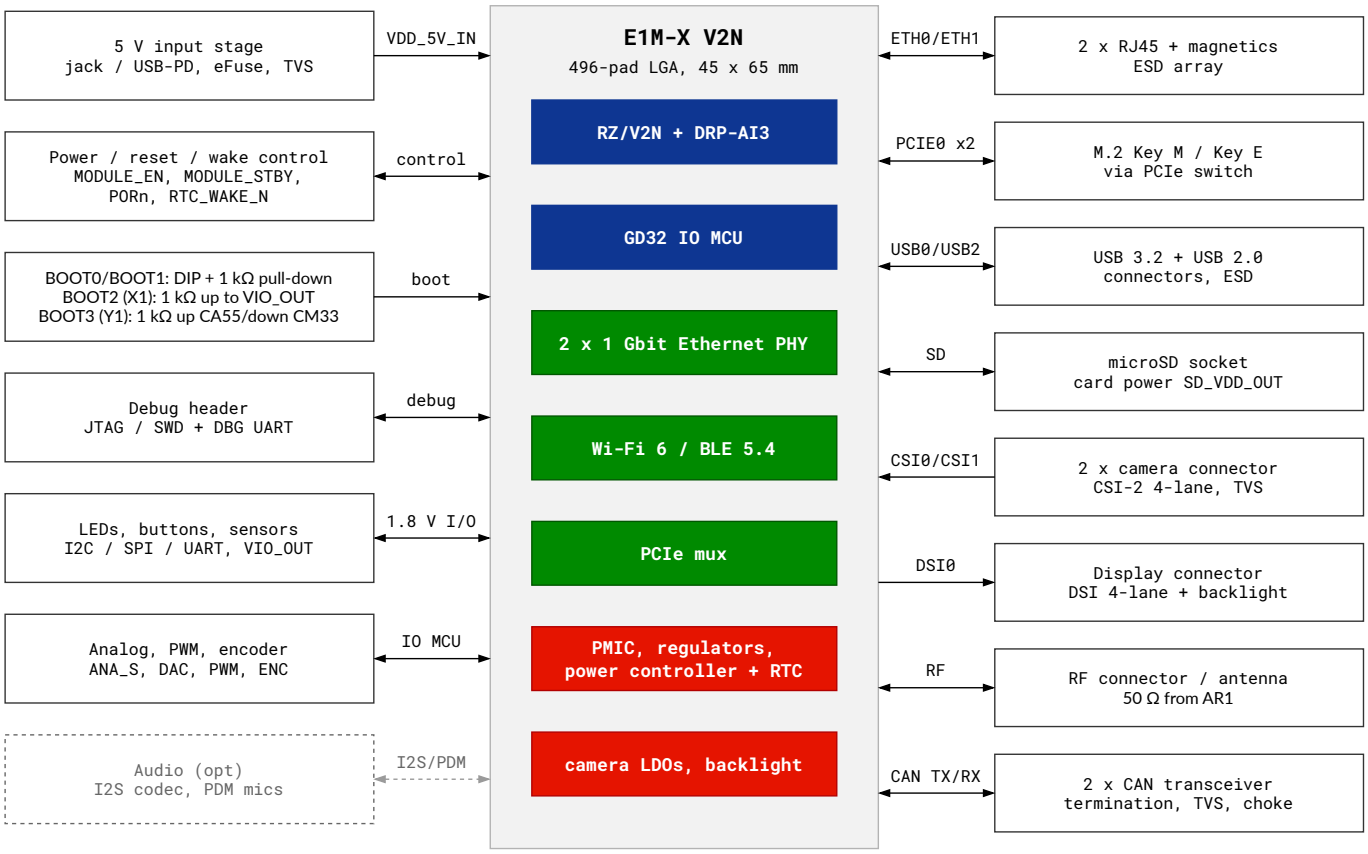
The carrier board **MUST** provide a way to drive BOOT0 and BOOT1. The simplest implementation is a 2-position DIP switch with a 1 kΩ pull-down to GND on each line; closing a switch ties its line to VIO_OUT (logic 1), an open switch leaves the 1 kΩ pull-down (logic 0). Production carriers may hard-strap the pins to the desired boot mode with 1 kΩ resistors (pull-up to VIO_OUT for 1, pull-down to GND for 0).

Note: MODULE_EN has a 1 MΩ pull-up to +1V8_AON on the module, behind an on-module clamp; drive it low to switch the module off, leave it floating if not used. PORn is open drain with a 10 kΩ pull-up to VDD1G_1P8 on the module; drive it low for ≥ TBD µs to reset the RZ/V2N. See Section 4.3.

6 Carrier-Board Reference Block Diagram

The carrier board has been designed for the **E1M-X** open standard to support all E1M-X variants. The V2N family routes the following subset of the E1M-X pinout; carriers that target only V2N may leave the other pads unused.

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Dashed: optional (opt). The carrier provides the protection on every external interface except SD (on-module).
Arrowheads mark the receiving end (both ends: bidirectional). The module has no CAN transceiver fitted:
the carrier adds it.

Figure 4 Carrier-board reference block diagram for V2N

6.1 System-Level Overview

The carrier board provides:

- 5 V power input and protection (barrel jack, USB-PD)
- External connectors and signal conditioning
- Magnetics + RJ45 for both Ethernet ports
- CAN transceivers, termination and connectors for both CAN ports
- M.2 Key M / Key E slots for PCIe + Wi-Fi expansion
- Display + camera FFC connectors
- User-interface peripherals (LEDs, push-buttons, DIP switches)

All complex power, RF, EMI, and processing functions are integrated **into the E1M-X V2N module**.

6.2 Design Philosophy

- Keep the carrier board simple and application-specific.
- Avoid duplicating functionality already on-module (PMIC, Ethernet PHYs, Wi-Fi).
- Maintain reuse across V2N and V2N-M1 SoMs; both families share the same pinout subset.
- Minimise RF, power, and EMI risk on the carrier board.

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7 Interfaces Overview

All interfaces are exposed through the standardised **E1M-X™ pinout**. The remainder of this section captures the carrier-board design rules per interface.

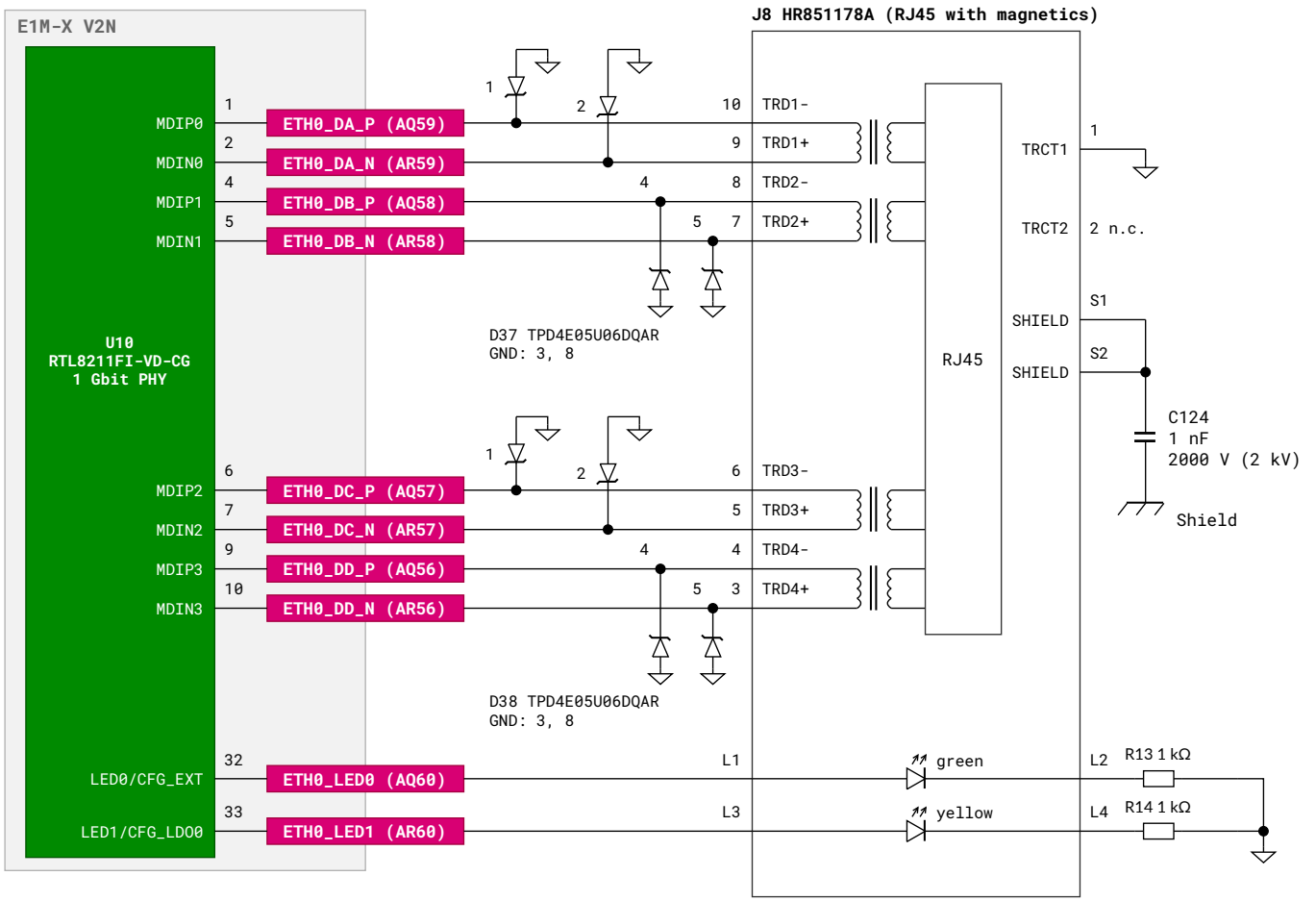
> **Note:** See the **E1M-X V2N Datasheet** (DS-V2N-001) and the **E1M Specification** (E1M-STD-1.0) for the canonical pad-list and pin-function mapping.

7.1 Ethernet Interfaces

- 2 × 1 Gbit Ethernet via on-module PHYs (Realtek `RTL8211FI-VD-CG`)
- External magnetics and RJ45 required on the carrier
- Auto-negotiation enabled by default
- `ETH0_LED0` / `ETH0_LED1` (and the ETH1 LED pins) are also PHY configuration straps: the module pulls `ETH0_LED0` up and `ETH0_LED1` down (4.7 kΩ each). Add no other pull-up or pull-down; the PHY sets each LED output's polarity from its strap level, so check the polarity in the `RTL8211FI-VD-CG` datasheet before you wire the LEDs
- EMI / ESD protection required on the carrier board

Route both Ethernet pairs as 100 Ω differential. Match the lengths within each pair to within ±2 ps; match across the four pairs of one port to within TBD ps. The module does not integrate Ethernet ESD/EMI protection — add a low-capacitance ESD/TVS array (and common-mode choke as needed) on the MDI lines between the magnetics and each connector.

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E1M-X development board, ETH0 (ETH1 is wired the same way to J20). MDI pairs: 100 Ω differential, matched within each pair (±2 ps). The board lands each pair P on TRDx- and N on TRDx+, as drawn. J8 integrates the magnetics (one transformer per pair; TRCT1 / TRCT2 are its centre-tap pins). U10 is the on-module PHY. ETH0_LED0 / ETH0_LED1 are also its configuration straps (LED0/CFG_EXT, LED1/CFG_LDO0): the module pulls LED0 up (4.7 kΩ) and LED1 down (4.7 kΩ); add no other pull-up or pull-down on the carrier. The PHY sets each LED output polarity from its strap level: check the RTL8211FI-VD-CG datasheet before copying the LED-to-GND wiring for LED0.

Figure 5 V2N Ethernet PHY-to-magnetics reference connection

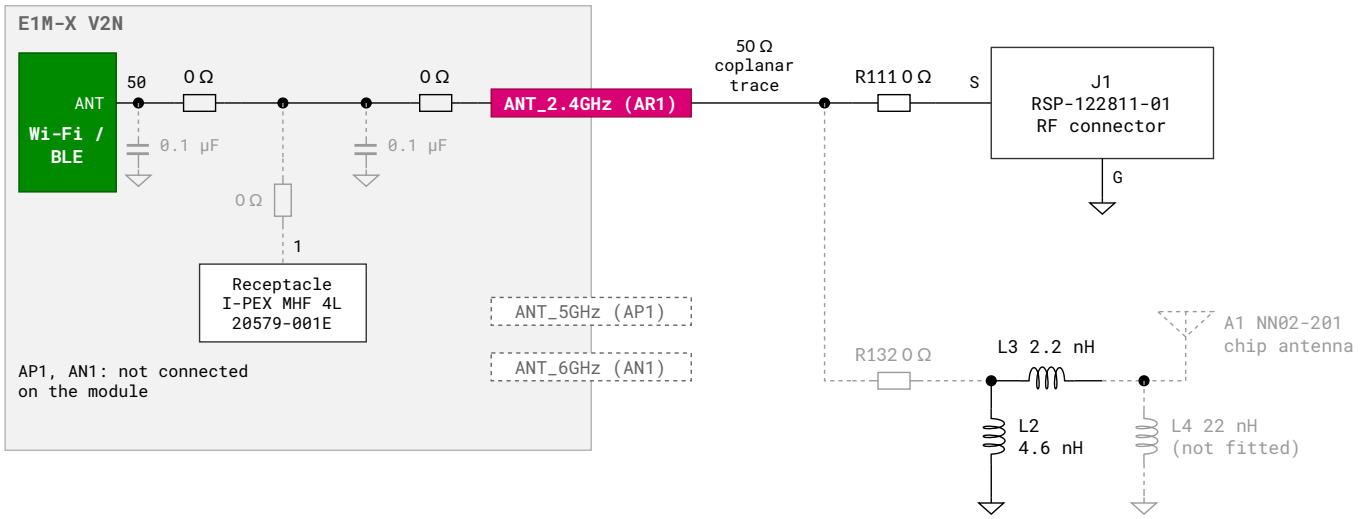
Warning: Carrier-board designers **SHALL NOT** add an external Ethernet PHY between the SoM and the magnetics. The on-module PHYs are mandatory per **E1M Spec** §6.5; adding a second PHY breaks conformance and may damage the on-module driver.

7.2 Wi-Fi and BLE

- Wi-Fi 6 (2.4 / 5 / 6 GHz, 802.11 a/b/g/n/ac/ax) + BLE 5.4 via on-module Murata LBEE5HY2FY (Infineon CYW55513)
- One antenna pad: ANT_2.4GHz (AR1), fed from the single antenna port of the Wi-Fi / BLE module. ANT_5GHz (AP1) and ANT_6GHz (AN1) are not connected on the module: leave them unconnected
- On the module the Wi-Fi / BLE antenna port reaches AR1 through two on-module 0 Ω links. The on-module I-PEX MHF 4L connector (20579-001E) is fitted but not fed: its 0 Ω link and the two 0.1 µF parts to GND on the RF path are assembly options and are not fitted. AR1 is the only RF feed
- 50 Ω impedance-controlled RF routing required on the carrier
- Keep digital noise away from RF paths; via stitching strongly recommended

Route each RF trace as 50 Ω controlled-impedance microstrip or coplanar waveguide. Maximum antenna gain to maintain regulatory compliance is TBD dBi per band.

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E1M-X development board: R111 and J1 fitted (RF connector). Dashed grey: not fitted (R132, L4, A1); L2 / L3 are fitted. Route the carrier trace as 50 Ω coplanar line with a GND via fence.
Module: ANT_2.4GHz (AR1) is the only antenna pad and the only feed of the on-module LBEE5HY2FY (pin 50 ANT), through two on-module 0 Ω links. Dashed grey on the module: assembly options, not fitted (the two 0.1 µF parts to GND, and the 0 Ω link that would feed the module receptacle). The receptacle is fitted, not fed.
Keep the trace short, away from noise sources, and keep the antenna keep-out free of copper (antenna vendor). Use only a certified antenna.

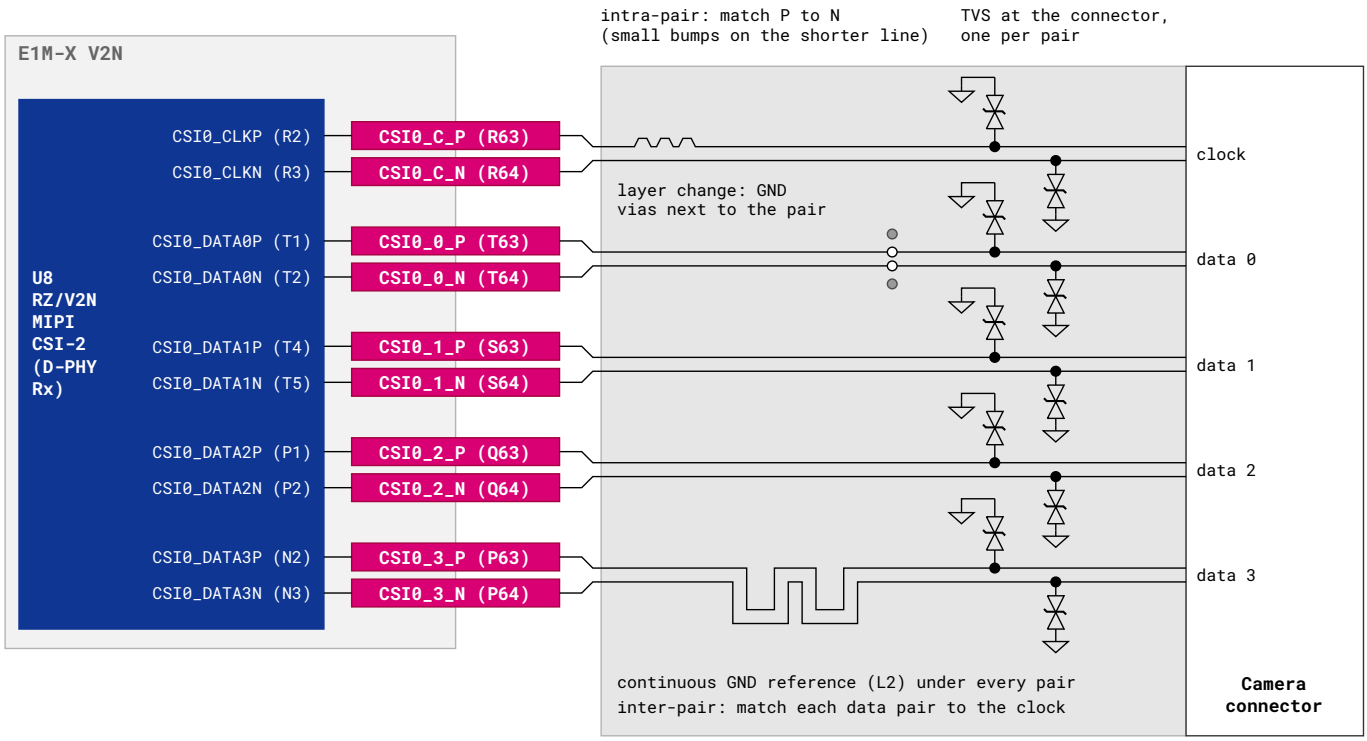
Figure 6 V2N RF antenna routing reference

7.3 MIPI CSI-2 Cameras

- 2 × 4-lane MIPI CSI-2 interfaces (CSI0, CSI1)
- Up to 4K @ 30 fps per interface, 4 virtual channels
- Controlled-impedance differential routing required
- Minimise vias and stubs

Route each CSI lane as 100 Ω differential, ±10%. Match lengths within each pair and across the four lanes + clock of one camera. The module does not integrate CSI ESD/EMI protection — protect the lanes with a low-capacitance TVS array on the carrier board.

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All CSI0 pairs: 100 Ω ±10 % differential. Keep pairs short; minimise vias and avoid stubs. Match within each pair first, then across the pairs (clock to the data lanes). CSI1 (X63/X64 clock, Z, Y, W, V data) is routed the same way. E1M-X development board TVS: Semtech RCLAMP3552T.TNT, one per pair (pins 1 / 2 on the lines, 3 to GND).

Figure 7 MIPI CSI-2 routing example

Per-camera LDOs (+V_CAM0…+V_CAM3) are available on-module. Place the divider feedback resistors close to the CAM_VFBx pins. The output voltage is set by:

$$V_{\mathrm{CAM}} = 0.6\ \mathrm{V} \times \left(1 + \frac{R_1}{R_2}\right)$$

7.4 MIPI DSI Displays

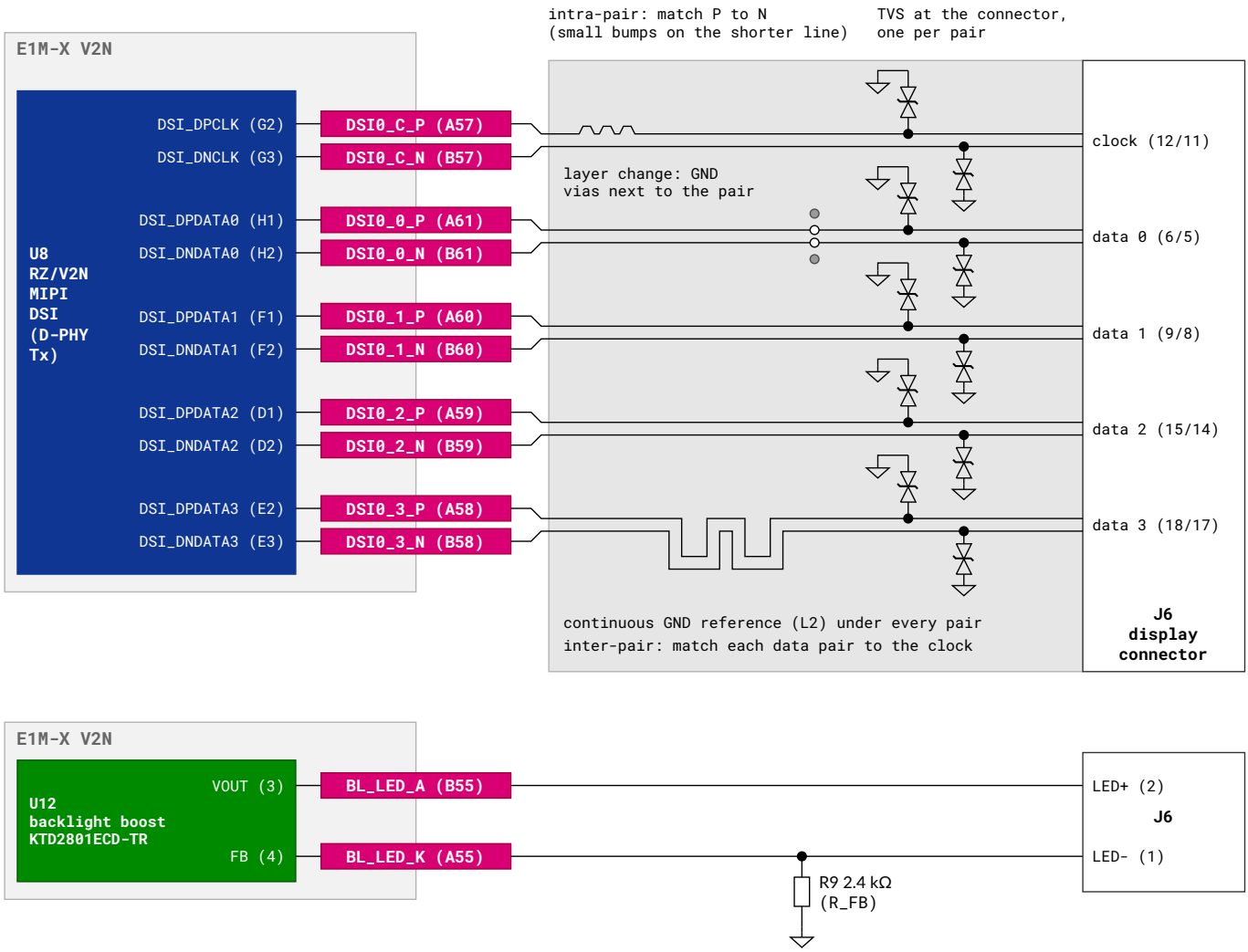
- 1 × 4-lane MIPI DSI interface (DSI0); the DSI1 pads are not connected on the module
- Up to 1920 × 1200 RGB888 @ 60 fps
- DSI signals require EMI / ESD protection (low-capacitance TVS array) on the carrier board
- On-module backlight driver supports up to 10 LEDs in series or 2P6S

Route each DSI lane as 100 Ω differential, ±10%. Connect the LED string anode to BL_LED_A (B55) and its cathode to BL_LED_K (A55); place the feedback resistor R_{FB} on the carrier between BL_LED_K and GND. The LED current of the on-module driver (KTD2801ECD-TR) is:

$$I_{\mathrm{LED}} = 200\frac{\mathrm{mV}}{R_{\mathrm{FB}}}$$

BL_LED_A carries the boost output (up to 36 V): never connect it to a logic input, and rate the carrier traces and connector for it.

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Backlight: the LED string anode on BL_LED_A, its cathode on BL_LED_K; R_FB from BL_LED_K to GND sets I_LED = 200 mV / R_FB. BL_LED_A carries the boost output (up to 36 V). E1M-X development board: J6 F34G-1A7Q1-E8C40 (pin numbers in brackets), R_FB = R9 2.4 kΩ; TVS Semtech RCLAMP3552T.TNT, one per pair.

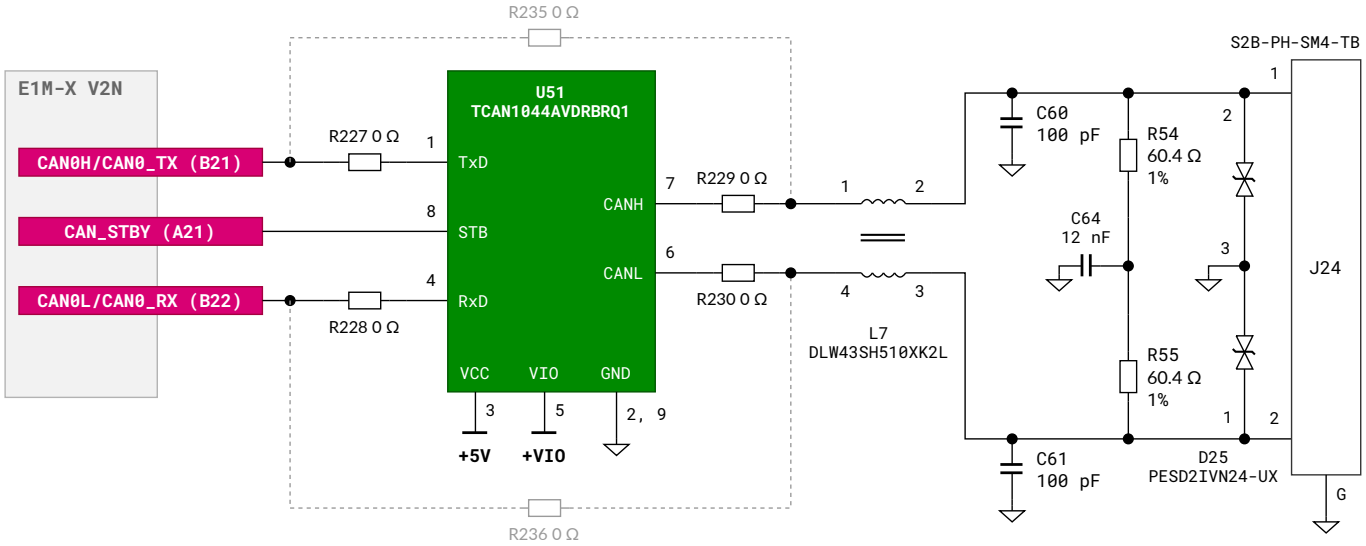
Figure 8 MIPI DSI routing example with backlight driver

7.5 CAN-Bus

- 2 × CAN-FD controllers of the RZ/V2N on the pads; the on-module CAN transceivers (TI TCAN1044AVDRBRQ1) are **not fitted** on the V2N module
- CAN0H/CAN0_TX (B21), CAN0L/CAN0_RX (B22), CAN1H/CAN1_TX (B24) and CAN1L/CAN1_RX (B25) carry the 1.8 V CAN-FD TX / RX logic signals
- The carrier **SHALL** add a CAN transceiver per port, with its VIO on VIO_OUT (the E1M-X development board uses TI TCAN1044AVDRBRQ1); CAN_STBY (A21) can drive the transceiver standby inputs

Add 120 Ω termination at each end of the bus (split termination on the E1M-X development board) and ESD / EMI protection at the connector.

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E1M-X development board CAN0, drawn as reworked for a V2N module (CAN1: U52, L8, D27, J25 the same way). On V2N, B21 / B22 are 1.8 V CAN-FD TX / RX logic pins: the carrier transceiver (VIO on +VIO, the module VIO_OUT pad) is required. Never connect the bus to B21 / B22 directly. As assembled (2626-R2 pick-and-place, DNP variant) the board has R235-R238 fitted and R227-R234 not fitted: with a V2N, fit R227-R234 and remove R235-R238 (dashed grey: the transceiver bypass) before connecting a bus to J24 / J25.

Figure 9 CAN-BUS reference transceiver, termination and connector

Warning: Hardware-damage hazard. B21 / B22 / B24 / B25 are 1.8 V logic pins on the V2N module. Never connect a CAN bus directly to them: bus voltages destroy the SoC pins. Always place a transceiver on the carrier (an isolated transceiver if the application needs isolation).

Warning: Hardware-damage hazard on the E1M-X development board. As assembled (2626-R2 pick-and-place, DNP variant), the board has the transceiver bypass links R235– R238 fitted and R227– R234 not fitted, so J24 / J25 connect straight to B21 / B22 / B24 / B25. With a V2N module, fit R227– R234 and remove R235– R238 before you connect a CAN bus to J24 / J25.

7.6 PCIe

- PCIe Gen3, 2 lanes (`PCIE0_*`)
- Differential signalling, controlled-impedance routing required
- The reference clock is generated on the module: `PCIE0_CLK_P` / `PCIE0_CLK_N` (A47 / B47) carry output `DIFF1` of the on-module clock generator through the on-module reference-clock buffer. The RZ/V2N root complex takes output `DIFF2` of the same PLL (common clock). Route `PCIE0_CLK` to the REFCLK input of the carrier device; the carrier **must not** add a second reference-clock source
- `PCIE0_TX0` / `PCIE0_TX1` are AC-coupled on the module (0.22 µF); add AC coupling only on the `PCIE0_RX*` lanes, at the carrier device's transmitter
- The lanes reach the `PCIE0_*` pads through an on-module PCIe multiplexer. Its PD input is pulled high (power-down) and its SEL input is pulled low on the module; software enables it and selects the pads through `P80` (PD) and `P95` (SEL)

Route the four data pairs + clock as 85 Ω differential, matched ±2 ps within each pair. PCIe is single-instance on V2N; M.2 Key M and Key E on the reference carrier share this controller via a switch (see **E1M-X EVK User Guide** (UG-E1M-X-001) for the switching scheme).

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> **Note:** For the V2N-M1 family the PCIe controller is multiplexed with the on-module DeepX DX-M1. See **E1M-X V2N-M1 HW Design Guide** (HG-V2N-M1-001) §6.7 for the bring-up details.

7.7 USB

- 1 × USB 3.2 Gen 2 (`USB0_30_*`) – Host or Function
- 1 × USB 2.0 (`USB2_*`) – Host or Function via `USB2_ID`
- `USB_CC1` / `USB_CC2` (A2 / B2) are not connected on the module: a USB-C connector needs its CC handling (pull-downs or a port controller) on the carrier

Route the USB 3.2 differential pairs as 85 Ω; the USB 2.0 pair as 90 Ω. Match lengths within each pair to within ±2 ps.

7.8 Digital Communication

- UART (× 2), SPI (× 3), I^2C (× 4), I^3C (× 1), I^2S (× 2)
- Pin-mux configured in software via the Alp SDK™
- I^2C / I^3C **require** external pull-ups (TBD kΩ) on the carrier. Exception: `GP_I2C` (AO3 / AP3) has its pull-ups on the module and takes none on the carrier (Section 4.3)
- SPI chip-selects handled on the carrier

> E1M-X uses a fixed pin-mux at the standard level. Use the relevant default function in your application; tertiary functions are silicon-specific and must be declared in the per-SoM manifest per **E1M Spec** §8.4.

7.9 Audio and Sensor Interfaces

- 2 × I^2S, 2 × PDM (up to 4 digital microphones)
- Audio master clock available on `AUDIO_CLK`
- Keep audio clocks clean and isolated from switching power planes

7.10 Analog Interfaces

- 8 × ADC inputs via the secondary MCU (`ANA_S0`…`ANA_S7`)
- 2 × DAC outputs via the secondary MCU (`DAC0`, `DAC1`)
- All analog signals are 1V8-referenced
- Keep analog routing short and isolated from digital aggressors

7.11 PWM and Encoder Interfaces

- 8 × PWM outputs
- 4 × quadrature-encoder inputs
- Suitable for motor and control applications
- Software configuration via Alp SDK™

8 Software Support

8.1 Alp SDK™

- Open-source, CMSIS-compliant
- Unified HAL across all E1M-X variants (V2N, V2N-M1, future SKUs)
- Vendor-agnostic software architecture

The SDK build targets for V2N are per SKU:

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- RZ/V2N quad Cortex-A55 (1.8 GHz) — Linux via Yocto `MACHINE` `e1m-v2n101-a55` / `e1m-v2n102-a55` / `e1m-v2n103-a55`
- RZ/V2N internal Cortex-M33 system manager (200 MHz) — Zephyr board target `alp_e1m_v2n101_m33_sm/r9a09g056n48gbg/cm33` on `E1M-V2N101` (the `E1M-V2N102` / `E1M-V2N103` M33 board trees are not yet built)

The on-module GD32 supervisor (216 MHz) is not a customer build target: it runs bridge firmware that Alp Lab programs in production, reached from the RZ/V2N through `<alp/chips/gd32g553.h>` and updated in the field over the bridge link. Customer reflashing of the GD32 is supported only to recover a bricked module.

8.2 AI Acceleration

- Renesas DRP-AI3, 4 TOPS dense, integrated in the RZ/V2N silicon
- Mali-C55 ISP for camera pre-processing
- Optimised for vision workloads (driver monitoring, object detection, classification)

For inference exceeding 4 TOPS, see the **E1M-X V2N-M1 HW Design Guide** (HG-V2N-M1-001) which adds the on-module DeepX DX-M1 25-TOPS accelerator.

9 Bring-Up Checklist

9.1 Pre-Power Checks

- Confirm the correct SoM variant (`E1M-V2N101`, `E1M-V2N102` or `E1M-V2N103`).
- Verify orientation and solder joints (A1 corner against carrier fiducial).
- Ensure only 5 V is connected to `VDD_5V_IN`.
- Check ground continuity across all 105 `GND` pads.
- Confirm DIP-switch state for the intended boot mode.

9.2 First Power-On

- Apply 5 V.
- Monitor current consumption (expected idle: TBD mA).
- Check for abnormal heating on the SoM.
- Confirm `PWR` and `IO_EN` LEDs light within 100 ms.
- Open the console UART at 115 200 8N1 and watch for boot output.

9.3 Basic Validation

- UART boot / debug output on the SCIF console.
- Both Ethernet links coming up when cables are plugged in.
- GPIO or PWM toggle from a simple Zephyr build.

9.4 Common Issues

- Wrong DIP-switch position for the intended boot device (most common first-time failure).
- Missing Ethernet magnetics or RJ45 with wrong wiring.
- Wrong firmware image (built for the wrong core / wrong SKU).
- USB-C cable that doesn't support data lines (power-only cables are common).
- Insufficient supply current under PCIe SSD + AI load.

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10 Design Checklist (Summary)

Item	Status
Single 5 V supply, ≥ 5 A rated	OK
Bulk + decoupling capacitance close to VDD_5V_IN	OK
Ethernet magnetics + RJ45 on both ports	OK
Controlled-impedance MIPI and PCIe routing	OK
RF-clean antenna routing, ≥ 1 RF connector or PCB antenna	OK
CAN transceiver, termination + ESD on both CAN ports	OK
Every boot strap set by a 1 kΩ resistor (pull-up to VIO_OUT for 1, pull-down to GND for 0): BOOT0 / BOOT1 DIP switch with 1 kΩ pull-downs, or hard-strap; BOOT2 (X1) 1 kΩ pull-up; BOOT3 (Y1) 1 kΩ pull-up for CA55 boot or 1 kΩ pull-down for CM33 boot	OK
PORn and MODULE_EN accessible (button or test-point)	OK
MODULE_EN / MODULE_STBY carrier leakage ≤ 0.1 µA per pad (ESD parts included); MODULE_EN held low ≥ 150 ms before 5 V is removed	OK
RTC_WAKE_N (AD3): carrier pull-up to an always-on rail, ≤ 5.5 V, ≥ 10 kΩ, or left floating	OK
GP_I2C (AO3 / AP3): no carrier pull-ups; pads high-impedance whenever module 5 V is absent	OK
PMIC_GPIO5_10V (AI3) left open; no carrier nets routed through AD3, AI3, AO3 or AP3	OK
Debug header on JTAG / SWD pins (optional but recommended)	OK
Module mounted on a spacer PCB (soldered on both faces), or over a carrier cut-out the size of the central cavity (57.45 × 39.45 mm, R1.00, 3.775 / 2.775 mm from the left / top outline edges); no carrier components inside the cavity outline; never directly on the carrier	OK
Correct firmware per SKU + target core	OK

Table 4 V2N carrier-board design checklist

11 Ordering Information

E1M-X V2N modules are ordered based on:

- Memory tier (4 GB / 8 GB LPDDR4X; 4 GB / 16 GB eMMC)
- Assembly options (lead finish, ball material)

Refer to the **E1M-X V2N Datasheet** (DS-V2N-001) §15 for the complete ordering matrix and MPN decoder.

12 Notices

- Specifications subject to change without notice.
- Some features may be preliminary at this revision.
- Always verify against the latest **E1M-X V2N Datasheet** (DS-V2N-001).
- This guide complements but does not replace the Renesas RZ/V2N PCB design guidelines (`r01an7339ej0100-rzv2n-pcb-design-guidelines.pdf`) for SoC-internal routing.

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