E1M-X V2N-M1 — RENESAS RZ/V2N + DEEPX DX-M1

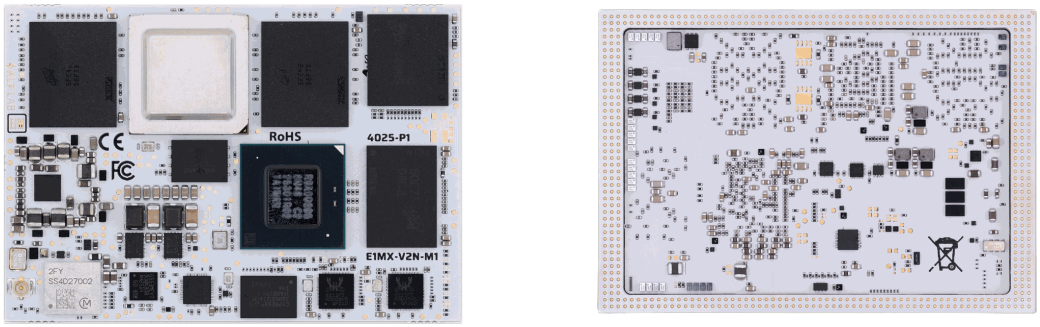


Figure 1 E1M-X V2N-M1 module — front (left) and back (right)

The E1M-X V2N-M1 module is built on the open E1M™ standard, with a unified pin layout and hardware functionality. This footprint allows users to interchange MPU modules seamlessly while keeping hardware compatible. E1M™ is designed for flexibility, functionality, and longevity in high- and medium-range MCU/MPUs.

Features

- **Renesas RZ/V2N**
  - Quad Arm® Cortex®-A55 (1.8 GHz)
  - Arm Cortex-M33 (200 MHz)
  - Arm Mali™-C55 ISP (Image Signal Processor)
  - Arm Mali™-G31 GPU
  - AI Accelerator DRP-AI3 — 4 dense TOPS
  - H.264 / H.265 codec
- **DeepX DX-M1 standalone AI accelerator**
  - Up to **25 TOPS** AI performance
  - PCIe-attached on-module to the RZ/V2N
  - 2 × LPDDR5X companion memory
  - SPI NAND companion storage
- **Dedicated I/O MCU**
  - Arm® Cortex®-M33 (216 MHz)
- **Various memory options**
  - LPDDR4X 32-bit 3.2 GT/s, up to 8 GB
  - eMMC — 4 GB to 256 GB
  - QSPI NOR – 512 Mbit, boot-supported
- **MIPI Display output** — 4 lanes
  - 1920 × 1200 RGB888 @ 60 fps
  - 1280 × 1024 RGB888 @ 120 fps
- **H.264 / H.265 codec**
  - H.264 1920 × 1080 × 60 fps
  - H.265 3840 × 2160p × 30 fps
- 2 × CSI-2 camera inputs — 4 lanes, up to 4K @ 30 fps, 4 virtual channels
- 2.4 GHz / 5 GHz / 6 GHz Wi-Fi® + Bluetooth® module
  - 802.11 a/b/g/n/ac/ax, 143 Mbps
  - Bluetooth® 5.4 BR/EDR/LE, 3 Mbps
- 2 × 1 Gbps Ethernet PHY
- 2 × CAN FD (CAN-BUS PHYs as an assembly option)
- PCIe Express® 3.0 — 2 lanes (multiplexed between on-module DeepX DX-M1 and external)
- Assembly variants available for cost reduction
- Smallest size in the industry: 45 × 65 mm

Applications

IoT, industrial, robotics, motor drive, drones, mobile PoS, smart speakers, object detection, medical devices, vending machines, smart home, process control, smart appliances, scanners.

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1 General Description

1.1 Highlights

The Alp Lab E1M-X V2N-M1 SoM (System-on-Module) is a high-performance, cost-effective solution designed for a range of AI-driven vision applications. Powered by the Renesas RZ/V2N processor **and** the DeepX standalone AI accelerator, it features an Arm® Quad Cortex®-A55 (1.8 GHz) CPU, an integrated AI accelerator, and a 4K encoder/decoder, making it optimised for vision-based tasks. The E1M-X V2N-M1 SoM supports up to two cameras via 2 × 4-lane MIPI CSI-2 connections and offers customisable options such as on-board Wi-Fi / Bluetooth, multiple memory and storage capacities, and PHY configurations.

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1.2 Block Diagram

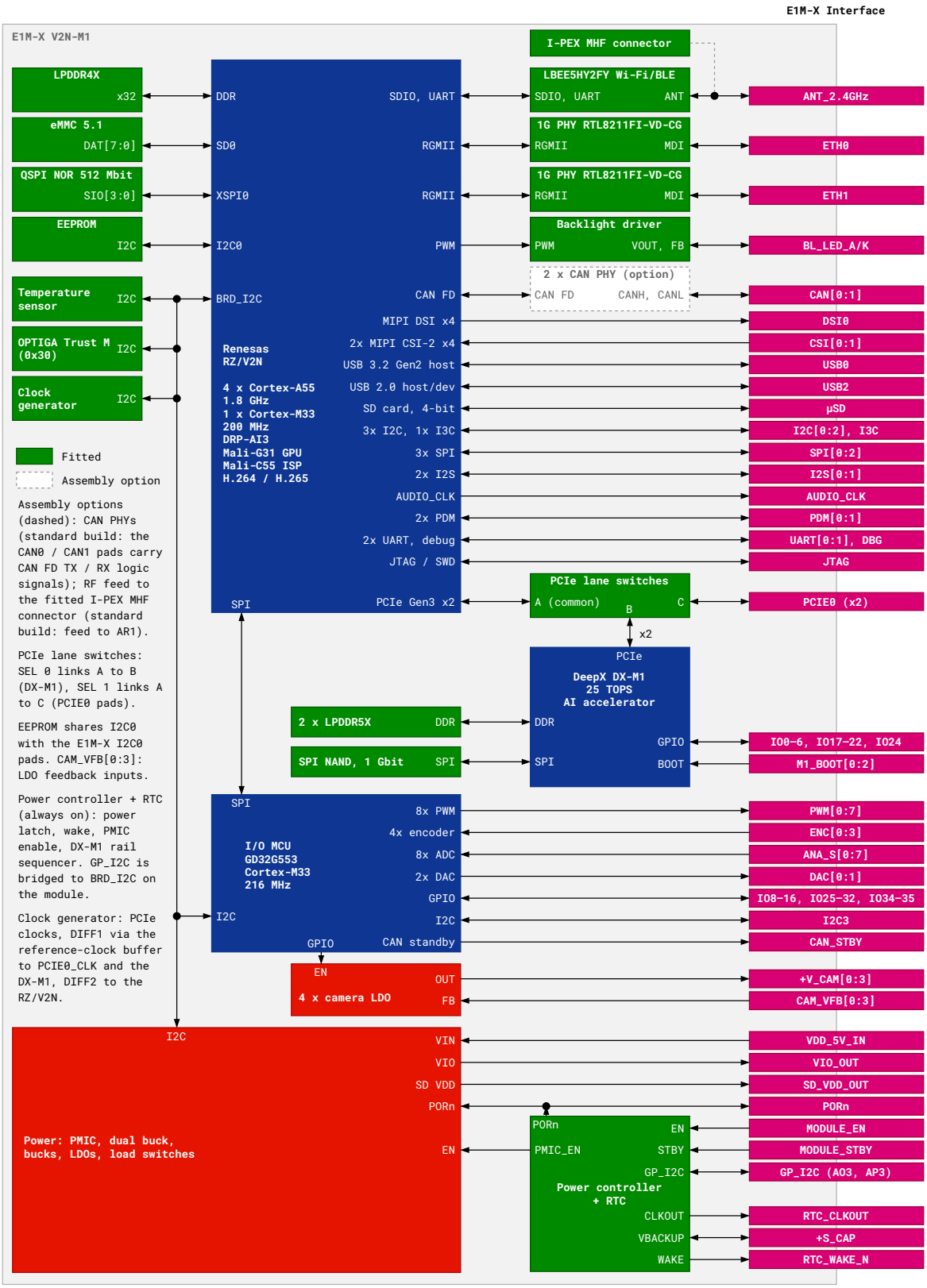


Figure 2 E1M-X V2N-M1 Block Diagram

1.3 Module Variants

The E1M-X V2N-M1 family ships in three MPN variants. All three populate the full V2N silicon stack **plus** the on-module DeepX DX-M1 accelerator and its companion memory; they differ only in the main-memory tier. See Section 16 for the full ordering matrix and MPN decoder.

MPN	Renesas part	LPDDR4X	eMMC	AI capability
E1M-V2M101	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 4 GB	V2N: 4 TOPS + DX-M1: 25 TOPS
E1M-V2M102	R9A09G056N44GBG#AC0	8 GB	eMMC 5.1, 16 GB	V2N: 4 TOPS + DX-M1: 25 TOPS
E1M-V2M103	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 16 GB	V2N: 4 TOPS + DX-M1: 25 TOPS

Table 1 E1M-X V2N-M1 Variant Summary

1.4 Renesas RZ/V2N MPU

The RZ/V2N is a vision-AI microprocessor (MPU) with Renesas' proprietary AI accelerator (DRP-AI3) supporting up to 15 TOPS of AI performance. Its CPUs are quad Arm® Cortex®-A55 (1.8 GHz) and Arm Cortex-M33 (200 MHz). The RZ/V2N is equipped with an ISP (Image Signal Processor) and dual-channel MIPI® CSI-2® camera interfaces for supporting dual-camera signal processing, which is crucial for realising vision systems. It is also equipped with high-speed interfaces such as PCIe® and USB 3.2, allowing for the expansion of external devices. The RZ/V2N is an ideal microprocessor for applications requiring both low power consumption and advanced AI inference, such as DMS (Driver Monitoring System), monitoring cameras, mobile robots, and more.

This document should be read together with the V2N datasheet from Renesas.

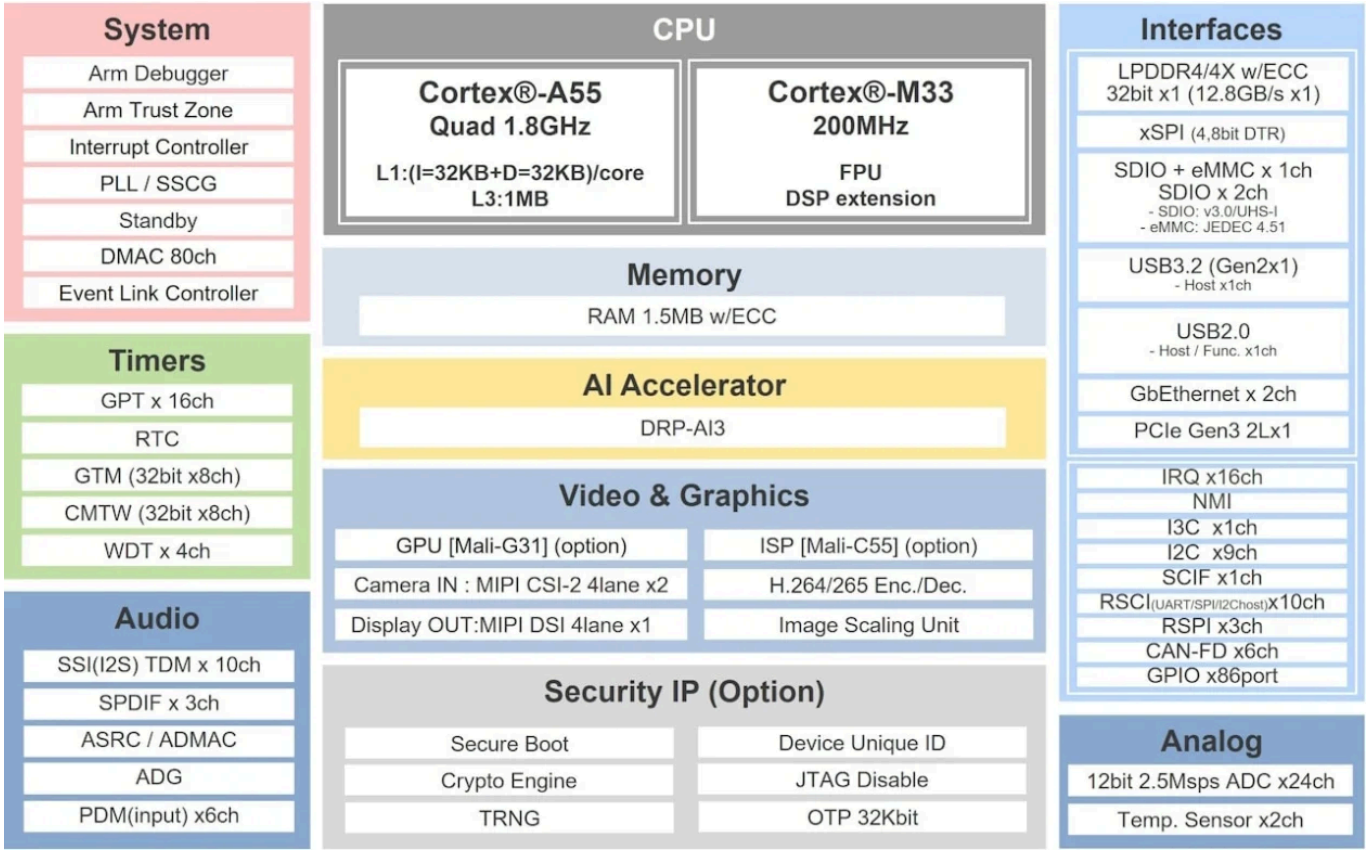


Figure 3 Renesas RZ/V2N MPU block diagram (source: Renesas Electronics)

Blocks marked (option) depend on the RZ/V2N part number; see Ordering Information.

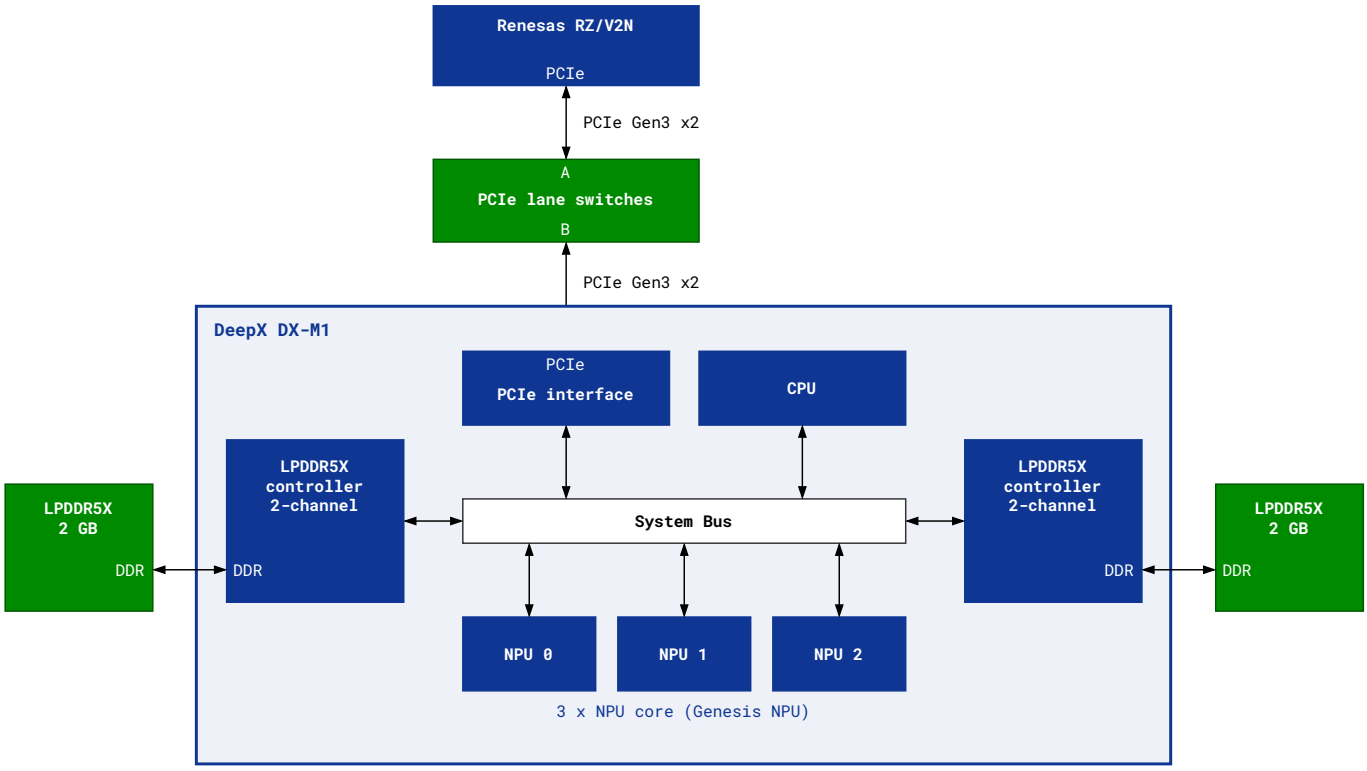
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Key MPU features:

- Cortex-A55 (1.8 GHz) × 4 cores
- Cortex-M33 (200 MHz) × 1 core
- AI Accelerator DRP-AI
- Arm Mali™-C55 ISP (option)
- 1.5 MB on-chip SRAM
- LPDDR4 / LPDDR4X memory interface
- Gigabit Ethernet 2 ch
- USB 2.0 interface 1 ch (Host/Function)
- USB 3.2 (Gen2) interface 1 ch (Host only)
- PCIe interface (Gen3, 2-lane) 1 ch
- MIPI CSI-2 camera interface 2 ch
- CAN interface (CAN FD) 6 ch
- AD converter 24 ch

1.5 DeepX DX-M1 — Standalone AI Accelerator

The DX-M1 is a 25 TOPS AI processor with class-leading power efficiency. DeepX designed the DX-M1 with the highest IPS (inference-per-second) per watt as a main goal. It is used as an AI accelerator with a host. The DX-M1 NPU is designed for deep-learning algorithm coverage including computer-vision tasks such as image classification, object detection, and identification of audio streams (e.g. keyword spotting). To speed up software development, DeepX provides a comprehensive software environment that includes an SDK and a model-zoo verified on DX-M1. The DX-COM™ tool automatically converts neural networks built in popular frameworks (PyTorch, ONNX, …) into optimised executable code for the DX-M1.



On the module the DX-M1 links to the RZ/V2N over PCIe Gen3 x2 through the PCIe lane switches (SEL = 0 links port A, the RZ/V2N, to port B, the DX-M1; U-Boot selects the DX-M1), and has 2 x LPDDR5X, 2 GB each.

Figure 4 DeepX DX-M1 Block Diagram

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2 Pin Diagram and List

The E1M-X™ standard defines the primary pin functions; the pin-out below follows that standard. Pins can be reassigned to alternate functions in software, but hardware compatibility with other E1M-X variants will no longer hold because each MCU/MPU has a different pin structure and peripheral mapping.

The pin-out is drawn in the top view (component side up), landscape: 65 mm across and 45 mm down. A1 is the top-left corner pad, 1.0 mm from the left and top edges, at the pin-1 fiducial. The pad letters A–AR are the rows, running top to bottom; the pad numbers 1–64 are the columns, running left to right. A2 is directly to the right of A1 and B1 directly below it. The pad band is two pads deep at the top and bottom edges (rows A, B and AQ, AR) and three pads deep at the left and right edges (columns 1–3 and 62–64). This is the frame of the alplab.ai pinout viewer and of the original E1M-X pinout drawing. The map is split into four quarters so that every pad name stays legible.

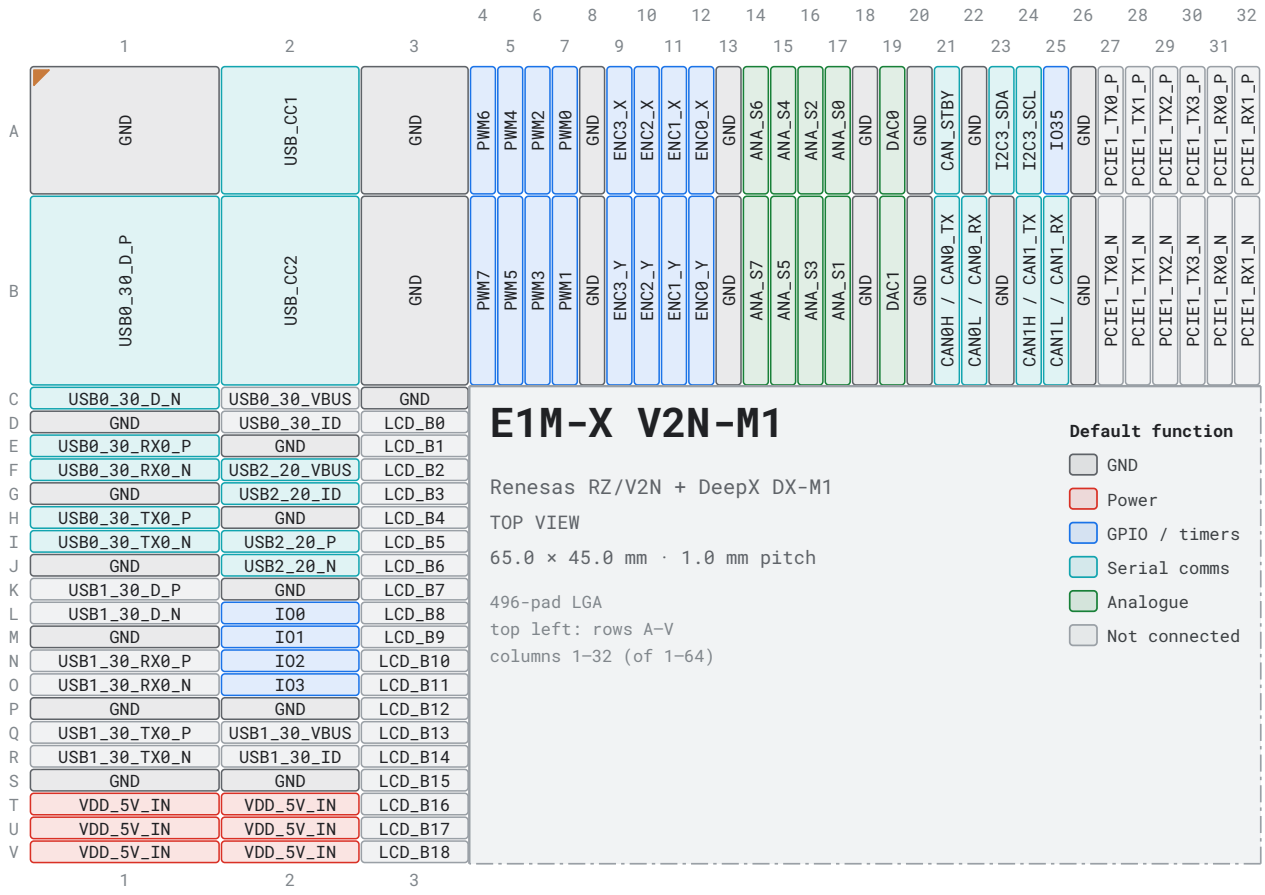


Figure 5 E1M-X V2N-M1 Pin-out (top view, 496-pad LGA), top left: rows A–V, columns 1–32

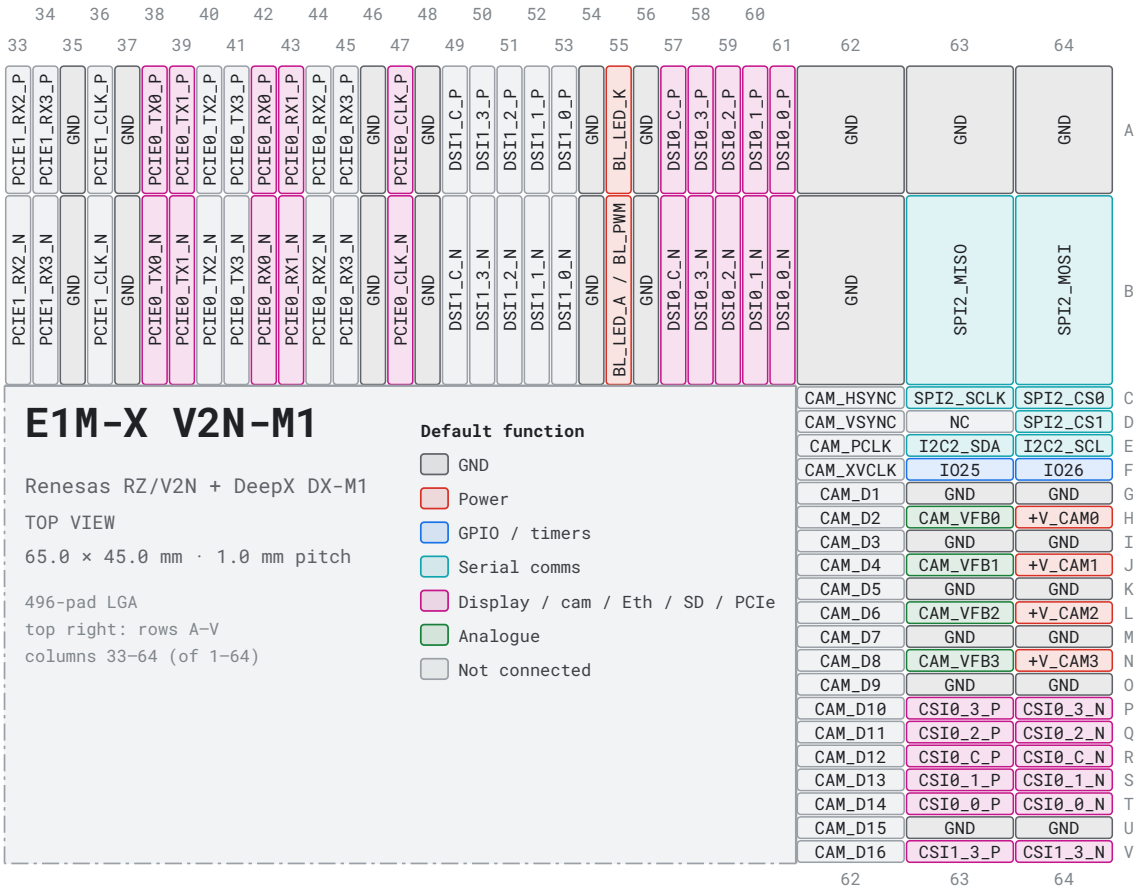


Figure 6 E1M-X V2N-M1 Pin-out (top view, 496-pad LGA), top right: rows A–V, columns 33–64

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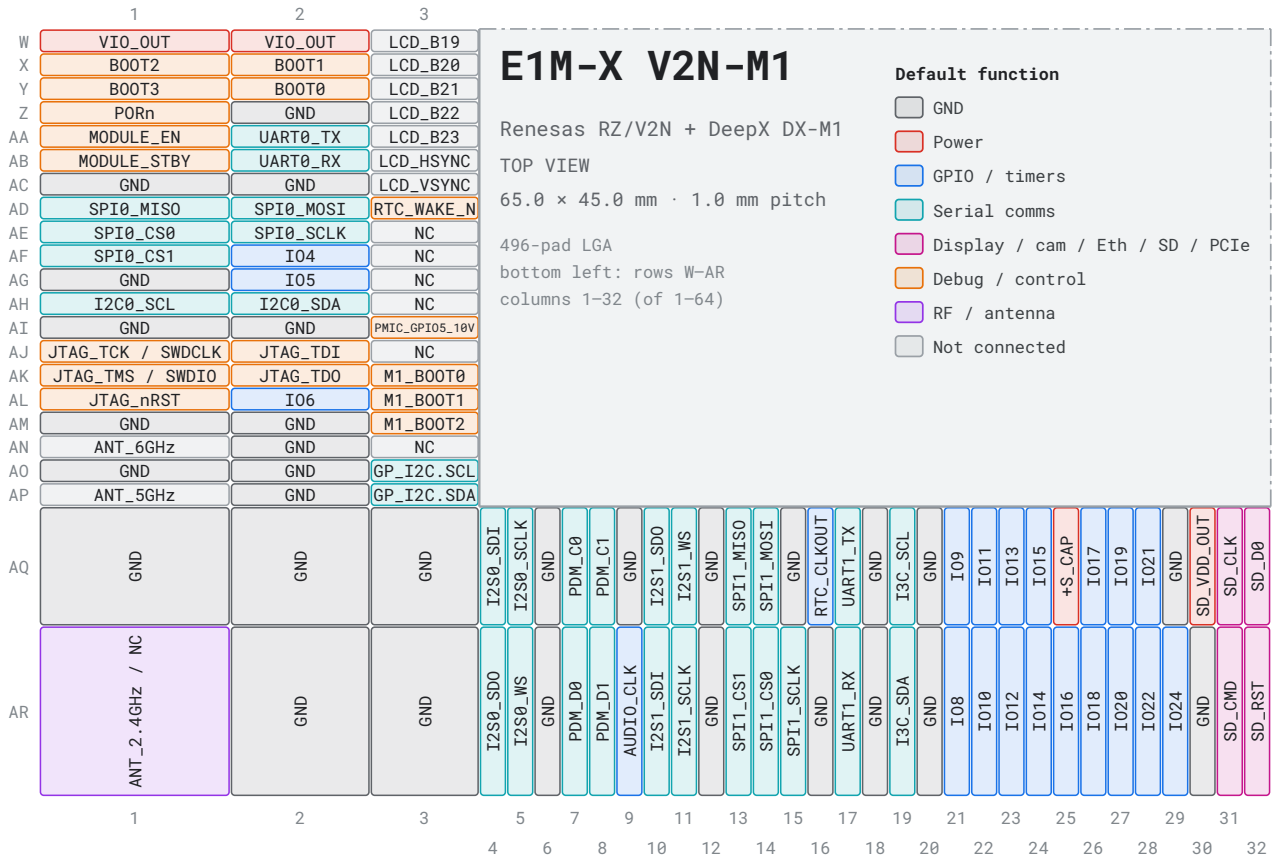


Figure 7 E1M-X V2N-M1 Pin-out (top view, 496-pad LGA), bottom left: rows W–AR, columns 1–32

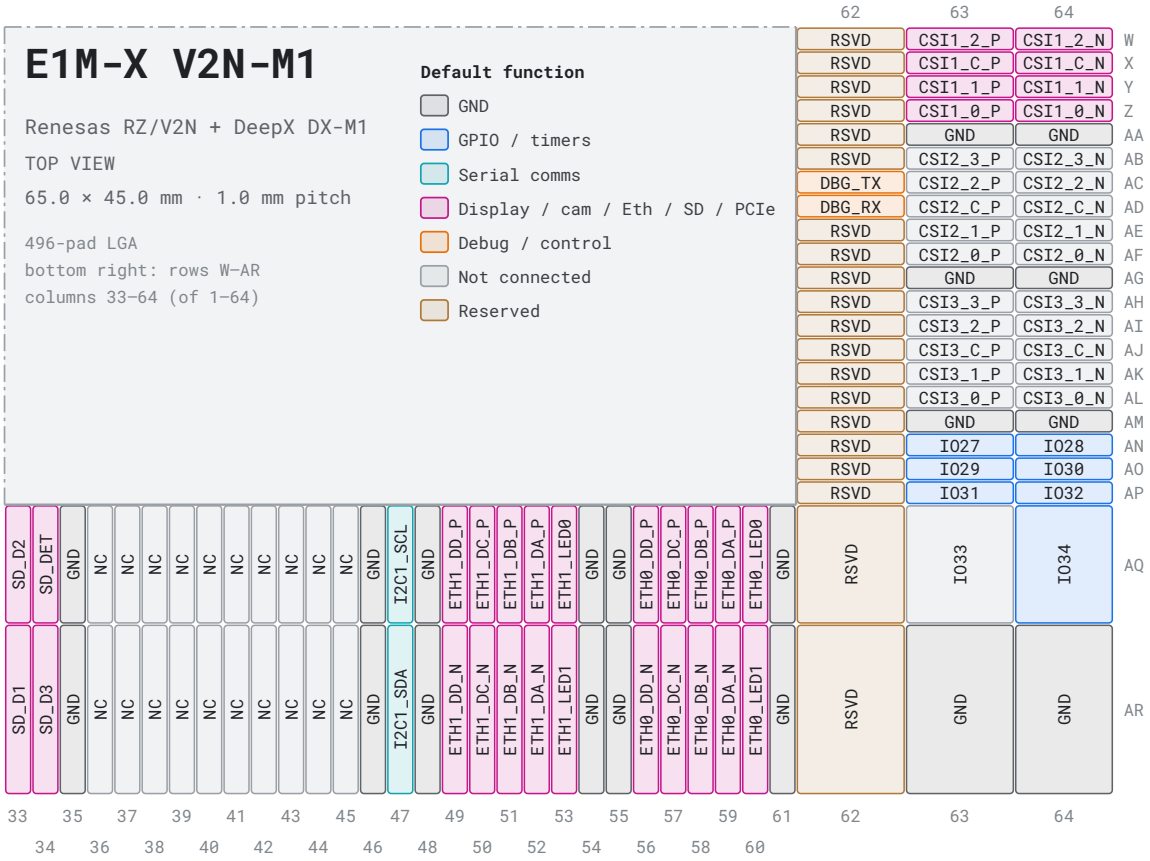


Figure 8 E1M-X V2N-M1 Pin-out (top view, 496-pad LGA), bottom right: rows W–AR, columns 33–64

2.1 Power & Control Pins

Pin Number	Pin Name	Description
A13, K63, AQ15, M1, M63, O63, A18, AQ18, P1, A20, AQ20, S1, A22, U63, A26, AA63, AQ29, AC1, AQ6, D1, A35, AG1, AG63, AQ35, A37, AI1, AM1, AM63, AO1, AQ1, A46, AQ46, AR63, A48, AQ48, A8, A54, AQ54, AQ55, A56, AQ61, A62, AQ9, G1, G63, I63, AQ12, J1, A1, A3, A63, AQ3, C3, K64, M64, O64, U64, AA64, AG64, AM64, AR64, G64, I64, A64, AR16, AR18, AR20, AR30, AR6, AR35, AR46, AR48, AR54, AR55, AR61, AR12, AR3, B13, K2, B18, P2, B20, S2, B23, B26, Z2, AC2, B35, AI2, B37, AM2, AN2, AO2, E2, AP2, AQ2, AR2, B46, B48, B8, B54, B56, B62, H2, B3	GND	Connect to ground.
W1, W2	VIO_OUT	+1V8 output for I/O power. Up to TBD mA.
T1, U1, V1, T2, U2, V2	VDD_5V_IN	+5 V main supply input to the module.
AQ25	+S_CAP	RTC backup supply input (net VBAT), connected directly to the backup input of the on-module RTC. Connect the carrier backup super-capacitor

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Pin Number	Pin Name	Description
		here. The module has no backup capacitor of its own. See Section 4.2.
Y2	BOOT0	Boot selection for Renesas RZ/V2N. Carrier strap: 1 kΩ pull-up to VIO_OUT for 1, 1 kΩ pull-down to GND for 0. See Section 4.5.
X2	BOOT1	Boot selection for Renesas RZ/V2N. Carrier strap: 1 kΩ pull-up to VIO_OUT for 1, 1 kΩ pull-down to GND for 0. See Section 4.5.
X1	BOOT2	Connected to the RZ/V2N MD_BOOT3 strap; no pull-up on the module. Fit a 1 kΩ pull-up to VIO_OUT on the carrier (BOOT2 = 1). See Section 4.5.
Y1	BOOT3	Boot CPU selection. High: RZ/V2N internal CA55 boot. Low: RZ/V2N internal CM33 boot. Also connected on the module, through an on-module 0 Ω link, to GPIO5 of the PMIC, which is an input (Hi-Z), and to pad AI3 (PMIC_GPIO5_10V). Carrier strap: 1 kΩ pull-up to VIO_OUT for CA55 boot (BOOT3 = 1), 1 kΩ pull-down to GND for CM33 boot (BOOT3 = 0).
AL1	JTAG_nRST	JTAG / SWD pins for programming and debug.
AJ1	JTAG_TCK / SWDCLK	
AJ2	JTAG_TDI	
AK2	JTAG_TDO	
AK1	JTAG_TMS / SWDIO	
AA1	MODULE_EN	Module enable input to the power controller, through an on-module clamp (1 MΩ pull-up to the 1.8 V always-on rail behind the clamp). Released: module on. Held low: module off. Carrier drive: open drain with no pull-up, a switch to GND, or push-pull logic from 1.8 V to 5 V. Leave floating if not used. See Section 6.1.
Z1	PORn	Power-on reset, open drain at 1.8 V: the PMIC reset output, with a 10 kΩ pull-up to VDD1G_1P8 on the module; the power controller also pulls it low. Pull low to reset the RZ/V2N with the rails kept up. No carrier pull-up. Leave floating if not used.
AB1	MODULE_STBY	Stand-by / wake request input to the power controller, through an on-module clamp (1 MΩ pull-up to the 1.8 V always-on rail behind the clamp). Same carrier drive options as MODULE_EN. Leave floating if not used. See Section 6.1.
AD3	RTC_WAKE_N	RTC wake output, active low, open drain. Valid in every module state while 5 V is present. Carrier pull-up to its always-on rail, ≤ 5.5 V, ≥ 10 kΩ. See Section 6.1.
AI3	PMIC_GPIO5_10V	PMIC GPIO5, the PMIC in-circuit programming path (about 10 V). Joined on the module through an on-module 0 Ω link to BOOT3 (Y1, RZ/V2N BOOTSELCPU): in normal use AI3 is electrically the same node as BOOT3, so a carrier that drives or straps AI3 also drives BOOT3.
AK3	M1_BOOT0	DX-M1 boot strap (DX-M1 GPIO00_00). 10 kΩ pull-down fitted on the module (default 0); 10 kΩ pull-up to M1_VDD_1V8 not fitted. Leave floating for the default. See Section 5.1.

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Pin Number	Pin Name	Description
AL3	M1_BOOT1	DX-M1 boot strap (DX-M1 GPIO00_01). 10 kΩ pull-down fitted (default 0); pull-up not fitted.
AM3	M1_BOOT2	DX-M1 boot strap (DX-M1 GPIO00_02). 10 kΩ pull-down fitted (default 0); pull-up not fitted.
A2	USB_CC1	USB Type-C Configuration Channel 1.
B2	USB_CC2	USB Type-C Configuration Channel 2.
AQ30	SD_VDD_OUT	SD-card voltage output. Connect to SD card VDD.
H64	+V_CAM0	CAM0 LDO output. 0.6 V to 3.3 V, 300 mA max.
J64	+V_CAM1	CAM1 LDO output. 0.6 V to 3.3 V, 300 mA max.
L64	+V_CAM2	CAM2 LDO output. 0.6 V to 3.3 V, 300 mA max.
N64	+V_CAM3	CAM3 LDO output. 0.6 V to 3.3 V, 300 mA max.
H63	CAM_VFB0	Feedback node for +V_CAM0. Place divider close to the module pin.
J63	CAM_VFB1	Feedback node for +V_CAM1. Place divider close to the module pin.
L63	CAM_VFB2	Feedback node for +V_CAM2. Place divider close to the module pin.
N63	CAM_VFB3	Feedback node for +V_CAM3. Place divider close to the module pin.
B55	BL_LED_A / BL_PWM	BL_LED_A: anode of backlight. BL_PWM: connect to backlight driver.
A55	BL_LED_K	Cathode of backlight. Leave floating if BL_PWM is used.

Table 2 E1M-X V2N-M1 Power & Control Pins

Note: The E1M-X™ standard lists pads AD3–AP3 as NC. On the V2N-M1 module, AD3 (RTC_WAKE_N), AI3 (PMIC_GPIO5_10V), AK3–AM3 (M1_BOOT0–M1_BOOT2) and AO3 / AP3 (GP_I2C.SCL / GP_I2C.SDA, see Section 2.3) carry module signals. A carrier must not route its own nets through these pads.

Warning: Hardware-damage hazard. PMIC_GPIO5_10V (AI3) is the PMIC in-circuit programming path, which takes about 10 V. Apply 10 V to AI3 only with the on-module 0 Ω link to BOOT3 removed. With the link fitted, the 10 V reaches the RZ/V2N BOOTSELCPU input and destroys the RZ/V2N. In normal use AI3 is electrically the same node as BOOT3 (Y1).

Warning: Back-power hazard. A carrier pull-up on M1_BOOT0–M1_BOOT2 (AK3–AM3) must come from a rail that is off whenever the DX-M1 I/O rail M1_VDD_1V8 is off; otherwise the DX-M1 I/O is back-powered through the pull-up.

2.2 Analog Pins

Pin Number	Pin Name	Peripheral	Description
A17	ANA_S0	AIN	Analog input channels, referenced to 1V8.
B17	ANA_S1		
A16	ANA_S2		
B16	ANA_S3		
A15	ANA_S4		

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Pin Number	Pin Name	Peripheral	Description
B15	ANA_S5		
A14	ANA_S6		
B14	ANA_S7		
A19	DAC0	DAC0	Analog output channels, referenced to 1V8.
B19	DAC1	DAC1	
AR1	ANT_2.4GHz / NC		ANT: module antenna output for Wi-Fi 6 and BLE. Route 50 Ω trace. NC: leave floating.

Table 3 E1M-X V2N-M1 Analog Pins

2.3 Digital Pins

Pin Number	Pin Name	Peripheral	Description
AR21	IO8	GPIO / SMCU	General purpose I/O, controlled by the secondary MCU on E1M-X.
AQ21	IO9		
AR22	IO10		
AQ22	IO11		
AR23	IO12		
AQ23	IO13		
AR24	IO14		
AQ24	IO15		
AR25	IO16		
F63	IO25		
F64	IO26		
AN63	IO27		
AN64	IO28		
AO63	IO29		
AO64	IO30		
AP63	IO31		
AP64	IO32		
AQ64	IO34		
A25	IO35		
AQ16	RTC_CLKOUT	RTC	Real-time clock output.
AC62	DBG_TX	DBG	On-module debug UART transmit.
AD62	DBG_RX	DBG	On-module debug UART receive.
L2	IO0	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
M2	IO1	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
N2	IO2	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
O2	IO3	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AF2	IO4	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.

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Pin Number	Pin Name	Peripheral	Description
AG2	IO5	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AL2	IO6	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AQ26	IO17	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AR26	IO18	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AQ27	IO19	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AR27	IO20	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AQ28	IO21	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AR28	IO22	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AR29	IO24	GPIO	General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch.
AR9	AUDIO_CLK	–	Audio clock output.
AQ7	PDM_C0	PDM0	Digital microphone interface. PDM_C is the clock, PDM_D is the data line.
AR7	PDM_D0		
AQ8	PDM_C1	PDM1	Digital microphone interface.
AR8	PDM_D1		
AQ5	I2S0_SCLK	I2S0	I^2S interface.
AQ4	I2S0_SDI		
AR4	I2S0_SDO		
AR5	I2S0_WS		
AR11	I2S1_SCLK	I2S1	I^2S interface.
AR10	I2S1_SDI		
AQ10	I2S1_SDO		
AQ11	I2S1_WS		
AH1	I2C0_SCL	I2C0	I^2C interface.
AH2	I2C0_SDA		
AQ47	I2C1_SCL	I2C1	I^2C interface.
AR47	I2C1_SDA		
E64	I2C2_SCL	I2C2	I^2C interface.
E63	I2C2_SDA		
A24	I2C3_SCL	I2C3	I^2C interface, controlled by the secondary MCU on E1M-X.
A23	I2C3_SDA		
AO3	GP_I2C.SCL	GP_I2C	Always-on I^2C, 3.3 V, open drain: the power controller (0x08, also its programming port) and the RTC (0x52). 4.7 kΩ pull-ups to +3V3_AON on SCL and SDA on the module. No carrier pull-ups. See Section 8.4.2.
AP3	GP_I2C.SDA		
AQ19	I3C_SCL	I3C	I^3C interface.
AR19	I3C_SDA		
AE1	SPI0_CS0	SPI0	SPI interface.

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Pin Number	Pin Name	Peripheral	Description
AF1	SPI0_CS1		
AD1	SPI0_MISO		
AD2	SPI0_MOSI		
AE2	SPI0_SCLK		
AR14	SPI1_CS0	SPI1	SPI interface.
AR13	SPI1_CS1		
AQ13	SPI1_MISO		
AQ14	SPI1_MOSI		
AR15	SPI1_SCLK		
C64	SPI2_CS0	SPI2	SPI interface.
D64	SPI2_CS1		
B63	SPI2_MISO		
B64	SPI2_MOSI		
C63	SPI2_SCLK		
AB2	UART0_RX	UART0	UART interface.
AA2	UART0_TX		
AR17	UART1_RX	UART1	UART interface.
AQ17	UART1_TX		
B21	CAN0H / CAN0_TX	CAN0	CAN-BUS interface.
B22	CAN0L / CAN0_RX		
B24	CAN1H / CAN1_TX	CAN1	CAN-BUS interface.
B25	CAN1L / CAN1_RX		
A21	CAN_STBY	CAN	Standby control for CAN-BUS.
A7	PWM0	PWM	PWM output, controlled by the secondary MCU on E1M-X.
B7	PWM1		
A6	PWM2		
B6	PWM3		
A5	PWM4		
B5	PWM5		
A4	PWM6		
B4	PWM7		
A12	ENC0_X	ENC0	Encoder input.
B12	ENC0_Y		
A11	ENC1_X	ENC1	Encoder input.
B11	ENC1_Y		
A10	ENC2_X	ENC2	Encoder input.
B10	ENC2_Y		
A9	ENC3_X	ENC3	Encoder input.
B9	ENC3_Y		
AR56	ETH0_DD_N	ETH0	Ethernet interface. 1 Gbit PHY connection.
AQ56	ETH0_DD_P		
AR57	ETH0_DC_N		
AQ57	ETH0_DC_P		
AR58	ETH0_DB_N		

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Pin Number	Pin Name	Peripheral	Description
AQ58	ETH0_DB_P		
AR59	ETH0_DA_N		
AQ59	ETH0_DA_P		
AQ60	ETH0_LED0		
AR60	ETH0_LED1		
AR49	ETH1_DD_N	ETH1	Ethernet interface. 1 Gbit PHY connection.
AQ49	ETH1_DD_P		
AR50	ETH1_DC_N		
AQ50	ETH1_DC_P		
AR51	ETH1_DB_N		
AQ51	ETH1_DB_P		
AR52	ETH1_DA_N		
AQ52	ETH1_DA_P		
AQ53	ETH1_LED0		
AR53	ETH1_LED1		
AQ31	SD_CLK	SD0	SD card or eMMC interface.
AR31	SD_CMD		
AQ32	SD_D0		
AR33	SD_D1		
AQ33	SD_D2		
AR34	SD_D3		
AQ34	SD_DET		
AR32	SD_RST		
T64	CSI0_0_N	CSI0	MIPI CSI camera interface.
T63	CSI0_0_P		
S64	CSI0_1_N		
S63	CSI0_1_P		
Q64	CSI0_2_N		
Q63	CSI0_2_P		
P64	CSI0_3_N		
P63	CSI0_3_P		
R64	CSI0_C_N		
R63	CSI0_C_P		
Z64	CSI1_0_N	CSI1	MIPI CSI camera interface.
Z63	CSI1_0_P		
Y64	CSI1_1_N		
Y63	CSI1_1_P		
W64	CSI1_2_N		
W63	CSI1_2_P		
V64	CSI1_3_N		
V63	CSI1_3_P		
X64	CSI1_C_N		
X63	CSI1_C_P		
B61	DSI0_0_N	DSI0	MIPI DSI display interface.

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Pin Number	Pin Name	Peripheral	Description
A61	DSI0_0_P		
B60	DSI0_1_N		
A60	DSI0_1_P		
B59	DSI0_2_N		
A59	DSI0_2_P		
B58	DSI0_3_N		
A58	DSI0_3_P		
B57	DSI0_C_N		
A57	DSI0_C_P		
B47	PCIE0_CLK_N	PCIE0	PCIe interface (multiplexed with on-module DeepX DX-M1).
A47	PCIE0_CLK_P		PCIe reference clock output from the on-module reference-clock buffer (OUT0), fed by the clock generator DIFF1; the DX-M1 shares the same DIFF1 output. Present only while the DX-M1 rails are up. See Section 8.3.
B42	PCIE0_RX0_N		
A42	PCIE0_RX0_P		
B43	PCIE0_RX1_N		
A43	PCIE0_RX1_P		
B38	PCIE0_TX0_N		
A38	PCIE0_TX0_P		
B39	PCIE0_TX1_N		
A39	PCIE0_TX1_P		
C1	USB0_30_D_N	USB0	USB 3.0 interface.
B1	USB0_30_D_P		
F1	USB0_30_RX0_N		
E1	USB0_30_RX0_P		
I1	USB0_30_TX0_N		
H1	USB0_30_TX0_P		
G2	USB2_20_ID	USB2	USB 2.0 interface.
J2	USB2_20_N		
I2	USB2_20_P		
F2	USB2_20_VBUS		

Table 4 E1M-X V2N-M1 Digital Pins

Note: The pads controlled by the secondary MCU (GD32, 1.8 V I/O): PWM0–PWM7, ENC0–ENC3 X / Y and the GD32 GPIO pads (IO8–IO16, IO25–IO32, IO34, IO35) have no series resistors on the module. The GD32 drives them directly: drive strength and ESD robustness are those of the GD32 pin itself.

Warning: GP_I2C (AO3 / AP3): fit no carrier pull-ups (the module has 4.7 kΩ pull-ups to +3V3_AON), and keep both pads high-impedance whenever module 5 V is absent.

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2.4 DX-M1 GPIO Pads

Fourteen carrier pads connect directly to DX-M1 GPIOs. The table gives the DX-M1 pin behind each `M1_G0.n` net; the DX-M1 firmware pin map follows it.

Net	Pad	Pad name	DX-M1 GPIO	DX-M1 ball
M1_G0.0	AR26	IO18	GPIO01_00	AE10
M1_G0.1	AR27	IO20	GPIO01_01	AC10
M1_G0.2	AR28	IO22	GPIO00_04	AD14
M1_G0.3	AR29	IO24	GPIO00_06	AB9
M1_G0.4	AQ26	IO17	GPIO00_14	AC11
M1_G0.5	AQ27	IO19	GPIO01_04	AC9
M1_G0.6	AQ28	IO21	GPIO00_05	AB11
M1_G0.7	L2	IO0	GPIO00_15	AD11
M1_G0.8	M2	IO1	GPIO00_13	AD10
M1_G0.9	N2	IO2	GPIO01_07	AC8
M1_G0.10	O2	IO3	GPIO00_07	AD13
M1_G0.11	AF2	IO4	GPIO01_02	AE9
M1_G0.12	AG2	IO5	GPIO01_03	AD9
M1_G0.13	AL2	IO6	GPIO01_05	AE8

Table 5 E1M-X V2N-M1 DX-M1 GPIO Mapping

> **Warning:** Back-power hazard. Fit no carrier pull-ups on the DX-M1 GPIO pads. The DX-M1 I/O is powered only while the DX-M1 rails are up, and a carrier pull-up back-powers it while they are off.

2.5 Not Connected Pins

These pins carry an E1M-X™ standard function that is not implemented on the V2N-M1 module. They retain their standard name for cross-variant compatibility and must be left floating.

Pin Number	Pin Name	Description
A27	PCIE1_TX0_P	Leave floating.
A28	PCIE1_TX1_P	Leave floating.
A29	PCIE1_TX2_P	Leave floating.
A30	PCIE1_TX3_P	Leave floating.
A31	PCIE1_RX0_P	Leave floating.
A32	PCIE1_RX1_P	Leave floating.
A33	PCIE1_RX2_P	Leave floating.
A34	PCIE1_RX3_P	Leave floating.
A36	PCIE1_CLK_P	Leave floating.
A40	PCIE0_TX2_P	Leave floating.
A41	PCIE0_TX3_P	Leave floating.
A44	PCIE0_RX2_P	Leave floating.
A45	PCIE0_RX3_P	Leave floating.
A49	DSI1_C_P	Leave floating.

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Pin Number	Pin Name	Description
A50	DSI1_3_P	Leave floating.
A51	DSI1_2_P	Leave floating.
A52	DSI1_1_P	Leave floating.
A53	DSI1_0_P	Leave floating.
AA3	LCD_B23	Leave floating.
AB3	LCD_HSYNC	Leave floating.
AB63	CSI2_3_P	Leave floating.
AB64	CSI2_3_N	Leave floating.
AC3	LCD_VSYNC	Leave floating.
AC63	CSI2_2_P	Leave floating.
AC64	CSI2_2_N	Leave floating.
AD63	CSI2_C_P	Leave floating.
AD64	CSI2_C_N	Leave floating.
AE3	NC	Leave floating.
AE63	CSI2_1_P	Leave floating.
AE64	CSI2_1_N	Leave floating.
AF3	NC	Leave floating.
AF63	CSI2_0_P	Leave floating.
AF64	CSI2_0_N	Leave floating.
AG3	NC	Leave floating.
AH3	NC	Leave floating.
AH63	CSI3_3_P	Leave floating.
AH64	CSI3_3_N	Leave floating.
AI63	CSI3_2_P	Leave floating.
AI64	CSI3_2_N	Leave floating.
AJ3	NC	Leave floating.
AJ63	CSI3_C_P	Leave floating.
AJ64	CSI3_C_N	Leave floating.
AK63	CSI3_1_P	Leave floating.
AK64	CSI3_1_N	Leave floating.
AL63	CSI3_0_P	Leave floating.
AL64	CSI3_0_N	Leave floating.
AN1	ANT_6GHz	Leave floating.
AN3	NC	Leave floating.
AP1	ANT_5GHz	Leave floating.
AQ36	NC	Leave floating.
AQ37	NC	Leave floating.
AQ38	NC	Leave floating.
AQ39	NC	Leave floating.
AQ40	NC	Leave floating.
AQ41	NC	Leave floating.
AQ42	NC	Leave floating.
AQ43	NC	Leave floating.
AQ44	NC	Leave floating.

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Pin Number	Pin Name	Description
AQ45	NC	Leave floating.
AQ63	IO33	Leave floating.
AR36	NC	Leave floating.
AR37	NC	Leave floating.
AR38	NC	Leave floating.
AR39	NC	Leave floating.
AR40	NC	Leave floating.
AR41	NC	Leave floating.
AR42	NC	Leave floating.
AR43	NC	Leave floating.
AR44	NC	Leave floating.
AR45	NC	Leave floating.
B27	PCIE1_TX0_N	Leave floating.
B28	PCIE1_TX1_N	Leave floating.
B29	PCIE1_TX2_N	Leave floating.
B30	PCIE1_TX3_N	Leave floating.
B31	PCIE1_RX0_N	Leave floating.
B32	PCIE1_RX1_N	Leave floating.
B33	PCIE1_RX2_N	Leave floating.
B34	PCIE1_RX3_N	Leave floating.
B36	PCIE1_CLK_N	Leave floating.
B40	PCIE0_TX2_N	Leave floating.
B41	PCIE0_TX3_N	Leave floating.
B44	PCIE0_RX2_N	Leave floating.
B45	PCIE0_RX3_N	Leave floating.
B49	DSI1_C_N	Leave floating.
B50	DSI1_3_N	Leave floating.
B51	DSI1_2_N	Leave floating.
B52	DSI1_1_N	Leave floating.
B53	DSI1_0_N	Leave floating.
C2	USB0_30_VBUS	Leave floating.
C62	CAM_HSYNC	Leave floating.
D2	USB0_30_ID	Leave floating.
D3	LCD_B0	Leave floating.
D62	CAM_VSYNC	Leave floating.
D63	NC	Leave floating. Tied to 0V on the module in the current design (to be confirmed).
E3	LCD_B1	Leave floating.
E62	CAM_PCLK	Leave floating.
F3	LCD_B2	Leave floating.
F62	CAM_XVCLK	Leave floating.
G3	LCD_B3	Leave floating.
G62	CAM_D1	Leave floating.

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Pin Number	Pin Name	Description
H3	LCD_B4	Leave floating.
H62	CAM_D2	Leave floating.
I3	LCD_B5	Leave floating.
I62	CAM_D3	Leave floating.
J3	LCD_B6	Leave floating.
J62	CAM_D4	Leave floating.
K1	USB1_30_D_P	Leave floating.
K3	LCD_B7	Leave floating.
K62	CAM_D5	Leave floating.
L1	USB1_30_D_N	Leave floating.
L3	LCD_B8	Leave floating.
L62	CAM_D6	Leave floating.
M3	LCD_B9	Leave floating.
M62	CAM_D7	Leave floating.
N1	USB1_30_RX0_P	Leave floating.
N3	LCD_B10	Leave floating.
N62	CAM_D8	Leave floating.
O1	USB1_30_RX0_N	Leave floating.
O3	LCD_B11	Leave floating.
O62	CAM_D9	Leave floating.
P3	LCD_B12	Leave floating.
P62	CAM_D10	Leave floating.
Q1	USB1_30_TX0_P	Leave floating.
Q2	USB1_30_VBUS	Leave floating.
Q3	LCD_B13	Leave floating.
Q62	CAM_D11	Leave floating.
R1	USB1_30_TX0_N	Leave floating.
R2	USB1_30_ID	Leave floating.
R3	LCD_B14	Leave floating.
R62	CAM_D12	Leave floating.
S3	LCD_B15	Leave floating.
S62	CAM_D13	Leave floating.
T3	LCD_B16	Leave floating.
T62	CAM_D14	Leave floating.
U3	LCD_B17	Leave floating.
U62	CAM_D15	Leave floating.
V3	LCD_B18	Leave floating.
V62	CAM_D16	Leave floating.
W3	LCD_B19	Leave floating.
X3	LCD_B20	Leave floating.
Y3	LCD_B21	Leave floating.
Z3	LCD_B22	Leave floating.

Table 6 E1M-X V2N-M1 Not-connected Pins

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2.6 Reserved Pins

Pin Number	Pin Name	Description
W62, X62, Y62, Z62, AA62, AB62, AF62, AG62, AH62, AI62, AJ62, AK62	RSVD	Do not connect. Used for production purposes.
AE62, AL62, AM62, AN62, AO62, AP62, AQ62, AR62	RSVD	Not connected on the module. Do not connect.

Table 7 E1M-X V2N-M1 Reserved Pins

3 Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power-supply voltage	VDDIN to GND	- 0.3	6.0	V
Analog input voltage	V(ANA_Sx)	- 0.3	1.98	V
Digital IO (1V8)		- 0.3	1.98	V

Table 8 E1M-X V2N-M1 Absolute Maximum Ratings

Warning: Stresses beyond Absolute Maximum Ratings may cause permanent damage. Operation at these conditions is not implied.

3.2 Recommended Operating Conditions

The module is specified to meet the Electrical Characteristics in Section 3.3 over the conditions below. Operation outside this range is not guaranteed.

Parameter	Symbol	Min	Typ	Max	Unit
Module supply voltage	VDDIN	4.5	5.0	5.5	V
Ambient operating temperature	T_A	- 40	–	+85	°C
Relative humidity (operating, non-condensing)	RH	TBD	–	TBD	%

Table 9 E1M-X V2N-M1 Recommended Operating Conditions

3.3 Electrical Characteristics

Symbol	Description	Min	Nom	Max	Unit
Power supply					
VDDIN	Module power supply	4.5	5.0	5.5	V
I_{DDMAX}	Maximum I_{DD} current			TBD	
SD_VDD_OUT	SD-card supply (switched)		3.3		V
Analog inputs					
V(AINx)	Input voltage	0	–	1.8	V
Digital IOs					
V_{OL}	Low-level output voltage				

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Symbol	Description	Min	Nom	Max	Unit
V_{OH}	High-level output voltage				
V_{IL}	Low-level input voltage				
V_{IH}	High-level input voltage				
Camera LDOs					
+V_CAM0	CAM0 LDO output	0.6	–	3.3	V
+V_CAM1	CAM1 LDO output	0.6	–	3.3	V
+V_CAM2	CAM2 LDO output	0.6	–	3.3	V
+V_CAM3	CAM3 LDO output	0.6	–	3.3	V

Table 10 E1M-X V2N-M1 Electrical Characteristics

3.4 ESD & Latch-up Ratings

ESD ratings apply at module-level — i.e. directly to the LGA pads as exposed to a carrier-board assembly process. Customer ESD protection requirements on the carrier board are described in the relevant interface sub-sections.

Parameter	Standard	Min	Max	Unit
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001	–	TBD	V
Charged Device Model (CDM)	ANSI/ESDA/JEDEC JS-002	–	TBD	V
Latch-up	JESD78	–	TBD	mA

Table 11 E1M-X V2N-M1 ESD & Latch-up Ratings

3.5 Thermal Characteristics

The E1M-X V2N-M1 dissipates heat through both the Renesas RZ/V2N SoC and the on-module DeepX DX-M1 accelerator. Sustained AI workloads run both heat sources concurrently; an active heatsink or forced-air cooling is recommended above 50% DX-M1 utilisation at +25 °C ambient. Thermal-resistance figures below assume a 45 × 65 mm module mounted on a 4-layer FR4 carrier with a ground-plane heatsink.

Parameter	Symbol	Typ	Max	Unit
Thermal resistance, junction-to-ambient (RZ/V2N, still air)	$\theta_{JA,V2N}$	TBD	–	°C/W
Thermal resistance, junction-to-ambient (DX-M1, still air)	$\theta_{JA,M1}$	TBD	–	°C/W
Maximum junction temperature (RZ/V2N)	$T_{J,max,V2N}$	–	TBD	°C
Maximum junction temperature (DX-M1)	$T_{J,max,M1}$	–	TBD	°C
Power dissipation derating (above +85 °C)	P_D	TBD	–	mW/°C

Table 12 E1M-X V2N-M1 Thermal Characteristics

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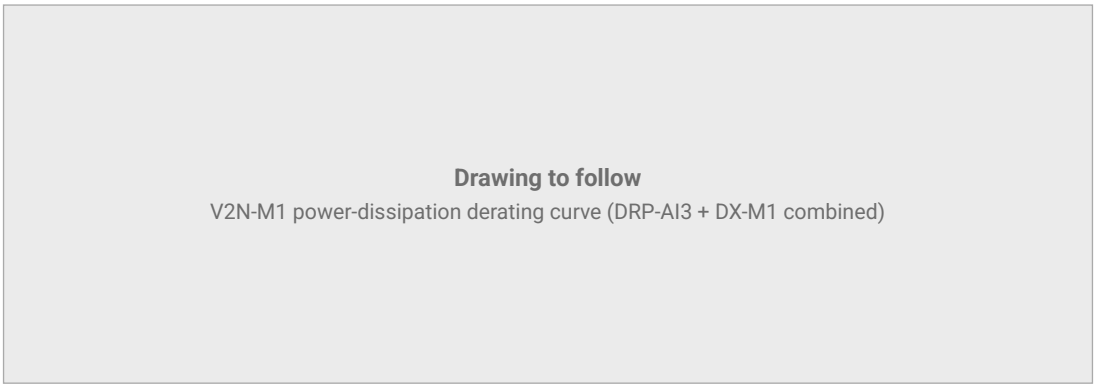


Figure 9 V2N-M1 power-dissipation derating curve (DRP-AI3 + DX-M1 combined)

4 Power

4.1 Power Architecture

All power rails on the module are generated and managed on-board from a single externally-supplied 5 V input on VDD_5V_IN. The carrier board supplies the 5 V input and does not need to sequence any power rails.

The module power tree is split into three domains:

- **Always-on domain**, alive whenever VDD_5V_IN is present, independent of MODULE_EN: an always-on 3.3 V LDO (+3V3_AON) and an always-on 1.8 V LDO (+1V8_AON, fed from +3V3_AON), the real-time clock (RV-3028-C7) with its backup input +S_CAP for a carrier-side backup store (see Section 4.2), and a programmable power controller. The power controller filters MODULE_EN (about 1 ms) and MODULE_STBY, holds the module power latch, drives the PMIC enable and PORn, sequences the DX-M1 rails on request from the RZ/V2N (Section 4.1.3), and wakes the module on the RTC interrupt, which also drives RTC_WAKE_N.
- **RZ/V2N domain**: an I^2C-controlled PMIC, which sequences the RZ/V2N rails once its enable is high and then releases PORn, together with a Renesas DA9292 dual buck converter and discrete bucks, LDOs and load switches. It is off while MODULE_EN is held low and after the firmware self-off. The GD32 I/O MCU (Cortex-M33 @ 216 MHz) enables the camera LDOs; it does not sequence the module rails.
- **DX-M1 domain**: the DeepX DX-M1 rails are not part of the RZ/V2N power-up sequence. The power controller sequences them later, on request from the RZ/V2N boot firmware (Section 4.1.3).

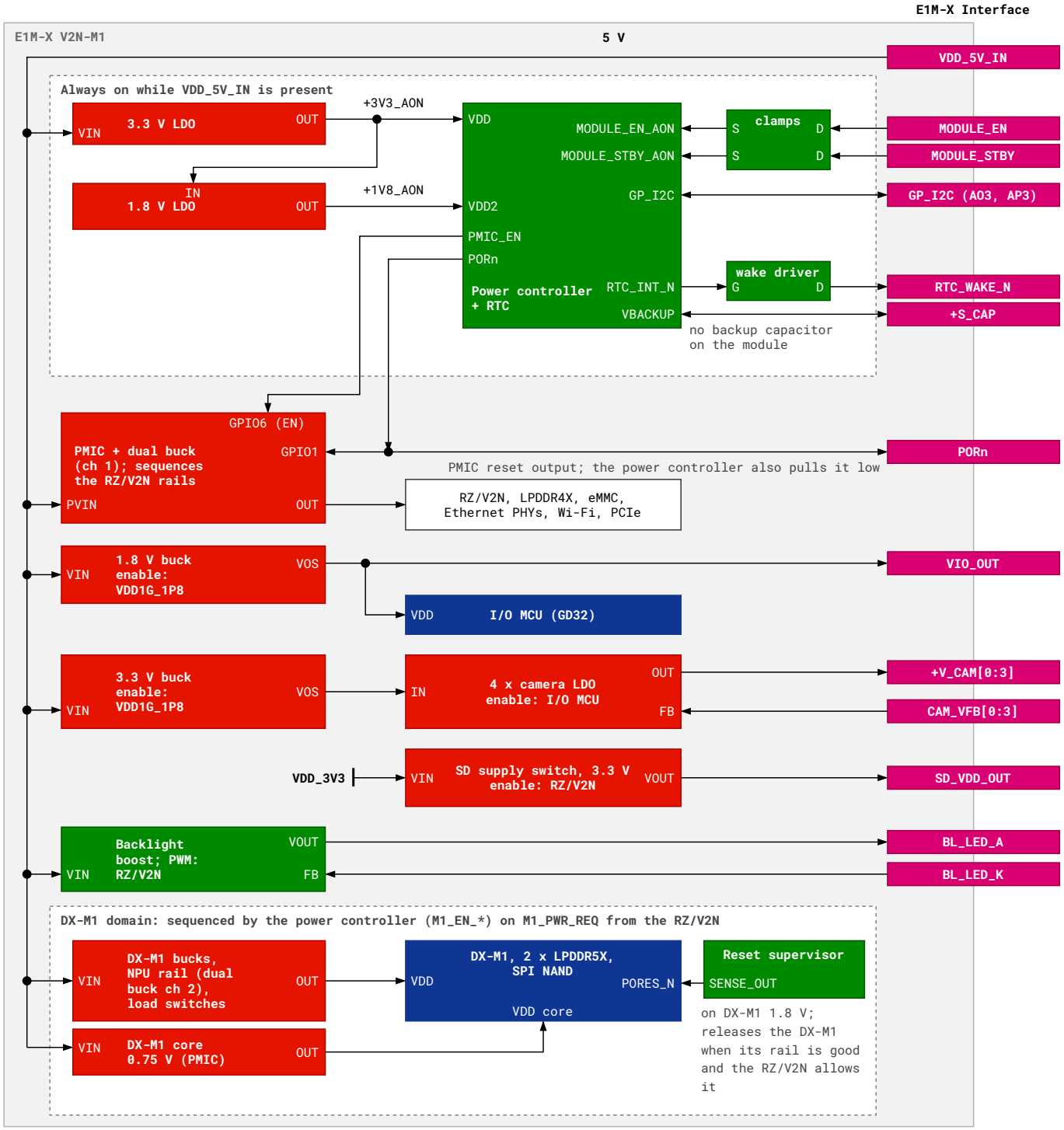
The E1M-X V2N-M1 includes all necessary decoupling capacitors. Additional decoupling capacitors on the carrier board may improve performance further.

The module exposes two regulated output rails to the carrier:

Rail	Pins	Voltage	Max current	Purpose
VIO_OUT	W1, W2	1.8 V ± 5%	TBD mA	I/O reference for carrier-side level shifters.
SD_VDD_OUT	AQ30	3.3 V	300 mA	microSD slot supply, switched by the RZ/V2N. The SD signalling level (3.3 V or 1.8 V) is switched on the module; this rail stays at 3.3 V.

Table 13 Module Output Rails

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Single 5 V input; no carrier-side rail sequencing. +3V3_AON, +1V8_AON, the power controller and the RTC run whenever VDD_5V_IN is present. The power controller is the only driver of the PMIC enable; it also pulls PORn low at power-off and sequences the DX-M1 rails on request from the RZ/V2N. Clamps: on-module MODULE_EN / MODULE_STBY clamps. Wake driver: RTC_WAKE_N open-drain driver. RTC backup only from the carrier +S_CAP.

Figure 10 E1M-X V2N-M1 Power Architecture

4.1.1 Power Controller and RTC

The programmable power controller is fitted in every variant. It is the power latch, the self-off and wake logic and the DX-M1 / LPDDR5 power sequencer, and it is the only driver of the PMIC enable: a module without a programmed power controller never starts. One power-controller image, `v2n_ctl_v1`, serves all E1M-X V2N and V2N-M1 variants; it is not interchangeable with any E1M-AEN image. It runs from both always-on rails (+3V3_AON and +1V8_AON). The timings in this section are design values of the `v2n_ctl_v1` image; bench validation is pending.

The RTC (RV-3028-C7) runs from +3V3_AON and sits on GP_I2C at address 0x52, beside the power controller at 0x08 (Section 8.4.2). Its 32 kHz clock output is buffered on the module to RTC_CLKOUT (AQ16). Its interrupt RTC_INT_N (100 kΩ pull-up to +3V3_AON on the module) is a level-sensitive wake input of the power controller, and it drives RTC_WAKE_N (AD3) on the module (Section 6.1). The power controller signals wake and standby events on RTC_ALARM, an open-drain line read by the RZ/V2N (PA7) and by the GD32 (PC14).

Behaviour of the v2n_ctl_v1 image:

- **On:** MODULE_EN released (or an RTC / MODULE_STBY wake event) sets the latch; the PMIC enable rises at once, and the PMIC releases PORn when its rails are up.
- **Off:** MODULE_EN held low (Section 6.1), or the firmware self-off (Section 4.1.2). PORn goes low about 2 ms after the latch clears, the DX-M1 sequence unwinds, and the PMIC enable falls about 50 ms after the latch clears. The next start is locked out for about 145–158 ms.
- **Self-off refusal in hardware:** an OFF request is refused while RTC_INT_N is low or MODULE_STBY is asserted, so an event is never lost.
- **Blank or unprogrammed power controller:** all its outputs are high-impedance; on-module pull-downs hold the PMIC enable and every DX-M1 enable low, so the module stays off.

4.1.2 Firmware Self-Off and Power-Controller Access

The firmware powers the module off with two writes to power-controller register 0x7A: OFF_ARM, then OFF. Write 0x7A = 0x00 on every boot before the first use of the power controller: a wake from self-off is not a power-controller power-on reset. The register bit positions are released together with the v2n_ctl_v1 image.

Only the RZ/V2N may address the power controller, the RTC and the PMICs. The on-module GD32 can reach BRD_I2C but must not address them. The power controller is programmed over GP_I2C (AO3 / AP3) at provisioning, with MODULE_EN held low; a new image takes effect after the next 5 V cycle.

> **Warning:** Never set the power controller's lock bit, never issue its soft reset, and never write its NVM or register 0xC7 from the application. Each of these takes every power-controller output high-impedance: the module powers off uncontrolled, and every DX-M1 rail is cut at once (an uncontrolled LPDDR5 power-off).

4.1.3 DX-M1 Power Sequencing

The DX-M1's internal power rails (LPDDR5X, NPU core, SPI NAND) are entirely on-module and not exposed to the carrier. They are not brought up at VDD_5V_IN power-up: the RZ/V2N boot firmware requests them on M1_PWR_REQ, and the power controller sequences them. The power controller acts on the request only with PORn released and LPDDR_1V8 good. Power-up order:

1. M1_EN_CORE (DX-M1 core rail request to the PMIC).
2. M1_EN_NPU, when the core rail is good.
3. M1_EN_IO (VDD1, M1_VDD_1V8), 3.8–6.3 ms later.
4. M1_EN_VDD2H, 3.8–4.2 ms later.
5. M1_EN_VDDQ, when VDD2H is good.

The firmware releases the DX-M1 reset only after the power-controller status register shows VDDQ on, plus 4 ms. Power-down runs in reverse order (VDDQ, VDD2H, VDD1, then NPU and core together), 27.7–33.2 ms in total, and finishes inside the PMIC-enable delay. These timings are design values of the v2n_ctl_v1 image.

> **Warning:** Hardware-damage hazard. Do not drive the DX-M1 power sequence or the DX-M1 reset from anywhere other than the Alp Lab boot firmware (not from a Cortex-M33 image, a Linux application or a bench tool). A second, uncoordinated PMIC writer can damage the DX-M1. Release the DX-M1 reset only after the power-controller status register shows VDDQ on, plus 4 ms. A replacement boot loader must request the rails on M1_PWR_REQ and follow the reset rule above.

> **Warning:** Hardware-damage hazard. The DX-M1 reference-clock input is driven from the clock generator DIFF1 output through the reference-clock buffer, which has no output enable. Enable DIFF1 (clock generator, I^2C 0x69) only while the DX-

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M1 rails are up; otherwise the buffer drives the unpowered DX-M1 input. The carrier PCIE0 slot therefore has a reference clock only while the DX-M1 is powered (Section 8.3).

4.2 RTC Backup

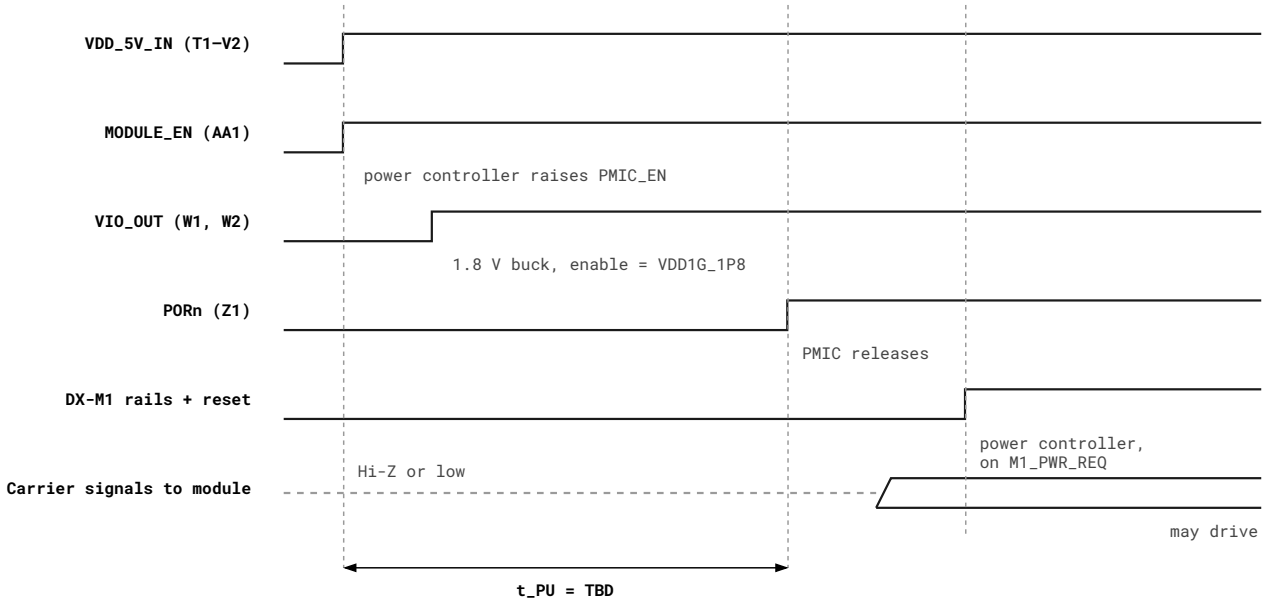
The real-time clock runs from the module's always-on 3.3 V rail whenever 5 V is present. Without 5 V it is backed only by what the carrier connects to +S_CAP (AQ25, net VBAT). +S_CAP is connected directly to the RTC backup input; the module has no backup capacitor of its own. Connect the carrier backup super-capacitor here.

Warning: With a non-rechargeable backup cell on +S_CAP, firmware must keep the RTC trickle charger disabled.

4.3 Power-Up & Reset Sequence

The on-module PMIC sequences the internal rails; no carrier-side rail sequencing is required. The recommended carrier-side control-signal bring-up order is:

1. Apply 5 V to VDD_5V_IN.
2. Release MODULE_EN (the on-module front end needs no carrier pull-up).
3. Release PORn (no carrier pull-up).
4. Wait for the on-module power-up to complete. Internal rails stabilise within TBD ms of MODULE_EN release; the DX-M1 subsystem is powered later by the power controller on request from the RZ/V2N boot firmware and needs no carrier action. The module exposes no ready-strobe output, so allow this fixed delay before driving signals into the module.
5. Begin communication with the module.



Not to scale. BOOT0–BOOT3 are sampled at the rising edge of PORn. The DX-M1 rails are sequenced by the power controller on request (M1_PWR_REQ) from the RZ/V2N boot firmware, which releases the DX-M1 reset after VDDQ on plus 4 ms.

Figure 11 V2N-M1 Power-Up Timing (module level, not to scale)

Warning: For power-down, hold MODULE_EN low for at least 150 ms before removing VDD_5V_IN. Removing 5 V with the module on is for recovery only.

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4.4 Power Consumption

Numbers below are typical at T_A = +25 °C, VDDIN = 5.0 V. The DX-M1 baseline draw (from the time the RZ/V2N boot firmware requests the DX-M1 rails) is the main delta vs the V2N family.

Mode	Description	Min	Typ	Max	Unit
Active					
A55 quad + DRP-AI3 + DX-M1 @ full load	Combined AI inference at 29 TOPS	–	TBD	TBD	mA
A55 quad + DX-M1 only	Single-NPU offload	–	TBD	TBD	mA
A55 quad + DRP-AI3 only (DX-M1 idle)	V2N-equivalent workload	–	TBD	TBD	mA
A55 quad @ 1.8 GHz, no AI	General Linux compute	–	TBD	TBD	mA
Active, with dual Ethernet + PCIe SSD + display + camera	Full-feature workload	–	TBD	TBD	mA
Low-power					
Idle (DX-M1 in reset)	Cores halted, M1 gated	–	TBD	–	mA
Sleep	Retention only, RTC running	–	TBD	–	µA
Shutdown (MODULE_EN low)	Module disabled	–	TBD	–	µA

Table 14 E1M-X V2N-M1 Power Consumption (typical)

4.5 Boot Settings

E1M-X V2N-M1 supports several boot options selected by the BOOT0–BOOT3 strap pins on the carrier.

BOOT1	BOOT0	Boot mode	Device	CA55 boot	CM33 boot
0	0	Mode 0	eSD (3.3 V for execution)	Supported	Not supported
0	1	Mode 1	eMMC (I/O voltage 1.8 V)	Supported	Not supported
1	0	Mode 2	QSPI NOR (I/O voltage 1.8 V)	Supported	Supported
1	1	Mode 3	SCIF download	Supported	Supported

Table 15 E1M-X V2N-M1 Boot Options

> **Note:** BOOT2 is fixed at 1. Each strap takes a 1 kΩ pull-up to VIO_OUT for 1 or a 1 kΩ pull-down to GND for 0; an open strap reads 1 (RZ/V2N internal pull-up), but do not rely on it.

5 Boot Modes

The Renesas RZ/V2N samples the four boot-strap pins (BOOT0–BOOT3) at the rising edge of PORn. BOOT0/BOOT1 select the boot source; BOOT2 is fixed at 1 on the V2N family; BOOT3 selects the boot CPU (high = CA55, low = CM33). See Section 4.5 for the full mapping.

Strap every boot pin (BOOT0–BOOT3) on the carrier with a 1 kΩ resistor: a 1 kΩ pull-up to VIO_OUT for 1, a 1 kΩ pull-down to GND for 0. The RZ/V2N has internal pull-ups on its boot-strap pins, so a strap left open reads 1, but a carrier design must not rely on them.

The carrier-board **MUST** drive BOOT0/BOOT1 (typically via a 2-position DIP switch to VIO_OUT with 1 kΩ pull-downs to GND: closed = 1, open = 0), or hard-strap them with 1 kΩ resistors. BOOT2 (X1) has no pull-up on the module, so the carrier fits a 1 kΩ pull-up to VIO_OUT (fixed at 1). BOOT3 (Y1) is also connected on the module, through an on-module 0 Ω link, to GPIO5 of the PMIC, which is an input (Hi-Z) and does not drive it, and to pad AI3 (PMIC_GPIO5_10V); see the hardware-damage warning in Section 2.1. For Cortex-A55 boot, the carrier pulls Y1 up to VIO_OUT with a 1 kΩ resistor; for Cortex-M33 boot it pulls Y1 down to GND with 1 kΩ.

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5.1 DX-M1 Boot Straps

The DeepX DX-M1 is not affected by the BOOT* pins. Its boot straps M1_BOOT0–M1_BOOT2 are on pads AK3, AL3 and AM3. Each has a 10 kΩ pull-down fitted on the module, so all three read 0 by default; the 10 kΩ pull-up positions to M1_VDD_1V8 are not fitted. Leave the pads floating for the default.

Pad	Net	DX-M1 pin	Pull-down (fitted)	Pull-up to M1_VDD_1V8	Default
AK3	M1_BOOT0	GPIO00_00	10 kΩ	10 kΩ, not fitted	0
AL3	M1_BOOT1	GPIO00_01	10 kΩ	10 kΩ, not fitted	0
AM3	M1_BOOT2	GPIO00_02	10 kΩ	10 kΩ, not fitted	0

Table 16 DX-M1 Boot Straps

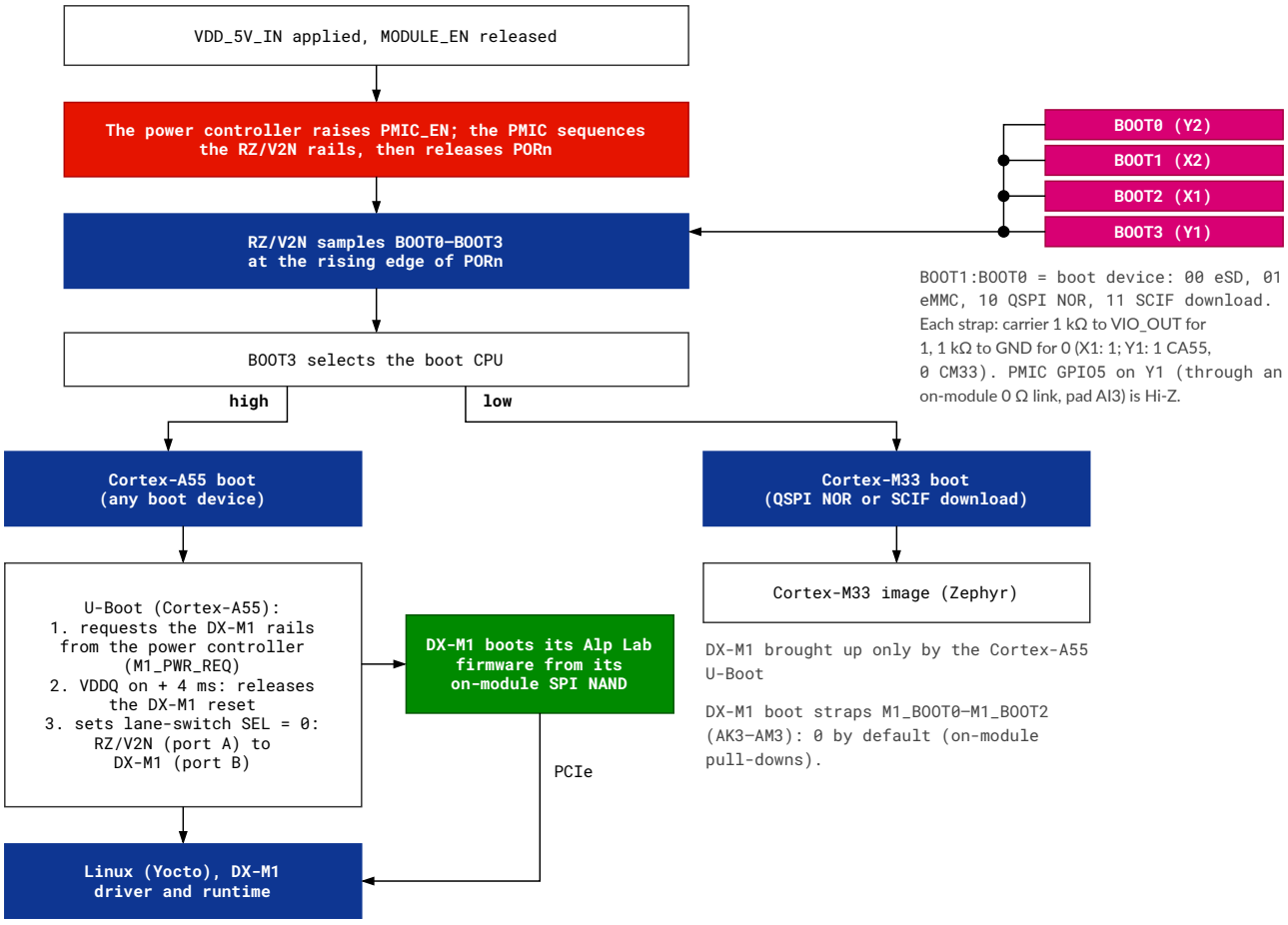
Warning: Back-power hazard. A carrier pull-up on M1_BOOT0–M1_BOOT2 must come from a rail that is off whenever M1_VDD_1V8 is off; otherwise the DX-M1 I/O is back-powered through the pull-up.

The DX-M1 is held in reset until the RZ/V2N boot firmware (U-Boot, on the Cortex-A55) has requested its rails from the power controller and the power-controller status register shows VDDQ on, plus 4 ms (Section 4.1.3); the firmware then releases the DX-M1 reset, and the DX-M1 boots its own firmware from its on-module SPI NAND.

Warning: The DX-M1 firmware is an Alp Lab build for this SoM, provisioned at the factory. Do **not** update it with stock DEEPX firmware: that leaves the NPUs dead (`dxrt_polling_ack: timeout`), and recovery needs the DX-M1 boot straps M1_BOOT0–M1_BOOT2 on pads AK3–AM3 (Section 5.1) set from the carrier to a non-default value; contact Alp Lab for the recovery procedure. The shipped `dxrt-cli` warns before its firmware-update (`-u`), firmware-upload (`-w`) and firmware-config (`-C`) options but does not block them; use them only with firmware supplied by Alp Lab for this module.

Note: For details on the secure-boot signing flow, see **AN-010: Secure Boot and Code Signing**. For the DX-M1 first-inference walkthrough see **AN-009: DeepX DX-M1 First Inference**.

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Use only Alp Lab DX-M1 firmware: stock DEEPX firmware leaves the NPUs dead. A custom boot loader must request the DX-M1 rails on M1_PWR_REQ and release the DX-M1 reset only after VDDQ on plus 4 ms (see the hardware-damage warning in DX-M1 Power Sequencing). Boot straps: an open strap reads 1 (RZ/V2N internal pull-up); the carrier sets every strap with its own 1 kΩ resistor.

Figure 12 E1M-X V2N-M1 Boot Flow

6 Reset, Module Enable & Power Control

The carrier controls the module with VDD_5V_IN, MODULE_EN and MODULE_STBY, and reads its state on PORn and RTC_WAKE_N. All other power sequencing is inside the module (Section 4.1). The E1M-X V2N-M1 exposes the same control signals as V2N. Asserting PORn resets **both** the RZ/V2N and the on-module DX-M1. Releasing the DX-M1 from reset afterwards is done by the RZ/V2N boot firmware (U-Boot in the Alp SDK™ Yocto image); application software does not manage it.

6.1 Control Pins

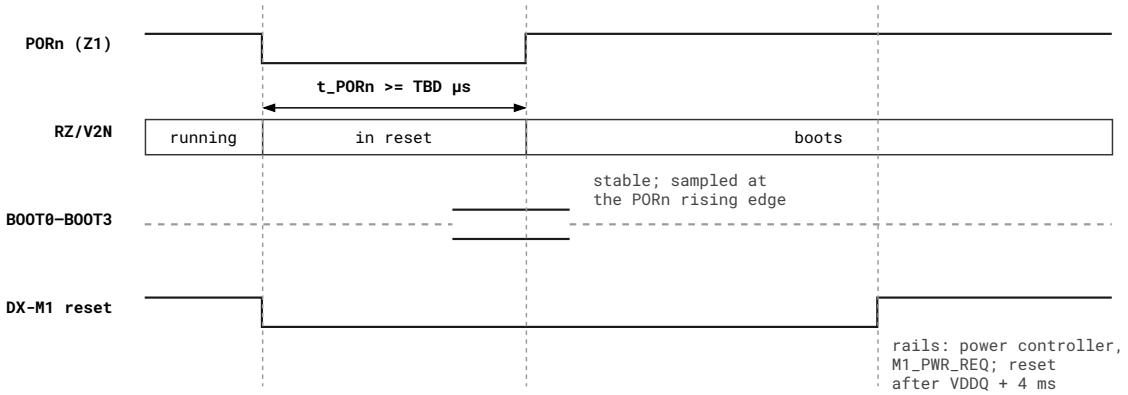
MODULE_EN (AA1) and MODULE_STBY (AB1) reach the power controller (Section 4.1.1) through on-module clamps, with 1 MΩ pull-ups to the 1.8 V always-on rail (+1V8_AON) behind the clamps. The carrier may drive them with an open-drain output and no pull-up, a switch to GND, or push-pull logic from 1.8 V to 5 V. Released, the pad sits at about 1.2–1.5 V (estimate). Keep the carrier leakage on each pad at ≤ 0.1 µA, including ESD parts. The timings below are design values of the v2n_ctl_v1 power-controller image.

Pin	Direction	Description
MODULE_EN (AA1)	Input, 1.8–5 V tolerant	Module enable. Released (or high): the module powers on. Low ≤ 0.5 ms: ignored. Low ≥ 4 ms: resets the RZ/V2N and the DX-M1 with the rails kept up. Low ≥ 55 ms: powers the module off (both V2N and DX-M1). Leave floating if unused.

Pin	Direction	Description
MODULE_STBY (AB1)	Input, 1.8–5 V tolerant	Stand-by / wake request, pulse-only. A low pulse ≥ 2 ms is a request to the firmware while the module is on (signalled on RTC_ALARM), and wakes the module from self-off. Held low, it blocks the self-off. Leave floating if unused.
PORn (Z1)	Bidirectional, open drain, 1.8 V	Power-on reset: the PMIC reset output (10 kΩ pull-up to VDD1G_1P8 on the module), also pulled low by the power controller at power-off. The carrier may pull it low to reset the RZ/V2N with the rails kept up. No carrier pull-up. Minimum low-pulse width: TBD µs.
RTC_WAKE_N (AD3)	Output, open drain	Active-low RTC wake: the RTC interrupt RTC_INT_N is inverted on the module onto RTC_WAKE (10 MΩ pull-up to +3V3_AON), and an on-module open-drain transistor drives AD3. Valid in every module state while 5 V is present. Carrier pull-up to its always-on rail, ≤ 5.5 V, ≥ 10 kΩ.

Table 17 Reset, Enable & Power-control Signals

Warning: Hold MODULE_EN low for at least 150 ms before removing VDD_5V_IN. Removing 5 V with the module on is for recovery only.



Not to scale. Pulling PORn low resets the RZ/V2N; its M1_PWR_REQ and DX-M1 reset outputs fall to their on-module pull-downs, so the DX-M1 stays in reset until the boot firmware requests its rails from the power controller again. PORn is a PMIC output, also pulled low by the power controller at power-off: it does not reset the PMIC.

Figure 13 V2N-M1 Reset Timing (PORn, not to scale)

7 JTAG / SWD Debug

The E1M-X V2N-M1 exposes a 5-pin JTAG / SWD interface for programming and debug of the RZ/V2N. Signals operate at 1.8 V; carrier-board level shifters are required for 3.3 V debug probes. The DeepX DX-M1's debug interface is **not** exposed to the carrier — it is brought up by the RZ/V2N boot firmware and is software-debuggable from the RZ/V2N host over PCIe.

Pin	Signal	Description
AL1	JTAG_nRST	Active-low reset to the SoC debug logic.
AJ1	JTAG_TCK / SWDCLK	Test clock (JTAG) or serial-wire clock (SWD).
AJ2	JTAG_TDI	Test data in (JTAG only).
AK2	JTAG_TDO	Test data out (JTAG only).

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Pin	Signal	Description
AK1	JTAG_TMS / SWDIO	Test mode select (JTAG) or serial-wire I/O (SWD).

Table 18 JTAG / SWD Pinout

Note: Alp Lab recommends exposing the JTAG/SWD pins on a 10-pin Cortex-M debug header on the carrier board. Refer to **UG-E1M-X-001** §5.1 for the reference connector pinout.

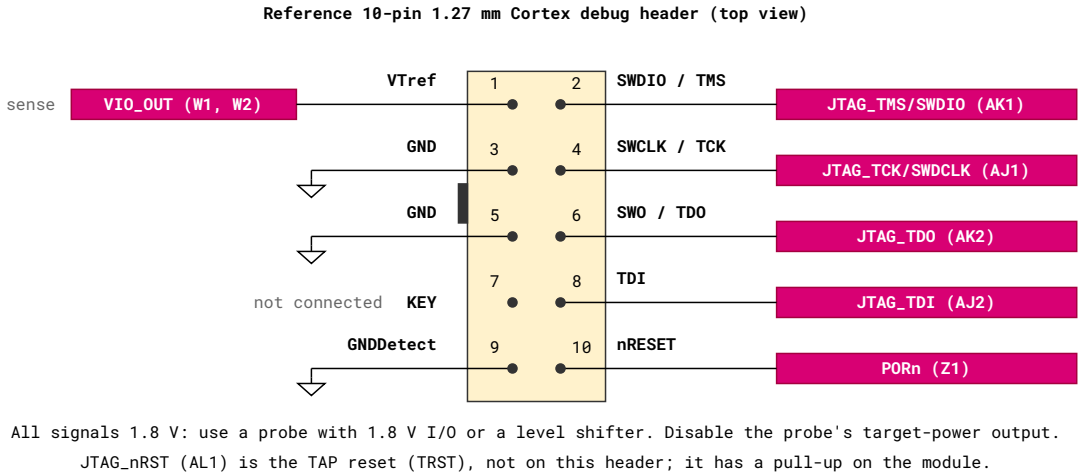


Figure 14 Reference JTAG / SWD Header Pinout

8 Interfaces

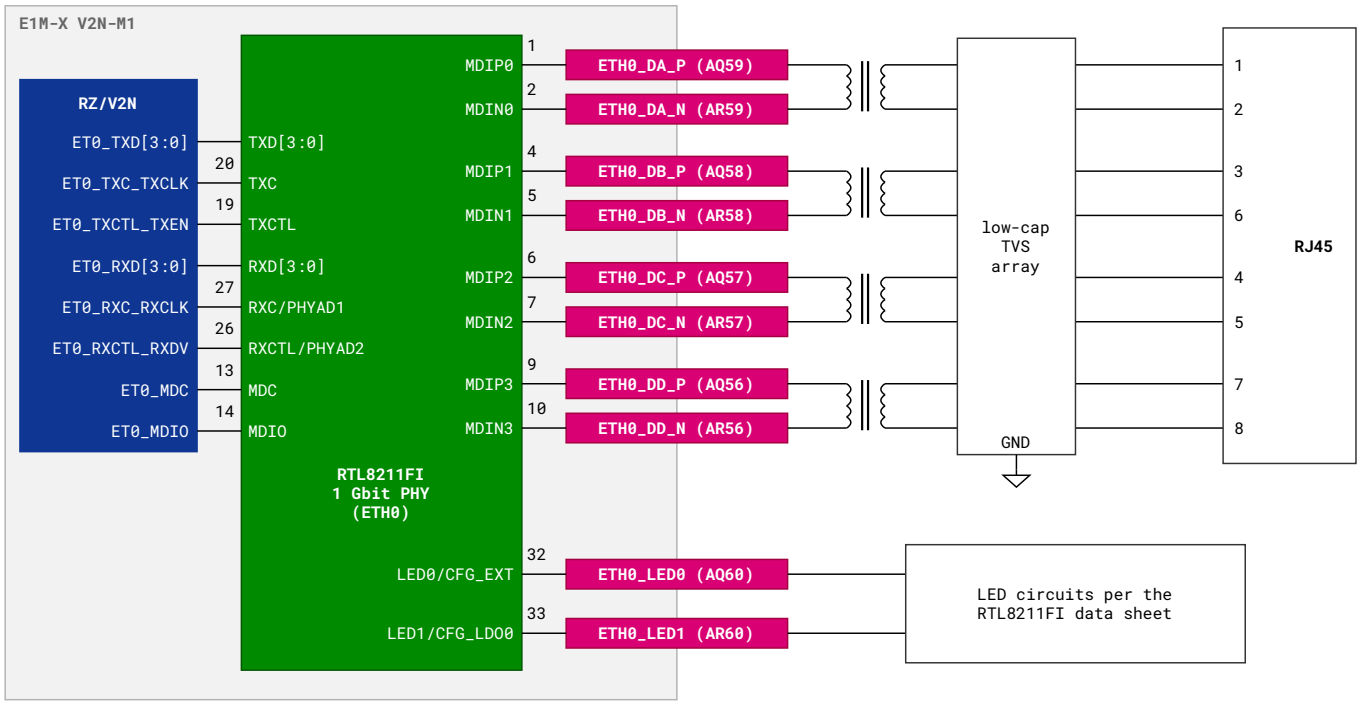
The E1M-X offers a wide set of interfaces to accommodate diverse system requirements:

- General-purpose digital I/O (GPIO)
- I^2C, I^3C, SPI, and UART serial buses
- USB 2.0 / 3.2 Gen 2 ports
- CAN FD (Flexible Data-rate)
- PCI Express Gen 3
- MIPI CSI and DSI for camera and display connectivity
- Dual Gigabit Ethernet with IEEE 1588 support

8.1 Ethernet

E1M-X V2N-M1 has two 1 Gbit Ethernet PHYs: the Realtek RTL8211FI-VD-CG. The interfaces do not include on-module EMI or ESD protection; the user must provide external magnetics transformers, connectors, and EMI/ESD protection on the carrier board.

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MDI pairs: 100 Ω differential; transformer centre taps per the magnetics and RTL8211FI data sheets. ETH0_LED0 / ETH0_LED1 are PHY strap pins (module: LED0 4.7 kΩ to the PHY 3.3 V supply, LED1 4.7 kΩ to GND): the LED circuits must keep these levels at reset.
ETH1 is identical: DA AQ52 / AR52, DB AQ51 / AR51, DC AQ50 / AR50, DD AQ49 / AR49, LED0 AQ53, LED1 AR53 (P / N).

Figure 15 E1M-X V2N-M1 Ethernet PHY Connection (ETH0; ETH1 identical)

8.2 USB

E1M-X V2N-M1 has one USB 2.0 and one USB 3.2 Gen 2 interface. USB 2.0 supports Host/Function; USB 3.2 is Host-only.

Pin Number	Pin Name	Peripheral	Description
C1	USB0_30_D_N	USB0	Route USB_N and USB_P as a differential pair with 90 Ω impedance.
B1	USB0_30_D_P		
F1	USB0_30_RX0_N		
E1	USB0_30_RX0_P		
I1	USB0_30_TX0_N		
H1	USB0_30_TX0_P		
G2	USB2_20_ID	USB2	Low: Host mode. NC: Device mode.
J2	USB2_20_N		Route USB_N and USB_P as a differential pair with 90 Ω impedance.
I2	USB2_20_P		
F2	USB2_20_VBUS		Connect to USB VBUS 5 V.

Table 19 E1M-X V2N-M1 USB Interface

8.3 PCIe

Renesas RZ/V2N has one PCIe® Gen3 2-lane interface. The PCIe interface is used to communicate with the standalone AI accelerator DeepX-M1 to sustain AI-computation performance. However, to increase user flexibility, the PCIe interface is multiplexed to work either with DeepX-M1 or exit the module for external connections.

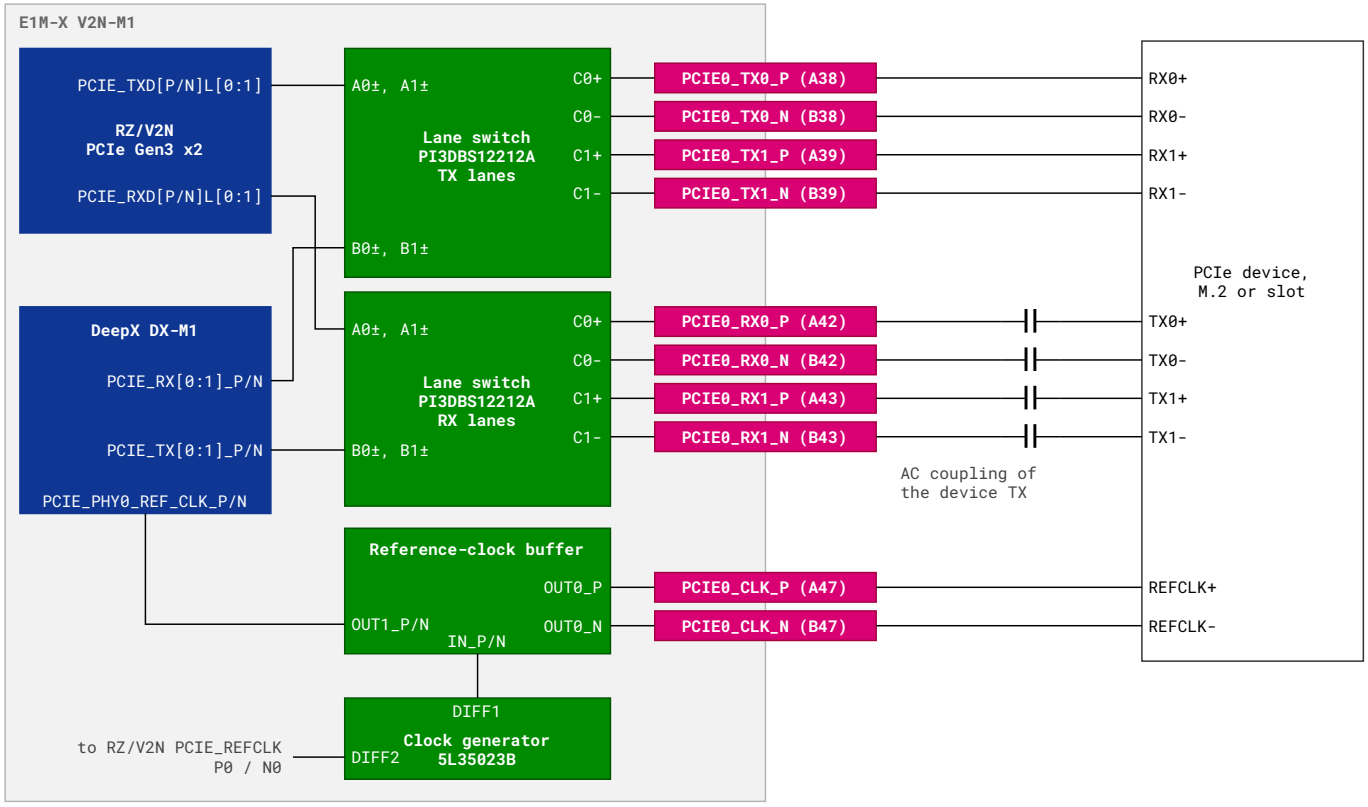
The multiplexer is two Diodes PI3DBS12212A 2:1 PCIe lane switches: one carries the two TX lanes and the other the two RX lanes. On both, port A (the common port) connects to the RZ/V2N, port B to the DX-M1 and port C to the PCIE0 pads. SEL = 0 links port A to port B (RZ/V2N to DX-M1); SEL = 1 links port A to port C (RZ/V2N to the PCIE0 pads), which disconnects the DX-

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M1. PD = 1 powers both switches down. The RZ/V2N drives SEL and PD (PCIe.MUX_SEL on P95, PCIe.MUX_PD on P80) through a level translator; in the Alp SDK™ Yocto image, U-Boot selects the DX-M1 (SEL = 0).

The PCIe reference clocks come from the on-module clock generator (5L35023B). DIFF2 drives the RZ/V2N PCIE_REFCLKP0 / PCIE_REFCLKN0 through 33 Ω series resistors. DIFF1 drives the SY75602 1:2 reference-clock buffer through 33 Ω series resistors: buffer OUT0 drives the PCIE0_CLK_P / PCIE0_CLK_N pads (A47 / B47), and OUT1 drives the DX-M1 PCIE_PHY0_REF_CLK_P / _N. The carrier PCIe device and the DX-M1 therefore share one clock output (DIFF1), and the RZ/V2N root complex uses DIFF2 of the same PLL: the link runs with a common clock. The carrier must not add a second reference-clock source for a device on PCIE0; clock it from PCIE0_CLK.

The reference-clock buffer has no output enable. The firmware enables DIFF1 only while the DX-M1 rails are up, so on the V2N-M1 the carrier PCIE0 slot has a reference clock only while the DX-M1 is powered (see the hardware-damage warning in Section 4.1.3).



Module TX lanes are AC-coupled on the module; module RX lanes are not. PCIE0_CLK is a reference-clock output. No PERST#, CLKREQ# or WAKE# pad on the module. Port A (RZ/V2N) is the common port of the two lane switches: SEL = 0 links it to the DX-M1 (port B), SEL = 1 to the PCIE0 pads (port C), which disconnects the DX-M1. The RZ/V2N drives SEL and PD (PCIe.MUX_SEL, PCIe.MUX_PD) through a level translator. U-Boot selects the DX-M1 (SEL = 0). PD = 1 powers both lane switches down. Reference clock: the clock-generator DIFF1 drives the reference-clock buffer; OUT0 drives PCIE0_CLK and OUT1 the DX-M1 (one shared output), and the RZ/V2N uses DIFF2 of the same PLL (common clock). DIFF1 runs only while the DX-M1 rails are up; the carrier adds no second reference clock.

Figure 16 E1M-X V2N-M1 PCIe MUX Connection

8.4 Serial Interfaces

8.4.1 I²C

E1M-X has four I²C interfaces. Refer to the Renesas RZ/V2N series datasheet for full details. External pull-ups are required.

> **Note:** The I2C3 interface is connected to the secondary MCU on E1M-X. It is handled by the Alp SDK™ from the main MPU.

8.4.2 On-Module I²C Buses

Two I²C buses serve the on-module devices:

- GP_I2C (3.3 V, always on, pads AO3 / AP3): 4.7 kΩ pull-ups to +3V3_AON on the module. While the module runs, on-module bus switches (gated by VDD1G_1P8) bridge it onto BRD_I2C.
- BRD_I2C (1.8 V, on-module only): the RZ/V2N board bus. It also carries the PMIC, and the GP_I2C devices through the bus switches.

Bus	Device	Address
GP_I2C	Power controller	0x08
GP_I2C	RTC RV-3028-C7	0x52
BRD_I2C	DA9292 dual buck	0x1E
BRD_I2C	TPS628640 buck (LPDDR5 VDD2H, DDR5_VDD2H_1V05)	0x44
BRD_I2C	TPS628640 buck (LPDDR5 VDDQ, DDR5_VDDQ_0V5)	0x4F
BRD_I2C	TPS628640 buck (VDD0V85_LPDDR)	0x48
BRD_I2C	Clock generator 5L35023B	0x69
BRD_I2C	Secure element OPTIGA™ Trust M	0x30
BRD_I2C	Temperature sensor TMP112	0x40
BRD_I2C	I/O MCU GD32	0x70

Table 20 On-Module I²C Devices (7-bit addresses)

Through the bus switches, 0x08 and 0x52 are also present on BRD_I2C while the module runs. Only the RZ/V2N may address the power controller, the RTC and the PMICs; the on-module GD32 can reach BRD_I2C but must not address them.

> **Warning:** GP_I2C (AO3 / AP3): the carrier fits no pull-ups and keeps both pads high-impedance whenever module 5 V is absent.

8.4.3 I³C

E1M-X has one I³C interface. Refer to the Renesas RZ/V2N series datasheet for full details. External pull-ups are required.

8.4.4 UART

E1M-X has two UART interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.5 SPI

E1M-X has three SPI interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.6 I²S

E1M-X has two I²S interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.7 CAN Bus

E1M-X includes two optional CAN-BUS PHYs to simplify carrier-board hardware design. When the internal PHY is used, the user must add termination, ESD, and EMI protection components on the carrier board.

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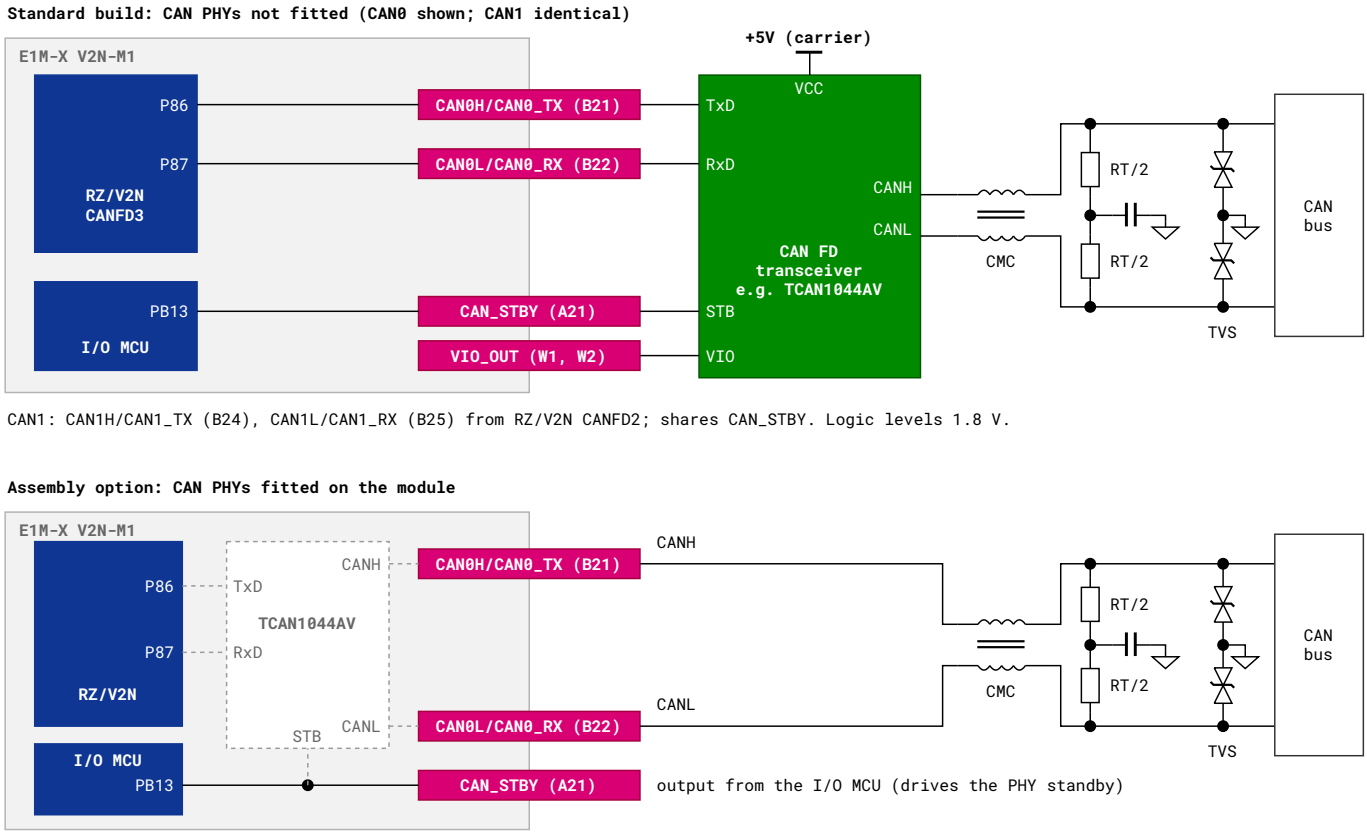
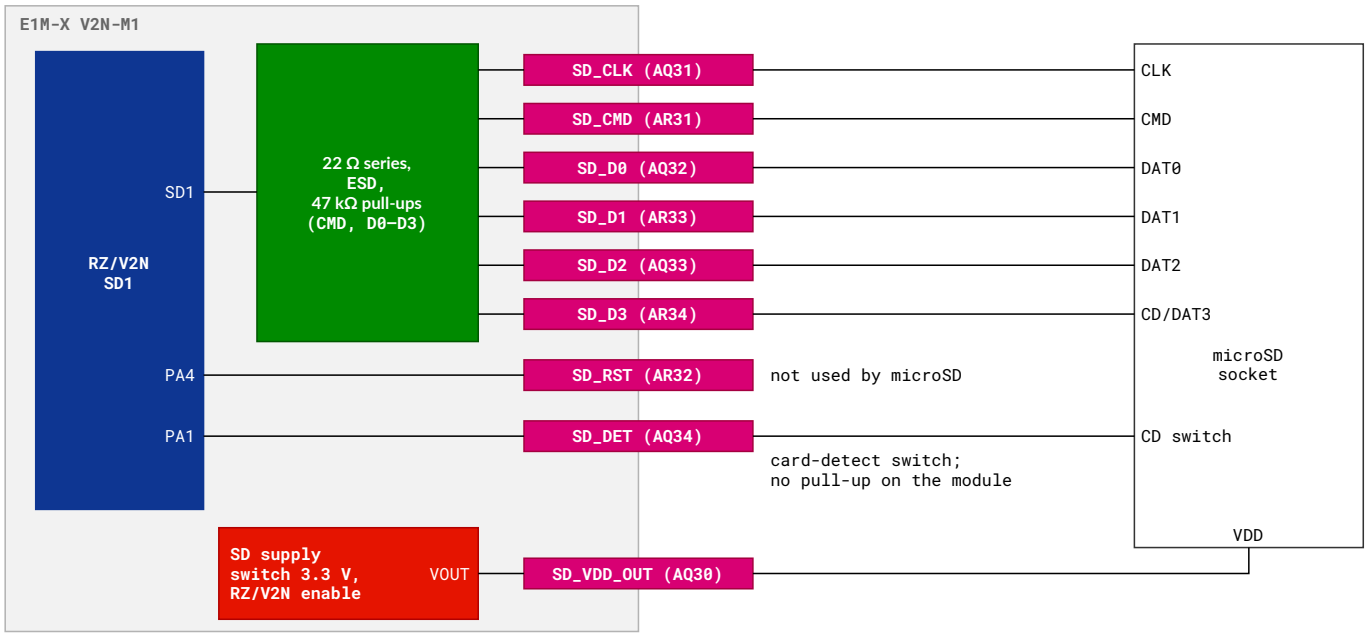


Figure 17 E1M-X V2N-M1 CAN-BUS Connection: Standard Build and CAN PHY Assembly Option

8.5 SD Card

E1M-X supports an external µ SD card over the SDIO interface. The SDIO lines have ESD protection and 22 Ω series resistors on the module, plus 47 kΩ pull-ups on SD_CMD and SD_D0–SD_D3 to the SD I/O supply. SD-card power (3.3 V) is supplied by E1M-X via SD_VDD_OUT, switched by the RZ/V2N; the module switches the SD signalling between 3.3 V and 1.8 V for the high-speed modes. SD_DET has no pull-up on the module.

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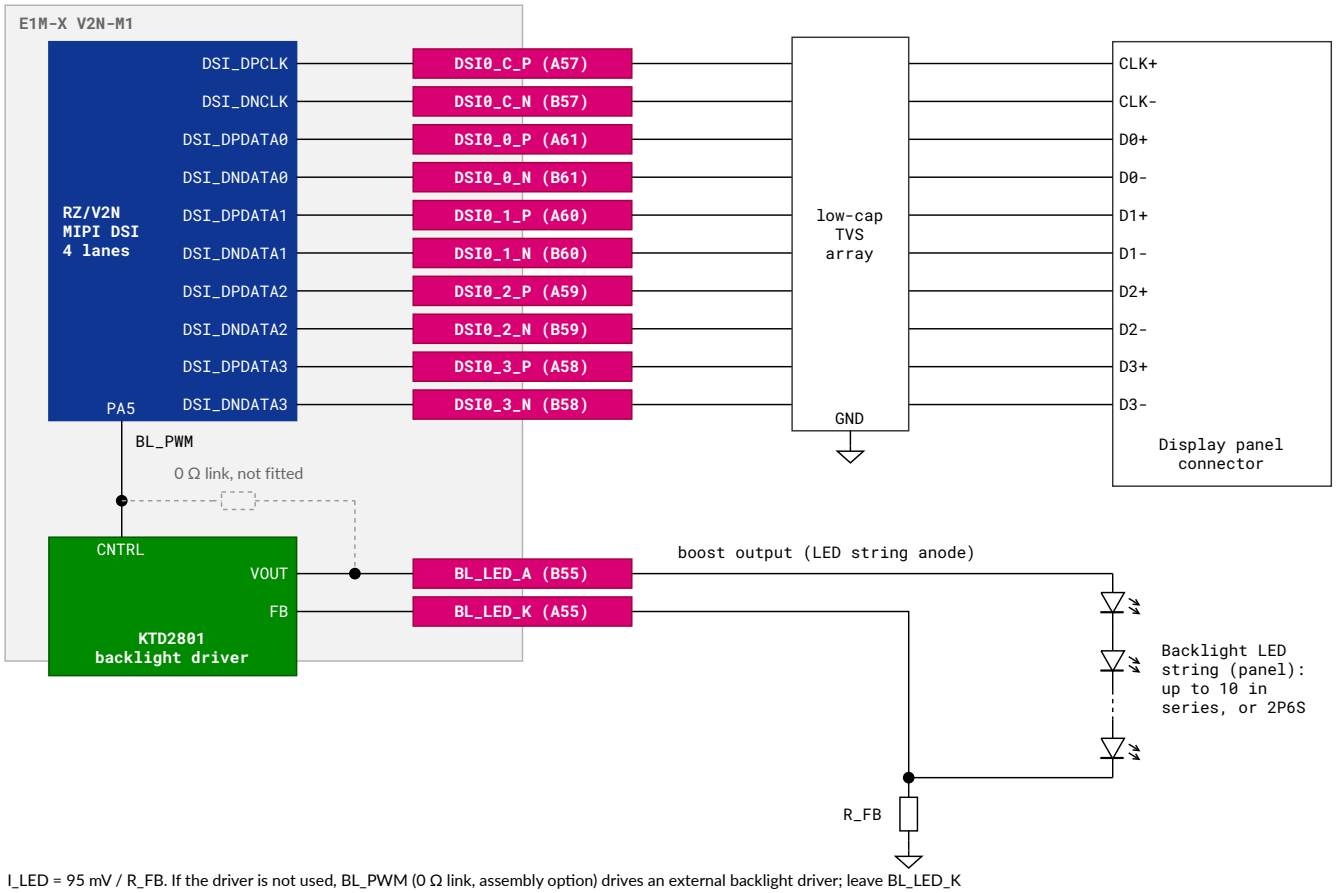


Connect SD_CLK, SD_CMD, SD_D0–SD_D3 directly. The module switches the SD signalling between 3.3 V and 1.8 V; SD_VDD_OUT stays 3.3 V.

Figure 18 E1M-X V2N-M1 SD Card Interface

8.6 MIPI DSI Display & Backlight Controller

Renesas RZ/V2N has a 4-lane MIPI DSI interface for an external display, supporting up to FHD resolution. The RZ/V2N also includes an internal 3D GPU (Arm Mali™-G31) that can accelerate display rendering.



I_LED = 95 mV / R_FB. If the driver is not used, BL_PWM (0 Ω link, assembly option) drives an external backlight driver; leave BL_LED_K floating.

Figure 19 E1M-X V2N-M1 Display Connection with Backlight Driver

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E1M-X has a backlight driver for external screens, controlled directly from the Alp SDK™. The driver is optional; outputs are configured via the BL_LED_A and BL_LED_K pins. The driver supports up to 10 LEDs in series, or 2P6S.

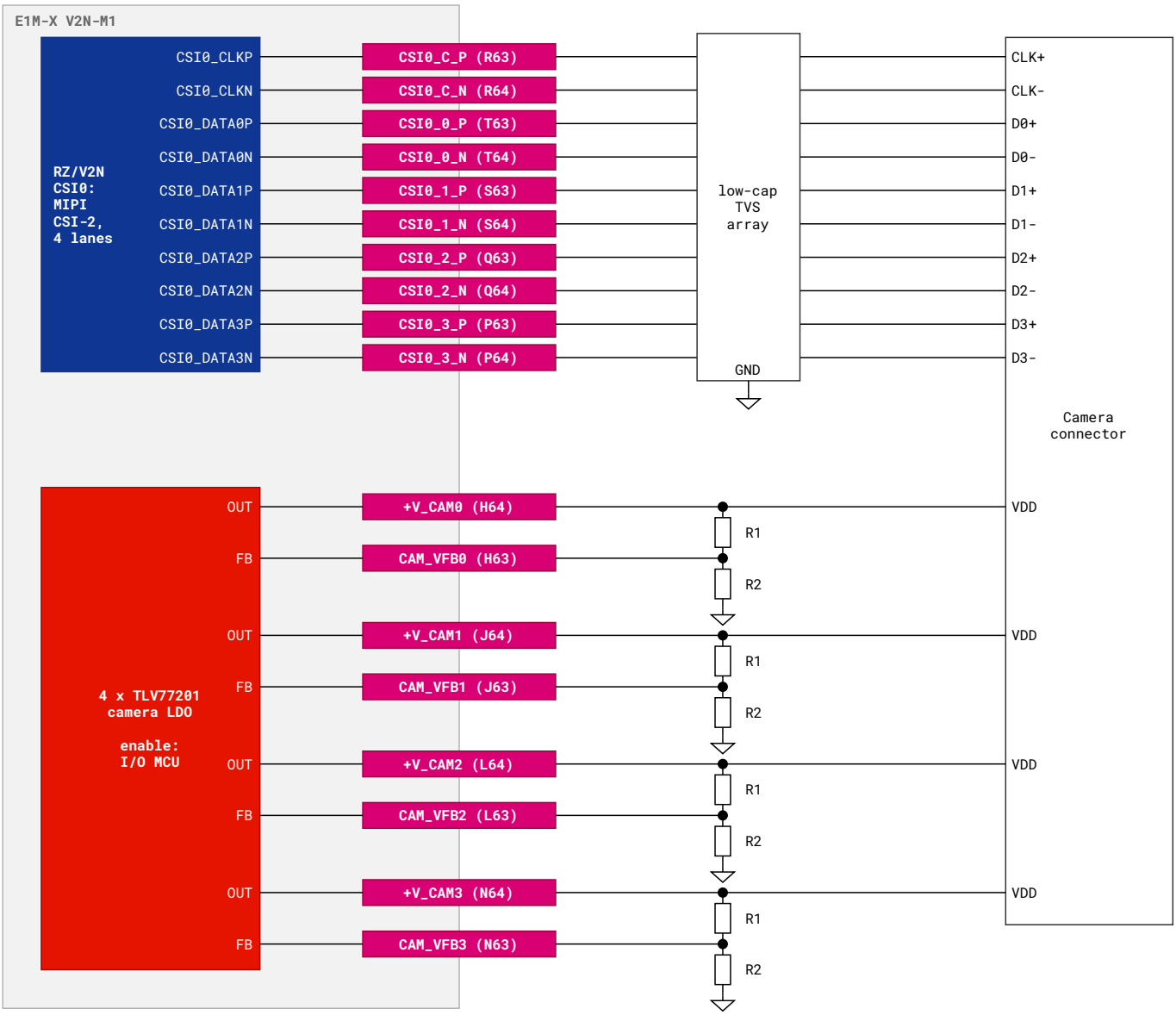
If the backlight driver is not needed, the BL_PWM signal can be exposed directly to drive an external backlight driver. The MIPI DSI interface does not include on-module EMI or ESD protection; protect the DSI lanes with a low-capacitance TVS array on the carrier board.

The feedback resistor value can be computed from the required LED current:

$$I_{\mathrm{LED}} = 95\frac{\mathrm{mV}}{R_{\mathrm{FB}}}$$

8.7 MIPI CSI Camera

Renesas RZ/V2N has two 4-lane MIPI CSI interfaces for external cameras. The RZ/V2N also includes an internal ISP (Arm Mali™-C55) that can accelerate image processing.



V_CAM = 0.6 V × (1 + R1 / R2); R1 + R2 <= V_OUT / (I_FB × 100). Place the dividers close to the CAM_VFBx pads. +V_CAMx: 0.6 V to 3.3 V, 300 mA max per rail.
CSI1 is identical: C X63 / X64, D0 Z63 / Z64, D1 Y63 / Y64, D2 W63 / W64, D3 V63 / V64 (P / N).

Figure 20 E1M-X V2N-M1 Camera Connection with LDO (CSI0; CSI1 identical)

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E1M-X supports direct camera implementation via on-board LDOs. Place the feedback resistors as close as possible to the CAM_VFBx pins. The MIPI CSI interface does not include on-module EMI or ESD protection; protect the CSI lanes with a low-capacitance TVS array on the carrier board.

The output voltage is set by the divider:

$$V_{\mathrm{CAM}} = 0.6\ \mathrm{V} \times \left(1 + \frac{R_1}{R_2}\right)$$

To minimise feedback-pin current error, set the divider current to 100 × the maximum feedback-pin current. The resulting series resistance limit is:

$$R_1 + R_2 \leq \frac{V_{\mathrm{OUT}}}{I_{\mathrm{FB}} \times 100}$$

8.8 Microphone – PDM

E1M-X supports up to 4 digital microphones over 2 PDM interfaces.

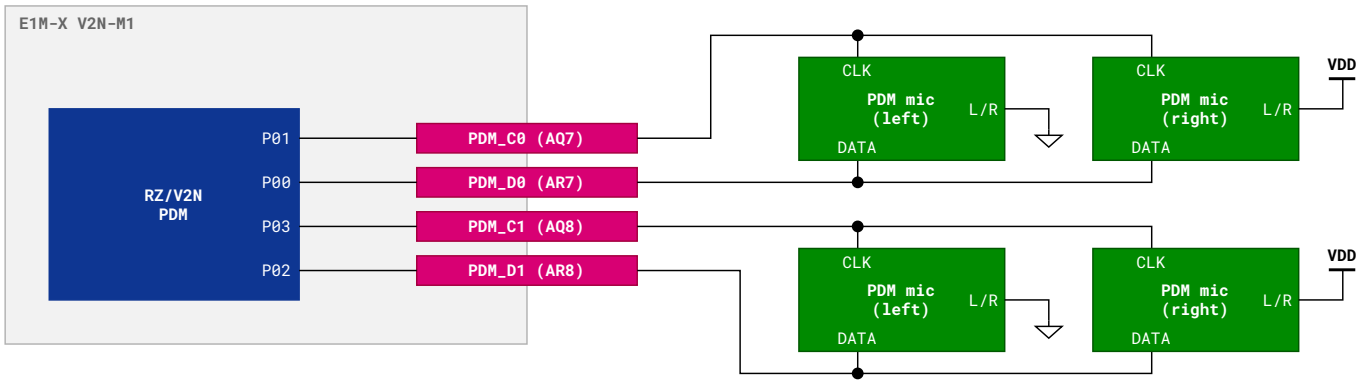


Figure 21 E1M-X V2N-M1 PDM Connection (two microphones per data line)

Refer to the E1M-X hardware design guide for full details.

8.9 Analog Inputs

E1M-X has 8 analog input channels (ADC). The analog inputs are connected to the secondary MCU, which has a 12-bit ADC with a 5.3 Msps sampling rate. Analog inputs are referenced to 1V8.

Refer to the secondary-MCU datasheet for electrical characteristics. TBD.

8.10 Analog Outputs

E1M-X has 2 analog output channels (DAC). The analog outputs are connected to the secondary MCU, which has a 12-bit DAC with a 1 kHz sampling rate. Analog outputs are referenced to 1V8.

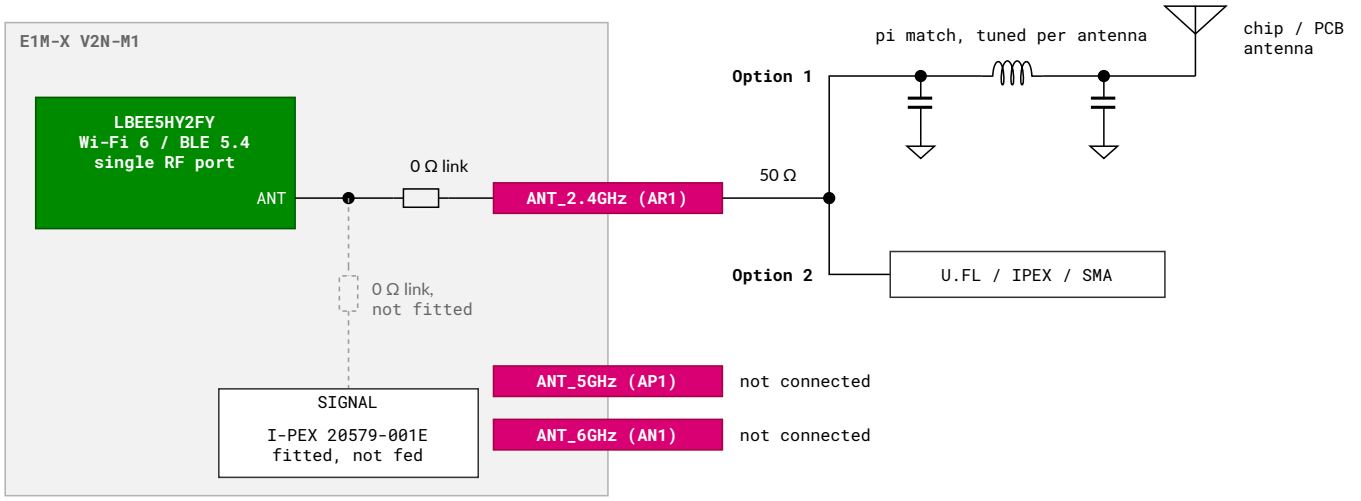
Refer to the secondary-MCU datasheet for electrical characteristics. TBD.

9 Components

9.1 Wireless Module & Antenna

E1M-X V2N-M1 integrates the Murata LBEE5HY2FY Wi-Fi 6 + BLE 5.4 combo module (based on Infineon CYW55513) on-module per **E1M Spec** §6.5. The radio has a single RF port for all bands; it exits on pad AR1 (ANT_2.4GHz) on a 50 Ω controlled-impedance trace, and the carrier provides either an RF connector or a PCB antenna.

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AR1 carries all bands of the radio (2.4 / 5 / 6 GHz). Option 1 or 2 (one only). Use only a certified antenna (Regulatory Information). Standard build: the 0 Ω feed goes to AR1. Assembly option: the feed is moved to the on-module I-PEX connector, and AR1 is then not driven.

Figure 22 E1M-X V2N-M1 Antenna Connection

9.1.1 RF Characteristics

Symbol	Description	Min	Typ	Max	Unit
Wi-Fi 6 (802.11ax)					
$f_{op,2.4}$	2.4 GHz band operating range	2400	–	2483.5	MHz
$f_{op,5}$	5 GHz band operating range	5150	–	5850	MHz
$f_{op,6}$	6 GHz band operating range	5945	–	7125	MHz
P_{TX}	TX output power (MCS0, 2.4 GHz)	–	TBD	TBD	dBm
P_{RX}	RX sensitivity (MCS0)	TBD	–	–	dBm
η	Max PHY throughput (single stream)	–	143	–	Mbps
Bluetooth LE 5.4					
$f_{op,BLE}$	Operating frequency range	2402	–	2480	MHz
$P_{TX,BLE}$	TX output power	–	TBD	TBD	dBm
$P_{RX,BLE}$	RX sensitivity (1 Mbps)	TBD	–	–	dBm

Table 21 E1M-X V2N-M1 Wi-Fi 6 / BLE RF Characteristics

9.1.2 Antenna Options

The E1M-X V2N-M1 has **one** connected antenna pad, AR1 (ANT_2.4GHz), which carries all bands of the radio (2.4 / 5 / 6 GHz). ANT_5GHz (AP1) and ANT_6GHz (AN1) are not connected.

1. **On-module I-PEX connector (20579-001E)** — the connector is fitted, but in the standard build its 0 Ω feed is not fitted and the radio feeds AR1. As an assembly option the feed is moved from AR1 to the connector; connect an external antenna directly to the module.
2. **Carrier-board PCB antenna** — route the AR1 pad as a 50 Ω controlled-impedance trace to a chip / PCB antenna.
3. **Carrier-board RF connector** — extend the 50 Ω trace to a U.FL / IPEX / SMA connector on the carrier.

Maximum antenna gain to maintain regulatory compliance is TBD dBi per band.

9.1.3 Regulatory Information

The on-module combo radio is pre-certified for the regions below. Reusing the module's certifications on the customer's end product requires following the integration guidelines (antenna gain, RF trace, enclosure) from the certification report.

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Region	Standard	Certificate ID	Notes
United States	FCC Part 15	TBD	Modular grant pending.
Europe	RED / CE	TBD	–
Canada	ISED RSS-247	TBD	–
Japan	MIC (Japan)	TBD	–

Table 22 Wireless Regulatory Approvals

> **Warning:** Certifications apply only when the module is used with the antenna(s) listed in the certification report. Using an unlisted antenna voids the modular grant and requires re-certification on the customer's end product.

9.2 Memories

E1M-X offers several memory options:

- **eMMC** — up to 256 GB.
- **LPDDR4X** — up to 8 GB.
- **NOR Flash** — on-module, boot-supported.

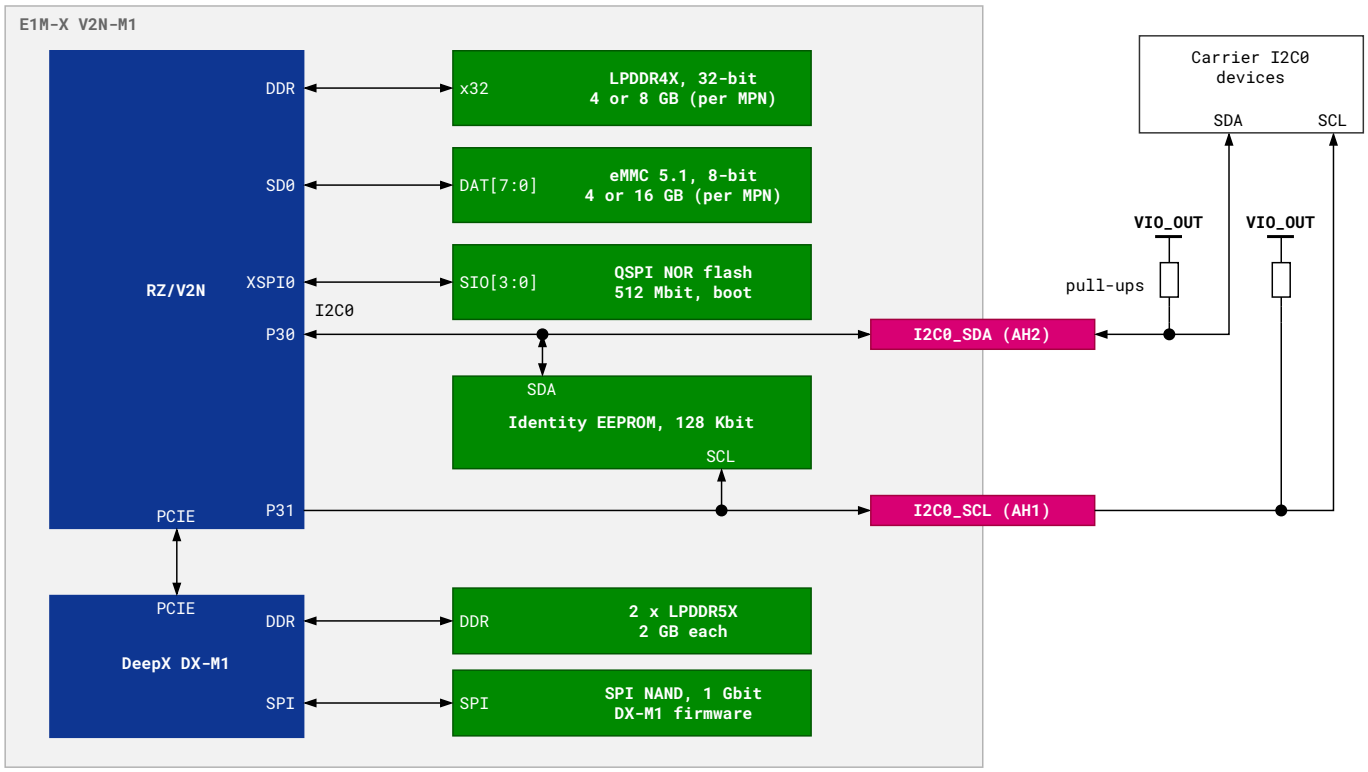


Figure 23 E1M-X V2N-M1 Memory Options

An optional EEPROM (N24S128C4DYT3G from onsemi) is also available on the board, connected through `I2C0` on E1M-X. It can be flashed in production. `I2C0` is also accessible on the E1M-X pinout. Refer to the E1M hardware design guide for details.

9.3 Secure Element

E1M-X V2N-M1 includes an Infineon OPTIGA™ Trust M secure element (`SLS32AIA010MLUSON10XTMA2`) on the on-module board I^2C bus (`BRD_I2C`) at 7-bit address `0x30`, for secure-boot and key-storage applications.

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9.4 Clocks

The on-module clock generator (5L35023B, BRD_I2C 0x69), with a 24 MHz crystal and supplies on VDD1G_1P8, provides:

Output	Frequency	Destination
REF	24 MHz	RZ/V2N QEXTAL, through a 22 Ω series resistor.
SE1	32.768 kHz	RZ/V2N RTXIN, and the Wi-Fi module WL_32K (LPO_IN), each through a 22 Ω series resistor.
SE2	25 MHz	CLK_25M: both RTL8211F Ethernet PHYs through an on-module clock buffer (powered from VDD_1V8), and the GD32 oscillator input through a 22 Ω series resistor.
SE3	–	Audio_CLKB to the RZ/V2N (P10), through a 22 Ω series resistor; output enable OE3 from the RZ/V2N P67.
DIFF1	–	LP-HCSL PCIe reference clock to the reference-clock buffer: PCIE0_CLK pads and the DX-M1 (Section 8.3).
DIFF2	–	LP-HCSL PCIe reference clock to the RZ/V2N PCIE_REFCLKP0 / PCIE_REFCLKN0 (Section 8.3).

Table 23 Clock Generator Outputs

A 22.5792 MHz crystal (44.1 kHz audio family) is on the RZ/V2N AUDIO_XTAL / AUDIO_EXTAL, and a 50 MHz crystal is on the DX-M1. The firmware sets the clock-generator crystal load capacitance and enables DIFF1 only while the DX-M1 rails are up.

9.5 PCB Temperature Sensor

An on-board PCB temperature sensor (TI TMP112D or equivalent) is available on BRD_I2C at address 0x40.

10 Environmental & Reliability

10.1 Operating & Storage Conditions

Parameter	Symbol	Min	Max	Unit
Ambient operating temperature	T_A	- 40	+85	°C
Storage temperature	T_{STG}	- 40	+125	°C
Relative humidity (operating, non-condensing)	RH	TBD	TBD	%

Table 24 Environmental Conditions

> **Warning:** Sustained AI workloads (DRP-AI3 + DX-M1 running concurrently) push the SoM toward its thermal envelope at +85 °C ambient. Active cooling or a copper-pour heatsink contact is recommended above 50% DX-M1 utilisation at the high end of the temperature range.

10.2 Reflow Profile

The E1M-X V2N-M1 is qualified per IPC/JEDEC J-STD-020 to MSL TBD. The recommended starting profile is the lead-free reflow profile shown in Figure 24: the measured E1M-AEN profile, smoothed, without its zone-boundary kink (an E1M-AEN module, a JTR1000 convection reflow oven, ALPHA OM338 (SAC, Pb-free) solder paste and a VCAM i612D profiler sampling every 0.5 s). On that run the peak package temperature was 240.9–244.3 °C and the time at or above 220 °C 56.5–60.0 s (the measured ranges in the table below); the SAC liquidus is 217 °C. Customers must keep the process within the recommended window in the table below and follow the dry-pack handling instructions in Section 15.2.

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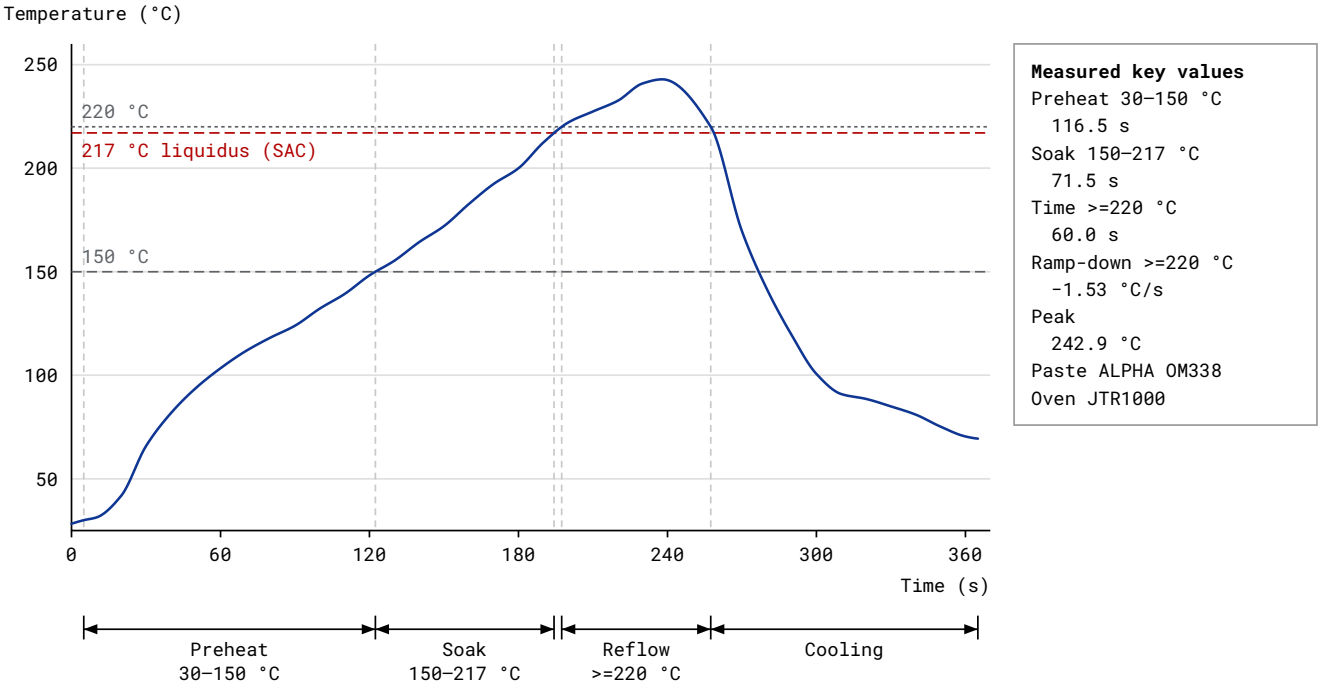


Figure 24 Recommended starting profile: measured E1M-AEN profile, smoothed

Parameter	Window min	Window max	Measured	Unit
Preheat time, 30–150 °C	60	160	116.5–122.0	s
Soak time, 150–217 °C	60	120	70.5–73.5	s
Time at or above 220 °C	45	90	56.5–60.0	s
Ramp-down slope at or above 220 °C	-4	-0.5	-1.53 to -1.66	°C/s
Peak package temperature	230	250	240.9–244.3	°C

Table 25 Reflow Profile Parameters (Pb-free): recommended window and measured values

10.3 Reliability Data

Parameter	Symbol	Value	Unit
Mean Time Between Failures (Telcordia SR-332, T_A = +25 °C)	MTBF	TBD	h
Moisture Sensitivity Level	MSL	TBD	–
Qualified shelf life (in dry-pack)	–	TBD	months

Table 26 Reliability Targets

11 Software & Operating System Support

The E1M-X V2N-M1 is supported by the open-source **Alp SDK™**. Out of the box, the SDK supports:

- **Linux** (Yocto) on the quad Cortex-A55 application cluster, **with the DX-M1 driver and runtime**. Each SKU has its own Yocto MACHINE: `e1m-v2m101-a55`, `e1m-v2m102-a55`, `e1m-v2m103-a55`. The DeepX driver/runtime layer is wired into these V2N-M1 machines only, not into the `e1m-v2n10x-a55` machines of the V2N family.

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- **Zephyr RTOS** on the RZ/V2N's internal Cortex-M33 system manager. On `E1M-V2M101` the board target is `alp_e1m_v2m101_m33_sm/r9a09g056n48gbg/cm33`; the Zephyr M33 board trees for `E1M-V2M102` and `E1M-V2M103` are not yet built.

The on-module GD32 I/O-MCU is **not** a customer application target. It runs bridge firmware that Alp Lab programs in production; applications on the RZ/V2N reach the peripherals it owns through the bridge driver (`<alp/chips/gd32g553.h>`), and field updates of the bridge firmware arrive over the bridge link (`update_channel: alp_ota_spi_bridge`). Customer reflashing of the GD32 is supported only to recover a bricked module, with Alp Lab-supplied binaries.

Target / Runtime	Zephyr	Linux (Yocto)	DX-M1 driver
`RZ/V2N Cortex-A55 (e1m-v2m10x-a55 MACHINE)`	–	`Yes`	`Yes`
`RZ/V2N internal M33 (200 MHz)`	`Yes (E1M-V2M101)`	–	–
`GD32 I/O-MCU (Cortex-M33 @ 216 MHz)`	`Alp Lab bridge firmware`	–	–

Table 27 Software Support Matrix

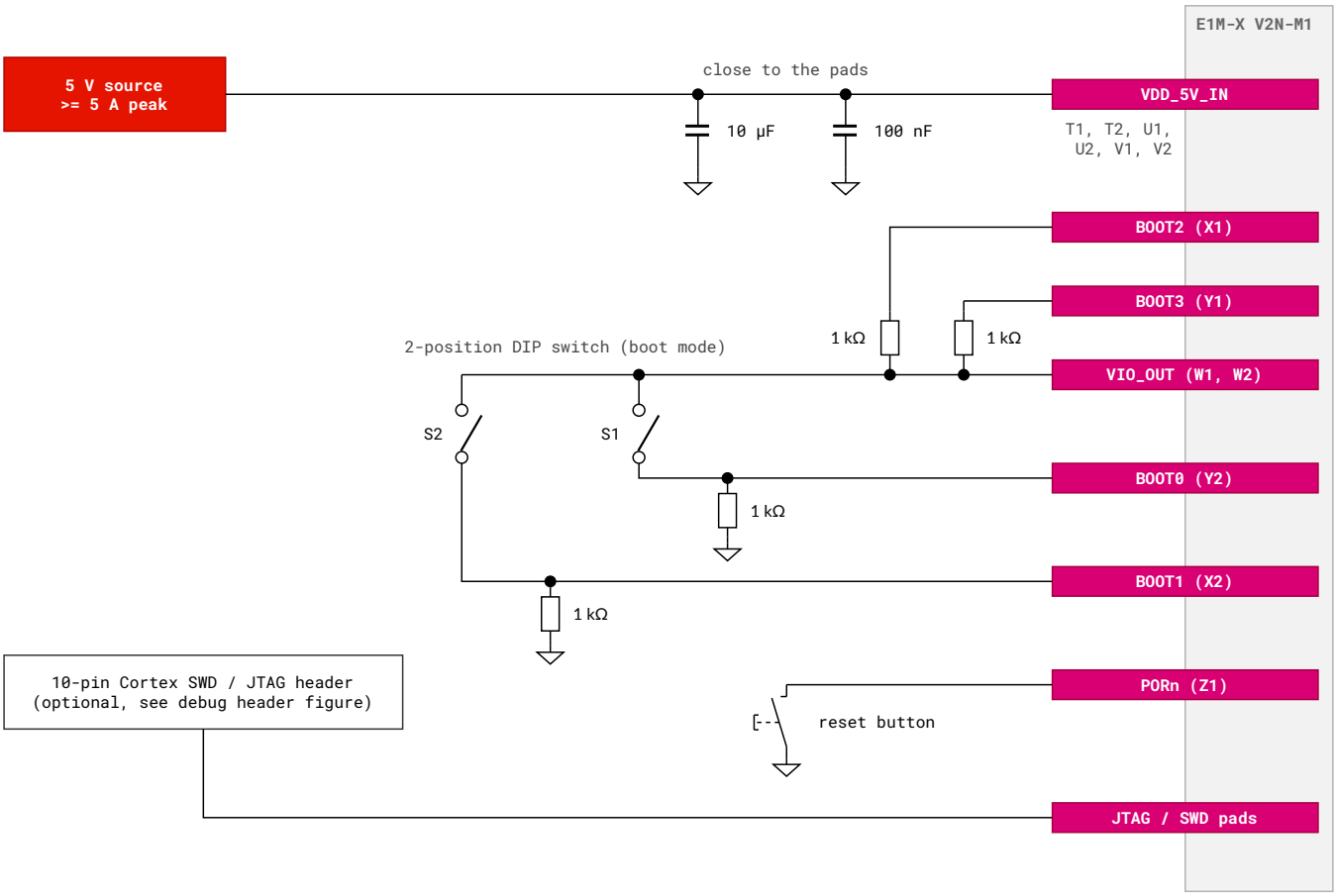
Warning: Build the A55 image for the module's own V2N-M1 `MACHINE` (`e1m-v2m101-a55` / `e1m-v2m102-a55` / `e1m-v2m103-a55`). A V2N-family machine does not carry the DeepX driver and runtime.

Note: See the Alp SDK™ repository (`docs/firmware-quickstart.md` and `docs/soms/v2n-m1.md`) for the per-target build instructions. For deeper integration patterns, see **AN-001** through **AN-010**; for DX-M1 specifically, **AN-009**.

12 Reference Schematic

The minimum carrier-board design below brings up an E1M-X V2N-M1 with a single 5 V input, reset push-button, boot-mode DIP switch, and JTAG/SWD debug header. The DX-M1 needs no carrier-side wiring — it lives entirely on the SoM behind the on-module PCIe mux.

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MODULE_EN (AA1), MODULE_STBY (AB1): leave floating if unused (internal pull-ups). BOOT2, BOOT3: 1 kΩ pull-ups to VIO_OUT (CM33 boot: BOOT3 1 kΩ to GND). Every BOOT strap: 1 kΩ to VIO_OUT for 1, 1 kΩ to GND for 0; an open strap reads 1 (RZ/V2N internal pull-up), do not rely on it. JTAG / SWD pads: JTAG_TCK/SWDCLK (AJ1), JTAG_TDI (AJ2), JTAG_TMS/SWDIO (AK1), JTAG_TDO (AK2).

Figure 25 E1M-X V2N-M1 Minimum Reference Schematic

Required external components:

- 5 V power source (>= 5 A peak) to VDD_5V_IN (T1, T2, U1, U2, V1, V2). Size for the higher peak (DRP-AI3 + DX-M1 + dual-Ethernet) compared to a V2N-only carrier.
- Bulk decoupling: 1 × 10 µF + 1 × 100 nF close to VDD_5V_IN.
- Boot-mode 2-position DIP switch from VIO_OUT (W1, W2) to BOOT0, BOOT1, with a 1 kΩ pull-down to GND on each line (closed = 1, open = 0).
- 1 kΩ pull-up from BOOT2 (X1) to VIO_OUT (W1, W2).
- 1 kΩ pull-up from BOOT3 (Y1) to VIO_OUT (W1, W2) for Cortex-A55 boot (a 1 kΩ pull-down to GND instead for Cortex-M33 boot).
- Reset push-button between PORn (Z1) and GND.
- 10-pin Cortex SWD/JTAG header on JTAG_* pads (optional, for development).

Do not leave a boot strap open: the RZ/V2N internal pull-ups read an open strap as 1, but the carrier sets every strap with its own 1 kΩ resistor.

Optional carrier-board components are described per interface in Section 8, and in detail in **HG-V2N-M1-001**.

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13 Compliance & Certifications

13.1 Environmental Compliance

Standard	Description	Status
RoHS 3 (EU 2015/863)	Restriction of hazardous substances	Compliant
REACH (EC 1907/2006)	Substances of very high concern	Compliant
Halogen-free (IEC 61249-2-21)	Br + Cl content limits	TBD
Conflict minerals (Dodd-Frank §1502)	Tin, tungsten, tantalum, gold sourcing	TBD

Table 28 Environmental Compliance

13.2 Wireless Certifications

See Section 9.1.3 for the per-region wireless certification IDs.

13.3 Functional Safety & Industry-specific Compliance

The E1M-X V2N-M1 is not currently certified for safety-critical applications (IEC 61508, ISO 26262, IEC 62304, etc.). Contact Alp Lab for the most recent qualification status.

14 Mechanical & Footprint Dimensions

All dimensions are in mm unless otherwise noted.

14.1 Module Dimensions

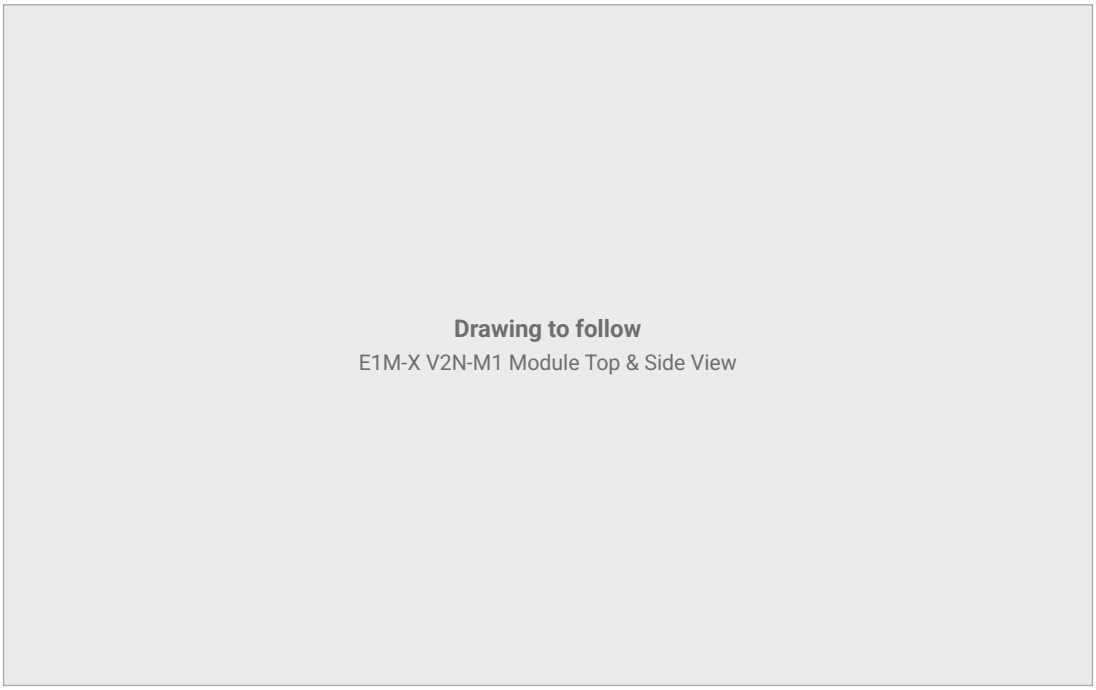


Figure 26 E1M-X V2N-M1 Module Top & Side View

Parameter	Symbol	Min	Max	Unit
Module length	L	64.9	65.1	mm

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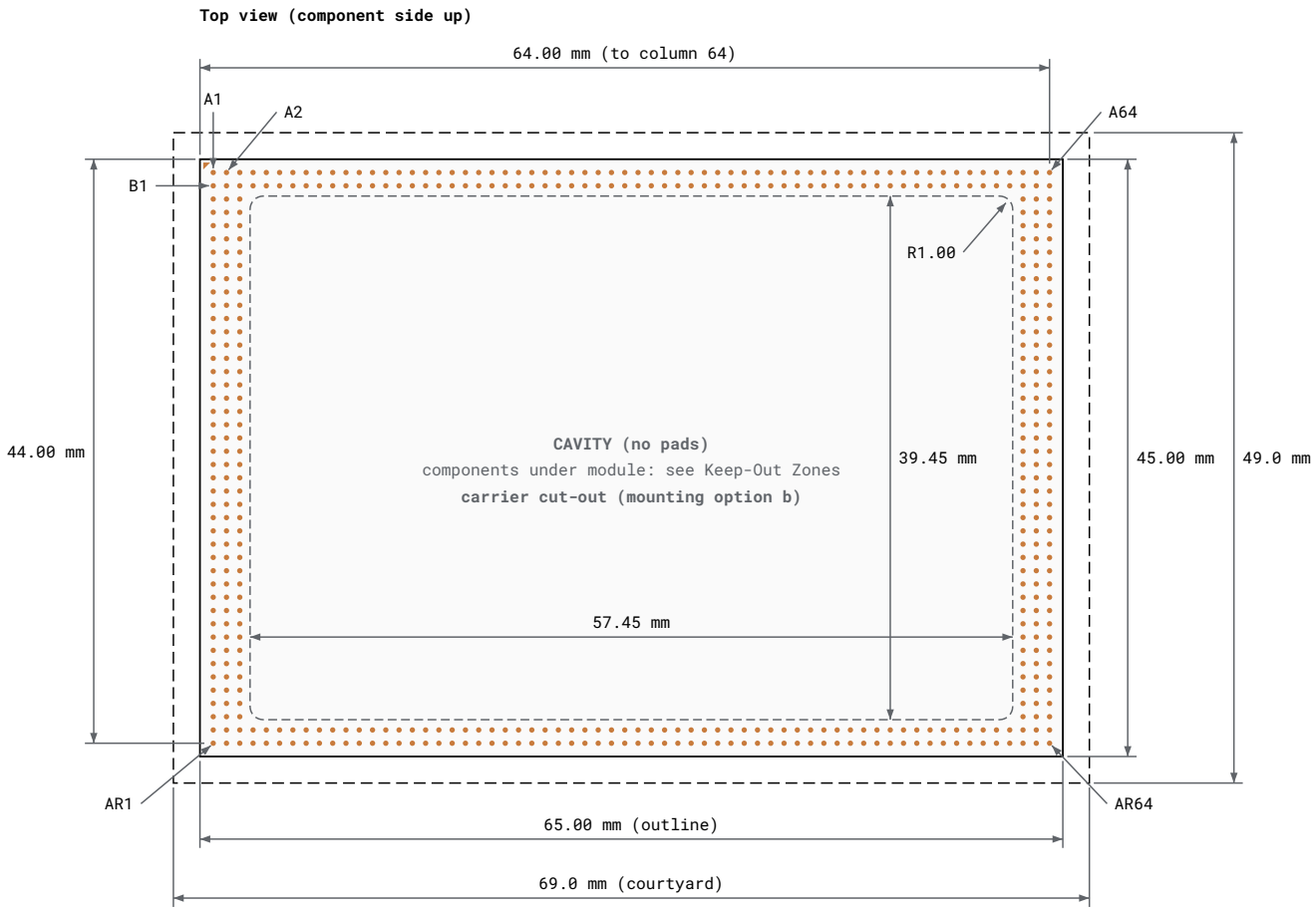
Parameter	Symbol	Min	Max	Unit
Module width	W	44.9	45.1	mm
Module height (PCB + tallest component)	H	–	TBD	mm
Module mass	m	–	TBD	g

Table 29 E1M-X V2N-M1 Mechanical Dimensions

14.2 Recommended PCB Land Pattern

The recommended carrier-board land pattern follows IPC-7351 nominal density for LGA packages. Identical to the V2N family — V2N and V2N-M1 are **pin-compatible**.

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Pad A1 next to the 0.52 mm triangular pin-1 fiducial, centred 1.00 mm from the left and top edges.
Rows A–AR top to bottom, columns 1–64 left to right; 496 pads on a 1.00 mm grid.
Courtyard: 2.0 mm clearance around the module outline, 69.0 mm across x 49.0 mm down.
Dimensions per E1M-STD §5.1.2 (E1M-X footprint) and §5.1.3 (carrier land pattern).

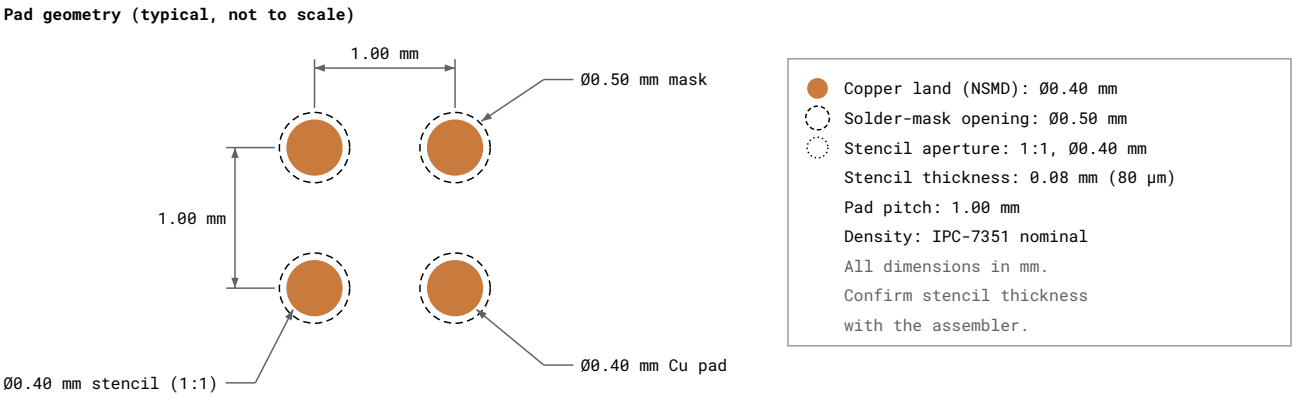


Figure 27 E1M-X V2N-M1 Recommended Land Pattern (top view; values per E1M-STD §5.1.2 and §5.1.3)

Parameter	Symbol	Value	Unit
Pad pitch (signal grid)	p	1.00	mm
Pad size (signal)	–	Ø0.40 (round, NSMD)	mm
Solder-mask opening	–	Ø0.50 (NSMD)	mm
Stencil aperture	–	1:1, Ø0.40	mm
Stencil material	–	Nano-coated steel mesh	–

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Parameter	Symbol	Value	Unit
Stencil thickness (recommended)	t	80	µm
Courtyard	–	2.0 mm clearance around the module outline, 69.0 × 49.0	mm

Table 30 Land Pattern Parameters

14.3 Keep-Out Zones

The E1M-X V2N-M1 carries components on its bottom side, in the central cavity inside the pad band. A module **shall not** be placed directly on a carrier board. Mount it in one of two ways (Figure 28):

1. **On a spacer PCB:** a spacer PCB between the module and the carrier raises the module so that its bottom-side components clear the carrier (E1M-STD §5.2). The spacer is soldered on both faces: the module LGA pads to the spacer, and the spacer to the carrier.
2. **Over a carrier cut-out:** a through cut-out in the carrier the size of the module's central cavity, 57.45 mm across × 39.45 mm down with R1.00 corners, its left edge 3.775 mm from the left outline edge and its top edge 2.775 mm from the top outline edge (E1M-STD §5.1.2). The bottom-side components sit in the cut-out.

With either option the carrier **shall** have no components inside the cavity outline (57.45 mm across × 39.45 mm down, R1.00 corners, 3.775 mm from the left and 2.775 mm from the top outline edge). The spacer-PCB thickness and the maximum bottom-side component height are TBD; E1M-STD §5.2 does not specify them. RF traces (especially the antenna feed) must be routed away from high-current digital paths.

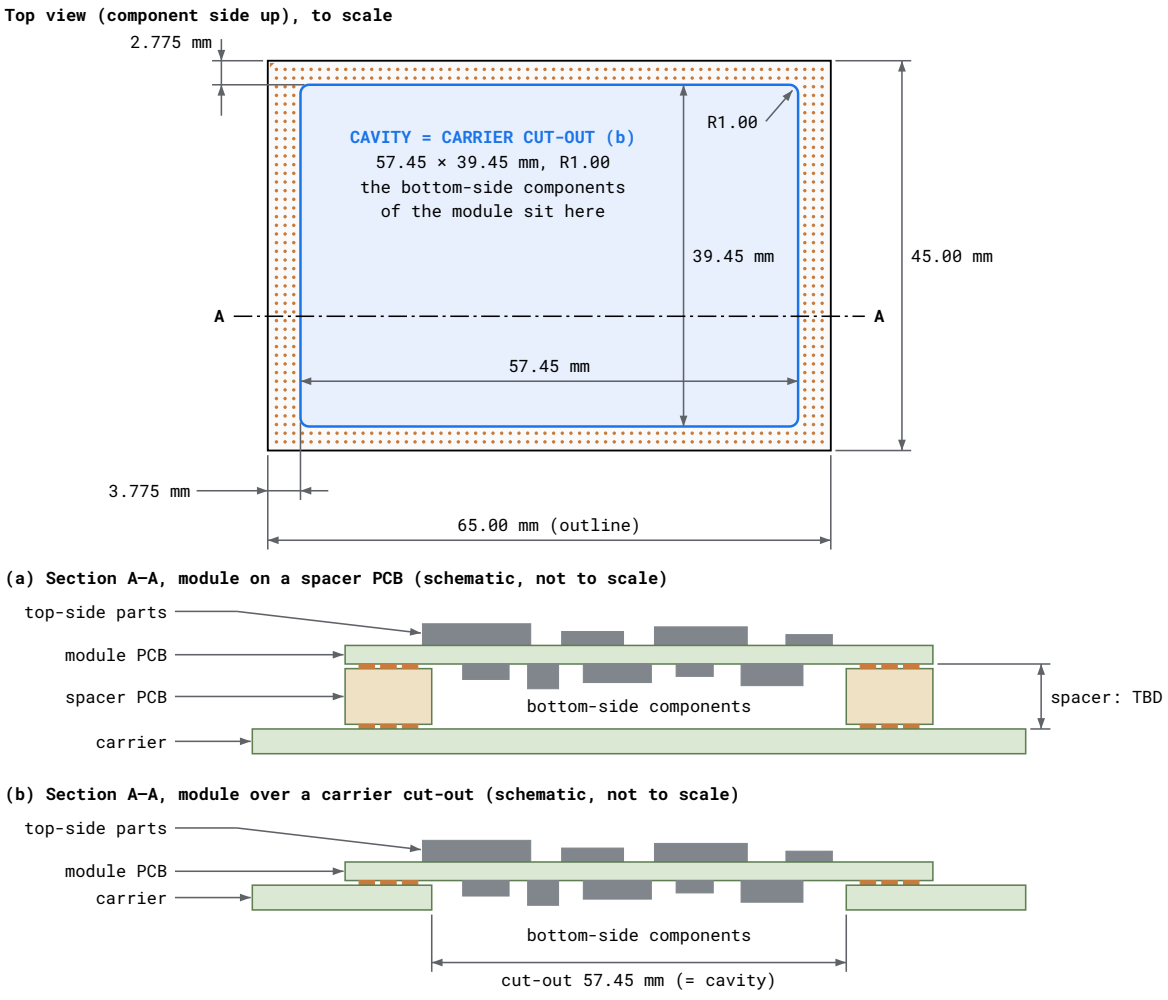


Figure 28 E1M-X V2N-M1 mounting: cavity = carrier cut-out (top view); section A–A, spacer PCB / cut-out

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14.4 Module Marking

Each module is laser-marked on the top side with:

- Manufacturer logo (Alp Lab)
- Full MPN (e.g. `E1M-V2M101`)
- Production date code (YYWW)
- Serial number (10 characters)
- FCC ID, ISED IC, MIC marks (where applicable)
- Wi-Fi MAC address (last 4 digits)
- DX-M1 firmware version code

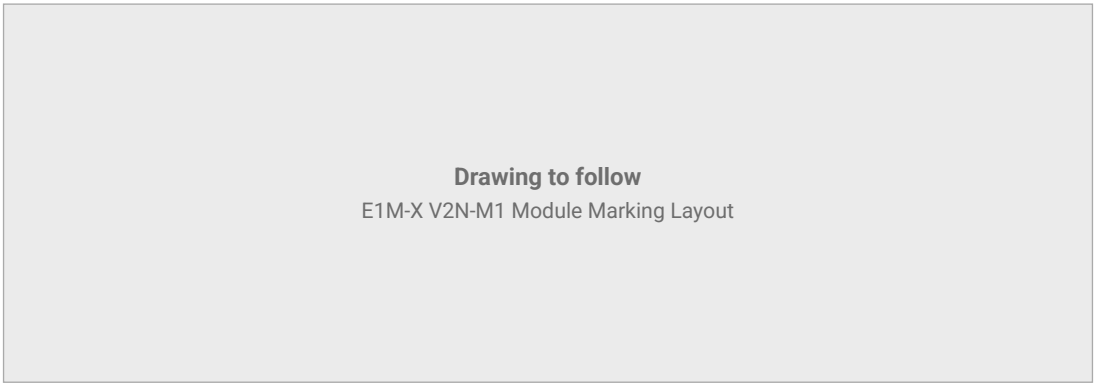


Figure 29 E1M-X V2N-M1 Module Marking Layout

15 Packaging

15.1 Tray

A JEDEC-compliant tray is available for low-volume or prototyping orders.

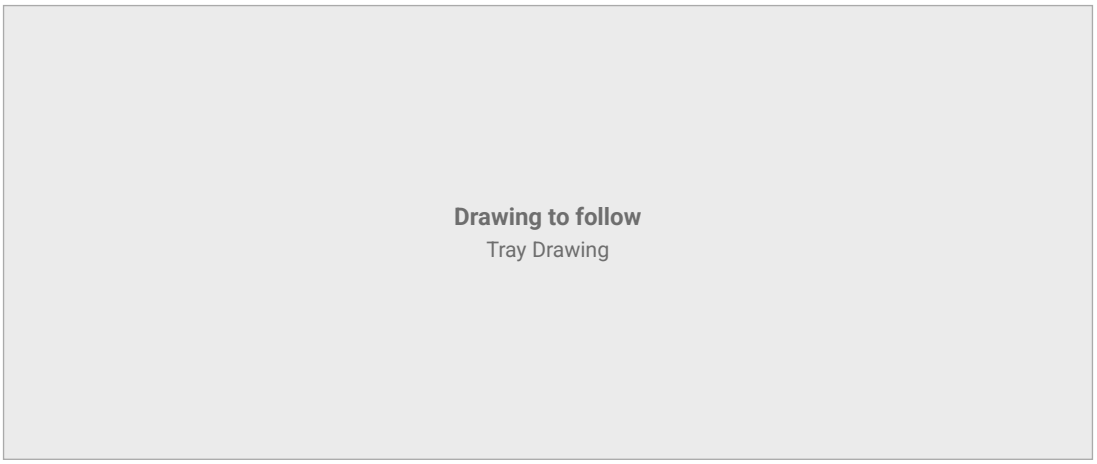


Figure 30 Tray Drawing

15.2 MSL & Handling

The E1M-X V2N-M1 is classified to Moisture Sensitivity Level (MSL) TBD per IPC/JEDEC J-STD-020. Modules are shipped in dry-pack with desiccant and a humidity-indicator card.

After opening the dry-pack:

- Floor life: TBD hours at <= 30 °C / <= 60% RH.

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- If floor life is exceeded before reflow, bake at TBD °C for TBD h before assembly.

Refer to IPC/JEDEC J-STD-033 for full moisture/reflow handling procedures.

16 Ordering Information

16.1 MPN Decoder

Field	Example	Description
Family	E1M	Edge-1 AI Module standard footprint.
Form factor	-V	Implied 45 × 65 mm E1M-X.
Product line	V2M	Renesas RZ/V2N with on-module DeepX DX-M1 accelerator (the "M" in V2M denotes the DX-M1). Sibling line V2N omits the DX-M1.
Variant code	101	Three-digit code identifying the memory configuration: 101 = 4 GB LPDDR4X + 4 GB eMMC, 102 = 8 GB LPDDR4X + 16 GB eMMC, 103 = 4 GB LPDDR4X + 16 GB eMMC. It is not a hardware-revision field.

Table 31 E1M-X V2N-M1 MPN Convention

Note: The module hardware revision is not encoded in the MPN. It is recorded in the on-module identity EEPROM and read by the Alp SDK™ at run time.

Note: Example: **E1M-V2M101** = E1M-X form factor, RZ/V2N + DX-M1, variant 101 (4 GB LPDDR4X + 4 GB eMMC).

16.2 Ordering Matrix

MPN	CPU	LPDDR4X	eMMC	AP cores	RT cores	AI	Temp. (°C)
E1M-V2M101	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 4 GB	A55 4 × 1.8 GHz	V2N M33 1 × 200 MHz I/O MCU M33 1 × 216 MHz	V2N: 4 TOPS DeepX DX-M1: 25 TOPS	-40 to +85
E1M-V2M102		8 GB	eMMC 5.1, 16 GB				
E1M-V2M103		4 GB	eMMC 5.1, 16 GB				

Table 32 Ordering Information

All configurations above include:

- 2.4 GHz / 5 GHz / 6 GHz Wi-Fi® + Bluetooth® 5.4 combo module
- 2 × 1 Gbit Ethernet PHY
- 1 × display backlight driver
- 4 × LDOs for external cameras
- 512 Mbit QSPI NOR flash
- I/O MCU Cortex-M33 (216 MHz)
- Secure element (Infineon OPTIGA™ Trust M)
- EEPROM
- RTC
- Temperature sensor
- DeepX DX-M1 25-TOPS AI accelerator (PCIe-attached on-module)

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- 2 × LPDDR5X companion memory for DX-M1
- SPI NAND companion storage for DX-M1

RoHS-compliant. Contact Alp Lab for custom assembly variants (lead finish, ball material, etc.).

17 References & Related Documents

Ref.	Title	Source
[1]	Renesas RZ/V2N Hardware Reference Manual	Renesas Electronics
[2]	Renesas RZ/V2N Series Datasheet	Renesas Electronics
[3]	DeepX DX-M1 Hardware Integration Manual	DeepX (vendor-supplied)
[4]	DeepX DX-COM™ User Guide	DeepX (vendor-supplied)
[5]	E1M™ Specification	E1M-STD-1.0 / github.com/alplabai/e1m-spec
[6]	E1M-X V2N-M1 Hardware Design Guide	Alp Lab (HG-V2N-M1-001)
[7]	E1M-X V2N Datasheet (sibling, without DX-M1)	Alp Lab (DS-V2N-001)
[8]	E1M-X EVK User Guide	Alp Lab (UG-E1M-X-001)
[9]	E1M-X EVK Getting Started Guide	Alp Lab (QS-E1M-X-EVK-001)
[10]	AN-009: DeepX DX-M1 First Inference Walkthrough	Alp Lab
[11]	Alp SDK™ Documentation	github.com/alplabai/alp-sdk
[12]	IPC/JEDEC J-STD-020 — Reflow Profile	JEDEC
[13]	IPC/JEDEC J-STD-033 — Moisture/Reflow Handling	JEDEC

Table 33 Related Documents

18 Revision History

Revision	Changes	Date
0.1	• Initial draft (docx port).	December 2025
0.2	• Second draft. • Added DeepX DX-M1 standalone AI accelerator description and PCIe-multiplexing details.	January 2026
0.3	• SoM-typical sections added: Module Variants, Recommended Operating Conditions, ESD & Latch-up, Thermal Characteristics, Power Architecture / Power-Up Sequence / Power Consumption, Boot Modes (top-level), Reset & Module Enable, JTAG / SWD Debug, Wireless RF/Antenna/Regulatory subsections, Environmental & Reliability, Software & OS Support, Reference Schematic, Compliance & Certifications, Mechanical & Footprint subsections, Packaging subsections, MPN Decoder, References, Legal Notices.	May 2026
0.4	• Pin-out drawing added: top-view, colour-coded 496-pad E1M-X diagram generated from the pin tables. • On-module interface ESD/EMI protection removed except on the SDIO / SD-card interface; carrier board must now provide ESD/EMI protection on Ethernet, MIPI DSI, and MIPI CSI. • Reflow profile populated (Pb-free, ALPHA OM338, peak 241–244 °C) with a parameters table. • SMT stencil specified (nano-coated steel mesh, 80 µm).	June 2026
0.5	• Cover page: replaced the block-diagram placeholder with front/back product photos of the E1M-X V2N-M1 module (with DeepX DX-M1).	July 2026
0.6	• Cover photos swapped to transparent-background versions.	July 2026

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Revision	Changes	Date
0.7	• Corrected the Alp SDK and E1M Specification repository links: the alpDevs GitHub organisation does not exist, so every link 404'd; the canonical organisation is alplabai.	July 2026
0.8	• Recommended Operating Conditions: removed the Junction operating temperature (T_J) row; the module is specified over the ambient range (- 40 °C to +85 °C). • Power-Up & Reset Sequence: clarified that the on-module GD32 supervisor sequences the internal rails (RZ/V2N, DX-M1, LPDDR5X) and no carrier-side rail sequencing is required, separate from the carrier-side control-signal bring-up steps.	July 2026
0.9	• Module Variants and Ordering Matrix: added E1M-V2M103 (32 Gbit LPDDR4X + 128 Gbit eMMC 5.1 + DX-M1, same silicon and pin-out as E1M-V2M101/E1M-V2M102). • Power Architecture, Power-Up & Reset Sequence, Boot, Reset & Module Enable: corrected who powers and releases the DX-M1. Per Alp SDK™ v0.17.0 the DX-M1 rail is enabled, the DX-M1 reset released and the PCIe multiplexer routed by the RZ/V2N boot firmware (U-Boot on the Cortex-A55), not by the GD32 supervisor at power-up. • Software & OS Support: replaced the non-existent alp_e1m_v2n_a55 / alp_e1m_v2m_a55 board targets with the per-SKU Yocto MACHINEs (e1m-v2m101-a55 / e1m-v2m102-a55 / e1m-v2m103-a55) and the Cortex-M33 Zephyr target alp_e1m_v2m101_m33_sm/r9a09g056n48gbg/cm33. Bare-metal and Zephyr-SMP support on the A55 is no longer claimed. • The GD32 I/O-MCU is no longer listed as a customer application target: it runs Alp Lab-programmed bridge firmware, updated in the field over the bridge link; customer reflashing is for bricked-module recovery only. • MPN Decoder: replaced the memory-tier digit + two-digit hardware-revision reading, which E1M-V2M103 contradicts, with a three-digit variant code for the memory configuration; the hardware revision is held in the on-module identity EEPROM, not in the MPN. • Power Architecture and Boot: added warnings that the DX-M1 rail sequence must not be re-implemented outside the Alp Lab U-Boot (an out-of-order sequence can damage the DX-M1) and that the factory-provisioned DX-M1 firmware must not be replaced with stock DEEPX firmware.	October 2026
0.10	• Power Architecture: the DX-M1 power-sequencing note is now a hardware-damage warning (do not run the sequence from a Cortex-M33 image, a Linux application, a custom boot loader or a bench tool; an uncoordinated PMIC writer or a rail enable driven before the sequence finishes can damage the DX-M1). • JTAG / SWD Debug: the DX-M1 is brought up by the RZ/V2N boot firmware, not autonomously.	October 2026
0.11	• Figures added in the pad-level interface style, drawn from the module netlist: block diagram, power architecture, power-up and reset timing, boot flow, JTAG / SWD header, Ethernet, PCIe multiplexer, CAN (standard build and PHY assembly option), SD card, MIPI DSI + backlight, MIPI CSI-2 + camera LDOs, PDM, antenna, memories and the minimum reference schematic. • Power Architecture, Power-Up & Reset Sequence: the RZ/V2N rails are sequenced by the Qorvo ACT88760 PMIC, which also drives PORn, with a Renesas DA9292 dual buck; the GD32 I/O MCU does not sequence the rails (it enables the camera LDOs). • SD_VDD_OUT is a switched 3.3 V supply, not a 1.8 / 3.3 V auto-switching rail; the SD signalling level is what switches. SD pull-ups are 47 kΩ (CMD, D0– D3), not 1 MΩ. • Antenna: one connected antenna pad (AR1, all bands); ANT_5GHz / ANT_6GHz are not connected; the on-module I-PEX connector (20579-001E) is fitted, and its RF feed (moved from AR1) is the assembly option. • Part references corrected to the netlist: Ethernet PHY RTL8211FI-VD-CG (was RTL8211FDI); NOR flash 512 Mbit QSPI (was 128 Mbit / size TBD); the security IC is an Infineon OPTIGA Trust M secure element, not a TPM 2.0.	October 2026

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Revision	Changes	Date
	• MODULE_STBY is pulled up to VDD_5V_IN (100 kΩ), not to 1V8. Features: the CAN PHYs are an assembly option (not fitted in the standard build). • eMMC capacities corrected from Gbit to GB (32 GB / 128 GB; the 128 GB part is EMMC128-TY29-5B111, 1 Tbit). Pin table: BOOT2 (X1) is the RZ/V2N MD_BOOT3 strap, not unconnected; BOOT3 (Y1) is also tied on the module to ACT88760 GPIO5. The reference debug header takes nRESET from PORn (Z1); JTAG_nRST (AL1) is the TAP reset. • Boot Modes, pin table, boot flow, minimum reference schematic and its component list: BOOT2 (X1) takes a 1 kΩ carrier pull-up to VIO_OUT (no pull-up on the module); BOOT3 (Y1) takes a 1 kΩ carrier pull-up to VIO_OUT for Cortex-A55 boot; the on-module ACT88760 GPIO5 on Y1 is an input (Hi-Z). • Boot straps: every strap (BOOT0–BOOT3) takes a 1 kΩ carrier resistor, a pull-up to VIO_OUT for 1 or a pull-down to GND for 0 (BOOT3: 1 kΩ pull-down for a Cortex-M33 boot). The BOOT0 / BOOT1 DIP-switch pull-downs are 1 kΩ (was 10 kΩ). The RZ/V2N internal pull-ups read an open strap as 1; carrier designs must not rely on them (pin table, Boot Settings, Boot Modes, Reference Schematic, minimum reference schematic and boot flow figures). • PCIe: the multiplexer is two PI3DBS12212A lane switches, one for the TX lanes and one for the RX lanes; port A (common) is the RZ/V2N, port B the DX-M1, port C the PCIE0 pads. SEL = 0 links the RZ/V2N to the DX-M1, SEL = 1 to the PCIE0 pads. The PCIe figure, block diagram and boot flow show these port roles. • Pin Diagram: the pin-out is redrawn in the top view, landscape (65 mm across, 45 mm down), in the frame of the alplab.ai pinout viewer: pad letters A–AR are the rows, top to bottom, pad numbers 1–64 the columns, left to right; A1 is top left, A2 right of A1, B1 below A1. Split into four quarters so that every pad name prints at 6 pt or more. The pad numbers in the pin tables are unchanged. • Pin Diagram: the module is drawn as a plain rectangle with four square corners. A1 is marked by the triangular pin-1 fiducial. • Reflow profile figure redrawn in the house style; all values unchanged. • Secure Element: stated the bus and address of the Infineon OPTIGA Trust M (BRD_I2C, 0x30). General Description: the module is built on the open E1M standard (was “open-source” form factor). • Recommended PCB Land Pattern: the land-pattern drawing replaces the placeholder (top view, A1 top left, corner pads A1, A64, AR1, AR64 marked, pad geometry detail), and the parameter table is filled from E1M-STD §5.1.2 / §5.1.3: 1.00 mm pitch, Ø0.40 mm round NSMD pads, Ø0.50 mm solder-mask opening, 1:1 Ø0.40 mm stencil aperture. The “Pad size (GND ring)” row is removed: E1M-X has one pad size. • Recommended PCB Land Pattern: new Courtyard row (2.0 mm clearance around the module outline everywhere, 69.0 × 49.0 mm) in the parameter table; the courtyard is drawn dashed and dimensioned on the land pattern, and the central cavity is labelled as the carrier cut-out (mounting option b). • Pin-1 fiducial: drawn in copper, the colour of the pads (was black), as a right triangle with its right angle towards the A1 corner, inside the module outline and clear of it: to scale in the land-pattern drawing (0.25 mm inset, 0.52 mm legs, E1M-STD §5.1.2); in the pad map in the outer corner of the A1 cell. The separate A1 label in the pad-map centre is removed. • Keep-Out Zones: the “clear of components taller than TBD mm” rule and the placeholder figure are replaced by the mounting rule: the module carries bottom-side components in its central cavity and is not placed directly on a carrier; it is mounted on a spacer PCB, or over a through cut-out in the carrier the size of the cavity (57.45 mm across × 39.45 mm down, R1.00, 3.775 / 2.775 mm from the left / top outline edges). New mounting figure: cavity dimensioned on the module outline (top view, to scale) and section A–A on a spacer PCB and over a carrier cut-out. The spacer is soldered on both faces, and under both options the carrier has no components inside the cavity outline. Spacer thickness and bottom-side component height remain TBD (E1M-STD §5.2). The RF note names the one antenna feed (was “the three antenna feeds”).	

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Revision	Changes	Date
	• Packaging: removed the Tape & Reel section (placeholder drawing and specification table); tape and reel is not offered. Tray packaging is unchanged. • Ordering Matrix: the CPU part number R9A09G056N44GBG#AC0 prints on one line (it ran into the LPDDR4X column), and the CPU, AP-core, RT-core, AI and temperature values span the rows of all three MPNs (the E1M-V2M102 / E1M-V2M103 cells were empty). • Renesas RZ/V2N MPU: the Renesas RZ/V2N block diagram (source: Renesas Electronics) replaces the placeholder figure; a note states that blocks marked (option) depend on the RZ/V2N part number.	
0.12	• Memory: eMMC is 4 GB (101) / 16 GB (102 / 103), 32 / 128 Gbit; the earlier 32 GB / 128 GB was wrong.	October 2026

0.13	• Block diagram:
	  ▸ pad names ANT_2.4GHz and BRD_I2C
	  ▸ secure element shown as OPTIGA Trust M (0x30)
	  ▸ Ethernet PHY RTL8211FI-VD-CG
	  ▸ AUDIO_CLK and CAN_STBY drawn as outputs
	  ▸ H.264 / H.265 in the SoC block.
		October 2026

0.14	• Release history: every entry formatted as a bullet list.	October 2026
0.15	• Layout: the Table of Contents heading and the Block Diagram heading are kept on the same page as their content.	October 2026
0.16	• Contact: contact@alplab.ai is the only contact address. • Memory sizes given in GB (Ordering Information, MPN decoder, Ordering Matrix and the Memories figure, including the DX-M1 LPDDR5X at 2 GB each): 101 = 4 GB LPDDR4X + 4 GB eMMC, 102 = 8 GB + 16 GB, 103 = 4 GB + 16 GB.	October 2026
0.17	• Reflow profile: figure redrawn from the measured E1M-AEN JTR1000 run (three thermocouples CH3, CH4, CH5 at their true time and temperature scale, with the 150 °C, 217 °C liquidus and 220 °C lines, the phase spans and a parameter box of the measured ranges); the text and caption state that it is the E1M-AEN measured profile, used as the recommended starting profile. • Reflow parameters (text, figure and table): measured time at or above 220 °C 56.5–60.0 s (was “about 60 s” above 217 °C), peak 240.9–244.3 °C (was 241–244 °C), soak 150–217 °C 70.5–73.5 s (was 70–74 s), preheat 30–150 °C 116.5–122.0 s, cooling slope from 220 °C −1.53 to −1.66 °C/s (was about −1.6 °C/s), over the three thermocouples. • Reflow parameters table: recommended window from the profiler report beside the measured values: preheat 30–150 °C 60–160 s (new), soak 150–217 °C 60–120 s (unchanged), at or above 220 °C 45–90 s (was “time above liquidus (≥217 °C)” 45–90 s), cooling from 220 °C −4 to −0.5 °C/s (was average ramp-down T_P to T_L min −1.6 °C/s), peak 230–250 °C (was 241–244 °C); the ramp-up (max 3 °C/s) and time 25 °C to peak (max 8 min) rows removed (not in the measurement report).	October 2026
0.18	• Reflow profile figure: one measured curve (was three traces), with its phase spans and values (preheat 30–150 °C 116.5 s, soak 150–217 °C 71.5 s, at or above 220 °C 60.0 s, cooling from 220 °C −1.53 °C/s, peak 242.9 °C) and no legend; caption “Recommended starting profile: measured reflow profile of the E1M-AEN”. • Reflow parameters table: the measured column is headed “Measured” (the ranges are unchanged).	October 2026
0.19	• Block diagram: the JTAG line no longer runs through the PCIe mux box; the PCIe mux sits below the JTAG / SWD row. • Boot flow figure: each BOOT0–BOOT2 strap line ends at the next junction of the strap bus, so no two lines overlap (the drawing looks the same).	October 2026
0.20	• Table of Contents: each entry links to its section; the front-matter lists are set tighter. • Page 1: the Applications section is back on the first page (smaller module photos); the Features and Applications headings are unnumbered.	October 2026

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Revision	Changes	Date
	• Reflow figure: measured E1M-AEN profile, smoothed, without its zone-boundary kink (was the measured trace with that kink); caption “Recommended starting profile: measured E1M-AEN profile, smoothed”. • DX-M1 block diagram added (was a placeholder): PCIe interface, CPU, three NPU cores, system bus and two 2-channel LPDDR5X controllers, with the PCIe Gen3 x2 link to the RZ/V2N through the PCIe mux and 2 × LPDDR5X, 2 GB each. • Reflow parameters: the ramp-down slope (−1.53 to −1.66 °C/s) is the slope at or above 220 °C, from the peak down to 220 °C (was labelled “cooling from 220 °C”).	
0.21	• Product name: the on-module accelerator is named DeepX DX-M1 (was DeepX M1) in the PCIe feature line, the B47 pin note, the product-line row and the Ordering Information AI column.	October 2026
0.22	• Hardware revision R3 (module netlist export 15) carried into the datasheet. • Power & Control Pins: new rows for the row-3 module signals AD3 RTC_WAKE_N (open drain), AI3 PMIC_GPIO5_10V, AK3 / AL3 / AM3 M1_BOOT0–M1_BOOT2 (on-module 10 kΩ pull-downs fitted, pull-ups not fitted); these pads are removed from the Not-connected Pins table, with a note that the E1M-X standard still lists AD3–AP3 as NC. • Hardware-damage warning: 10 V on AI3 only with the on-module 0 Ω link to BOOT3 removed (otherwise it reaches the RZ/V2N BOOTSELCPU input and destroys the RZ/V2N); AI3 is the same node as BOOT3 (Y1) in normal use. BOOT3 row and Boot Modes text name the link. • Back-power warning: a carrier pull-up on M1_BOOT0–M1_BOOT2 only from a rail that is off whenever M1_VDD_1V8 is off. • Digital Pins: AO3 / AP3 are GP_I2C.SCL / GP_I2C.SDA (3.3 V, open drain, 4.7 kΩ pull-ups to +3V3_AON on the module); warning: no carrier pull-ups, pads high-impedance whenever module 5 V is absent. • Digital Pins: the GD32 pads (PWM0–PWM7, ENC0–ENC3, GD32 GPIO pads) have no series resistors on the module. • New DX-M1 GPIO Pads table: the DX-M1 ball behind each M1_G0.0–M1_G0.13 net, with a back-power warning against carrier pull-ups on these pads. • Reserved Pins: AE62, AL62–AR62 are not connected on the module. • Not-connected Pins: D63 is tied to 0V on the module (to be confirmed). • Power & Control Pins: MODULE_EN, MODULE_STBY and PORn describe the R3 front end (on-module clamps, 1 MΩ pull-ups to +1V8_AON, carrier drive 1.8–5 V or open drain; PORn open drain at 1.8 V, no carrier pull-up); MODULE_STBY is no longer pulled up to VDD_5V_IN. • +S_CAP feeds the RTC backup input directly; the module has no backup capacitor of its own. • Power Architecture: three power domains; the always-on domain carries the always-on 3.3 V and 1.8 V LDOs, the RTC with its +S_CAP backup input and the programmable power controller (behaviour and design values of the v2n_ctl_v1 image). • New Power Controller and RTC section: the RTC (RV-3028-C7, GP_I2C 0x52, from +3V3_AON) together with the power controller (0x08); RTC_INT_N, RTC_WAKE_N and RTC_ALARM (read by RZ/V2N PA7 and GD32 PC14). • New RTC Backup section: backup only from the carrier +S_CAP. • New Firmware Self-Off section: power-controller register 0x7A, OFF_ARM then OFF, 0x7A = 0x00 on every boot. • New DX-M1 Power Sequencing section: the power controller sequences the DX-M1 rails on M1_PWR_REQ; DX-M1 reset released only after VDDQ on plus 4 ms. • Warning: never set the power controller’s lock bit, issue its soft reset or write its NVM or register 0xC7 from the application. • Warning: enable the clock generator DIFF1 (0x69) only while the DX-M1 rails are up. • The DX-M1 power warning now describes the power-controller sequence (was the U-Boot PMIC sequence) and no longer quotes a PMIC default voltage.	November 2026

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Revision	Changes	Date
	• Power-Up & Reset Sequence: hold MODULE_EN low at least 150 ms before removing 5 V (was: no controlled power-down needed). • Boot Modes: new DX-M1 Boot Straps section (M1_BOOT0–M1_BOOT2 on AK3–AM3, default 0); the DX-M1 no longer has "no carrier-visible boot configuration". • Reset & Module Enable renamed Reset, Module Enable & Power Control: new Control Pins section with the MODULE_EN / MODULE_STBY front end and timing (design values), PORn and RTC_WAKE_N. • PCIe: reference clock from the clock generator DIFF1 through the reference-clock buffer to PCIE0_CLK and the DX-M1 (shared output, common clock with DIFF2 to the RZ/V2N); no second carrier reference clock; the PCIE0 slot has a reference clock only while the DX-M1 is powered. A47 pin row updated. • I^2C: new On-Module I^2C Buses table (GP_I2C: power controller 0x08, RTC 0x52; BRD_I2C: DA9292 0x1E, TPS628640 bucks 0x44 / 0x4F / 0x48, clock generator 0x69, secure element 0x30, temperature sensor 0x40, GD32 0x70). • New Clocks section with the clock-generator clock tree, including SE1 to WL_32K. • Pin-out figure (bottom left): AD3, AI3, AK3–AM3, AO3 and AP3 labelled with their module signals (were NC). • Figures redrawn: block diagram and power architecture (one "Power controller + RTC" box in the always-on domain with its MODULE_EN, MODULE_STBY, PORn, GP_I2C, RTC_WAKE_N, RTC_CLKOUT and +S_CAP pads; M1_BOOT[0:2]; no on-module RTC backup capacitor; buck enables from VDD1G_1P8), power-up and reset timing, boot flow and PCIe (clock generator). • RTC Backup: with a non-rechargeable backup cell on +S_CAP, firmware keeps the RTC trickle charger disabled. • DX-M1 firmware warning: recovery uses the DX-M1 boot straps on the carrier pads AK3–AM3 (was "a boot-strap change on the module"). • On-module parts named by function; component designators removed, also in the Release History rows.	
0.23	• Older Release History rows no longer quote a PMIC default voltage.	November 2026

Table 34 Revision History

19 Legal Notices

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19.4 Contact

For sales, technical support, or custom-variant requests:

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