ALP LAB

E1M-X V2N-M1 HW Design Guide

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Release History

Revision	Changes	Date
0.1	• Initial draft.	May 2026
0.2	• Interface ESD/EMI protection moved to the carrier board (Ethernet, MIPI CSI, MIPI DSI); on-module protection retained only on the SD-card interface.	June 2026
0.3	• Added `E1M-V2M103` (32 Gbit LPDDR4X + 128 Gbit eMMC 5.1 + DX-M1) to the supported variants and the pre-power check. • PCIe: removed the I/O-expander routing instructions (`I2C0` `0x21`, register `0x07`, bit 2) and the `alp_pcie_select()` API, neither of which exists in Alp SDK™ v0.17.0; the on-module multiplexer is module-internal and is routed to the DX-M1 by U-Boot on the Cortex-A55, together with the DX-M1 rail and reset release. • Software Support: replaced the non-existent `alp_e1m_v2n_m33_io` / `alp_e1m_v2n_m33_rt` / `alp_e1m_v2m_a55` board targets with the per-SKU Yocto `MACHINE`s and `alp_e1m_v2m101_m33_sm/r9a09g056n48gbg/cm33`; the GD32 supervisor is Alp Lab-programmed bridge firmware, not a customer build target. • Bring-Up Checklist: the DX-M1 enumerates as PCIe `1ff4:0000` (not `0x1c3c:0x0001`); replaced the non-existent `deepx-hello-world` example with the `dxrt-cli -s` check and a first inference with DEEPX's `run_model` on the A55 Yocto image (`examples/v2n/`	October 2026

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Revision	Changes	Date
	`v2n-m1-deepx-inference` is a Cortex-M33 image and runs no DX-M1 inference on silicon). • Power Design Guidelines and Boot: the DX-M1 rail is brought up by U-Boot on the Cortex-A55, not by the GD32 supervisor with the SoC rails; added a warning against re-implementing that sequence (it can bring the 0.75 V DX-M1 core rail up at the wrong voltage). • On-Module Memory and DX-M1 model deployment: the DX-M1 SPI NAND holds the factory-provisioned DX-M1 firmware, not models; added a warning against updating it with stock DEEPX firmware. Removed the unverified “factory-loaded model-zoo vs blank companion NAND” ordering option. • AI Acceleration: the SDK has no cross-accelerator scheduler; one `<alp/inference.h>` handle per backend, and `ALP_INFERENCE_BACKEND_AUTO` resolves to the DX-M1. PCIe: the stock image routes the lanes to the DX-M1 on every boot, so a carrier `PCIE0_*` device is not reachable with it.	
0.4	• Power Design Guidelines: added a warning that the DX-M1 rail and reset are owned only by U-Boot (Renesas DA9292 CH2, fixed sequence, no other PMIC writer). • Boot: expanded the re-implementation warning to a hardware-damage hazard covering all other software and replacement boot loaders.	October 2026
0.5	• Figures: replaced the four placeholder figures with drawings from the module netlist and the E1M-X development board netlist: module block diagram, 5 V buck converter, carrier reference block diagram and PCIe multiplexer. • Carrier-Board Reference Block Diagram: the DX-M1 GPIOs are wired to the pads IO0– IO6, IO17– IO22 and IO24 (not connected on V2N); the DX-M1 is not fully encapsulated. • PCIe routing rules: `PCIE0_TX0` / `PCIE0_TX1` are AC-coupled on the module; `PCIE0_CLK` is a module output. • Key characteristics: the on-module CAN transceivers are not fitted (the CAN pads carry the CAN-FD TX / RX logic signals, the carrier adds the transceivers); power management names the on-module PMIC and regulator. Design checklist: CAN transceiver added. • SPI NOR flash corrected to 512 Mbit (was 128 Mbit). • Release History: the 0.4 row is now shown inside the table (its text is unchanged). • PCIe: the RZ/V2N reaches the DX-M1 and the `PCIE0_*` pads through two `PI3DBS12212AXUAEX` multiplexers, one for the TX lanes and one for the RX lanes: port A (the common port) to the RZ/V2N, port B to the DX-M1, port C to the pads; `SEL` low links the RZ/V2N to the DX-M1, `SEL` high to the pads, and `PD` high puts both multiplexers in high impedance. The PCIe multiplexer figure names the port roles and adds the level translator on `SEL` / `PD` and the DX-M1 TX AC coupling. • Boot: carrier strap on `BOOT3` (Y1), a 1 kΩ pull-up to `VIO_OUT` for a Cortex-A55 boot, and a 1 kΩ pull-up to `VIO_OUT` on `BOOT2` (X1), which has no pull-up on the module; shown in the carrier reference block diagram and the design checklist. • Boot straps: every strap (`BOOT0`–`BOOT3`) takes a 1 kΩ carrier resistor, a pull-up to `VIO_OUT` for 1 or a pull-down to GND for 0 (`BOOT3`: 1 kΩ pull-down for a Cortex-M33 boot). The `BOOT0` / `BOOT1` DIP-switch pull-downs are 1 kΩ. The RZ/V2N internal pull-ups read an open strap as 1; carrier designs must not rely on them (Boot, carrier reference block diagram, design checklist). • Mechanical Information and Design Checklist: a module is never placed directly on a carrier; it is mounted on a spacer PCB (soldered on both faces: module to spacer, spacer to carrier) or over a carrier cut-out the size of the central cavity (57.45 mm across × 39.45 mm down, R1.00, 3.775 / 2.775 mm from the left / top outline edges), as its bottom-side components sit in the cavity; under both options the carrier has no components inside the cavity outline. The sentence “no carrier-side cutout is required” is withdrawn. The datasheet reference names the Mechanical & Footprint Dimensions section (it cited §13; that section is §14 of DS-V2N-M1-001).	October 2026

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Revision	Changes	Date
	• Dimensions: the height-class statement (standard height, E1M Spec §5.2.1) is replaced by the mounting rule (a module is mounted on a spacer PCB or over a carrier cut-out the size of the cavity) and the 2.0 mm courtyard (69.0 × 49.0 mm).	
0.6	• Document status: the title page now reads Preliminary, matching the running header (it read Draft).	October 2026
0.7	• Release history: every entry formatted as a bullet list.	October 2026
0.8	• Memory sizes given in GB (supported-variants table, memory list, pre-power check): `101` = 4 GB LPDDR4X + 4 GB eMMC, `102` = 8 GB + 16 GB, `103` = 4 GB + 16 GB.	October 2026
0.9	• Table of Contents: each entry links to its section; the front-matter lists are set tighter.	October 2026
0.10	• Product name on page 1 links to the product page on alplab.ai.	November 2026
0.11	• Hardware revision R3 (module netlist export 15) carried into the guide, consistent with DS-V2N-M1-001 0.22. • PCIe routing rules: `PCIE0_CLK` comes from the on-module reference-clock buffer, fed by the clock-generator `DIFF1` output that also clocks the DX-M1 (common clock with `DIFF2` to the RZ/V2N); no second carrier reference clock; the carrier slot has a reference clock only while the DX-M1 rails are up. Warning: the firmware enables `DIFF1` only with the DX-M1 rails up. • New Row-3 Module Pads section: carrier rules for `AD3` (`RTC_WAKE_N`), `AI3` (`PMIC_GPIO5_10V`), `AK3–AM3` (`M1_BOOT0–M1_BOOT2`) and `AO3` / `AP3` (`GP_I2C.SCL` / `GP_I2C.SDA`): what the carrier may connect and at which level; the `AI3` programming procedure only with the on-module 0 Ω link to `BOOT3` removed (hardware-damage warning); the `M1_BOOT` back-power warning; no carrier pull-ups on `GP_I2C`. • New Power Controller and RTC section: the always-on domain (`+3V3_AON`, `+1V8_AON`, the on-module RTC and the programmable power controller on `GP_I2C`, RTC backup from the carrier `+S_CAP`), the `MODULE_EN` / `MODULE_STBY` / `PORn` carrier drive, the 150 ms `MODULE_EN` rule before removing 5 V, and the warning against setting the power controller's lock bit, its soft reset, or writing its NVM or register `0xC7`. • Power Design Guidelines and Boot: the DX-M1 rails are sequenced by the on-module power controller on request from U-Boot (`M1_PWR_REQ`); the DX-M1 reset is released only after VDDQ is on, plus 4 ms. The DX-M1 rail warnings describe this sequence (was the U-Boot PMIC sequence) and no longer quote a PMIC default voltage. The PMIC sequences the RZ/V2N rails (was the GD32 supervisor). • Boot: `BOOT3` reaches the PMIC `GPIO5` and pad `AI3` through an on-module 0 Ω link; strap `BOOT3` on `Y1` only. The DX-M1 boot straps `M1_BOOT0–M1_BOOT2` default to 0. • Key characteristics: the PMIC is named by function; the programmable power controller and the on-module RTC are listed. • DX-M1 GPIO pads (IO0– IO6, IO17– IO22, IO24): no carrier pull-ups (Design Philosophy back-power warning, design checklist). Release History row 0.3 no longer quotes a PMIC default voltage. • Design checklist: rows for the row-3 module pads, `GP_I2C` and the DX-M1 GPIO pads. • PCIe multiplexer figure: on-module parts labelled by function; the reference-clock path is shown from the clock generator through the buffer. • Block diagram and carrier reference block diagram redrawn: the power block carries the power controller and the RTC (always on), with the `RTC_WAKE_N` (`AD3`) and `GP_I2C` (`AO3` / `AP3`) pads and `MODULE_STBY`; the GD32 no longer sequences the power rails. • On-module parts named by function; component designators removed, also in the Release History rows.	November 2026

Table 1 Release History

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1 Introduction

1.1 Purpose of This Document

This guide provides practical guidance for developers and system integrators using the **E1M-X V2N-M1 System-on-Module (SoM)**.

It covers:

- Hardware integration and carrier-board design
- Power architecture and system bring-up
- Interface usage and pin functional intent
- DeepX DX-M1 bring-up + PCIe multiplexing
- Common pitfalls during first implementation

This guide complements:

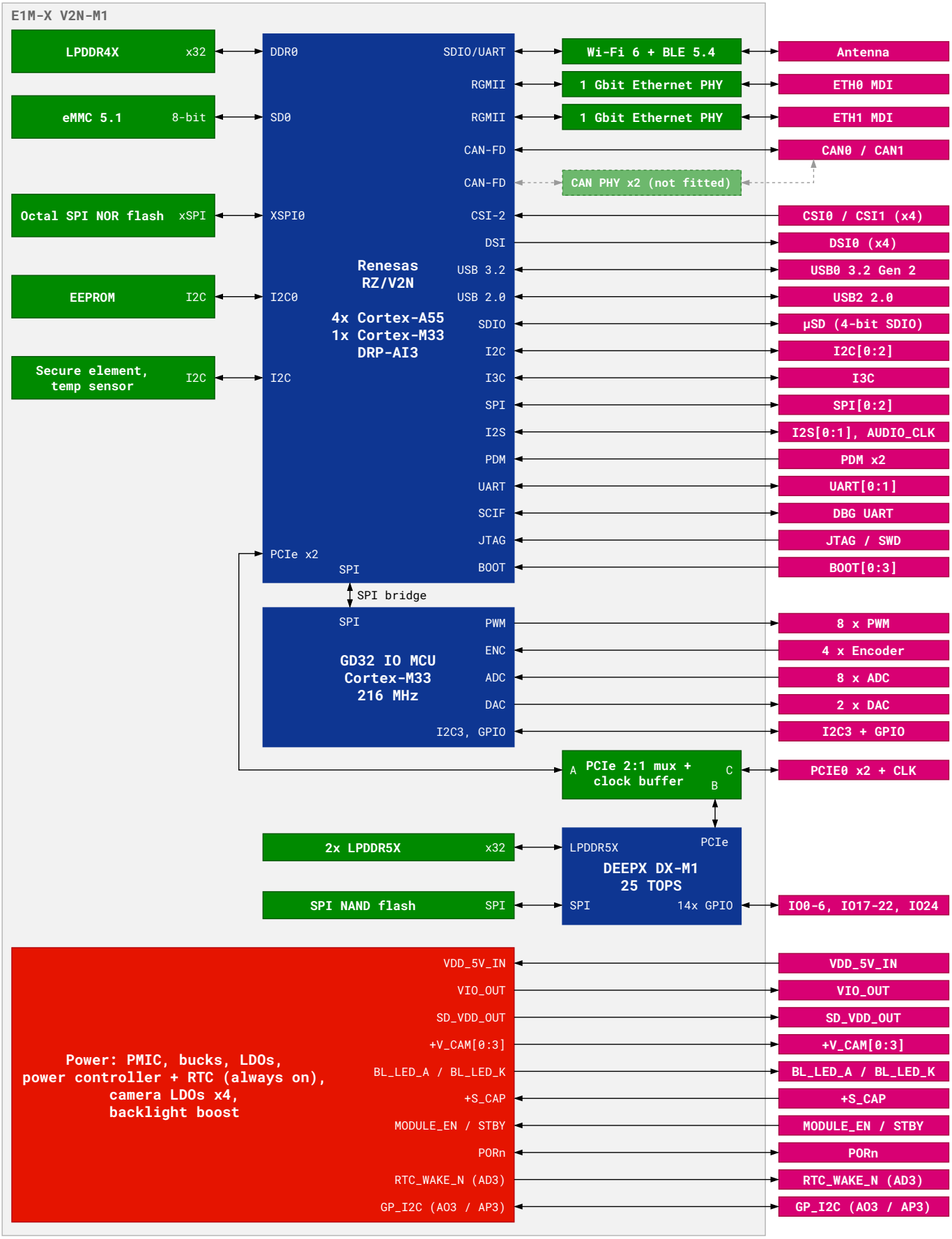
- The **E1M-X V2N-M1 Datasheet** (DS-V2N-M1-001)
- The **E1M-X V2N HW Design Guide** (HG-V2N-001) — the V2N-family rules apply unchanged to V2N-M1 except where §6.7 below diverges
- The **Renesas RZ/V2N** hardware reference manual and PCB design guidelines
- The **DeepX DX-M1** hardware integration manual
- The **E1M Specification** (E1M-STD-1.0) for form-factor and pinout requirements
- The **Alp SDK™** documentation

1.2 Product Overview

The **E1M-X V2N-M1** is a compact **45 × 65 mm Edge-AI System-on-Module** that pairs the **Renesas RZ/V2N** vision-AI MPU with the **DeepX DX-M1** standalone AI accelerator on a single SoM. It targets heavy-inference workloads (multi-camera object detection, LLM-class inference, model ensembles) that exceed the 4 TOPS budget of the V2N's internal DRP-AI3.

The module follows the **E1M-X™ open-standard pin layout** and is **pin-compatible with the V2N family**, so customers can prototype on V2N and upgrade to V2N-M1 without redesigning the carrier board.

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Dashed: not fitted (on-module CAN PHYs); 0 Ω links put the 1.8 V CAN-FD TX / RX logic signals on the
CAN pads instead. Memory sizes per SKU. Arrowheads mark the receiving end (both ends: bidirectional).
The power controller is the only driver of the PMIC enable; it and the RTC sit on the always-on GP_I2C.
PCIe x2 goes through the on-module mux (A common): SEL low A-B (DX-M1), SEL high A-C (PCIE0 pads),

Figure 1 E1M-X V2N-M1 Block Diagram

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Key characteristics:

- Unified E1M-X pinout, drop-in compatible with E1M-X V2N
- Quad Cortex-A55 @ 1.8 GHz + Cortex-M33 @ 200 MHz application + real-time cluster
- Renesas DRP-AI3 (4 TOPS) **plus** DeepX DX-M1 (25 TOPS) AI accelerators in parallel
- 2 × LPDDR5X companion memory for the DX-M1
- SPI NAND companion storage for the DX-M1
- Arm Mali-C55 ISP + Mali-G31 GPU
- On-module 1 Gbit Ethernet PHYs (× 2) and Wi-Fi 6 + BLE 5.4 combo; 2 × CAN-FD on the pads (logic level, the carrier adds the transceivers)
- On-module power management (PMIC, Renesas DA9292 regulator, programmable power controller with the on-module RTC in an always-on domain) plus GD32 supervisor MCU
- Single external **5 V supply**
- Long-term lifecycle orientation

2 Supported SoC Variants

SKU	Renesas Part	LPDDR4X	eMMC	AI capability
E1M-V2M101	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 4 GB	V2N: 4 TOPS DX-M1: 25 TOPS
E1M-V2M102	R9A09G056N44GBG#AC0	8 GB	eMMC 5.1, 16 GB	V2N: 4 TOPS DX-M1: 25 TOPS
E1M-V2M103	R9A09G056N44GBG#AC0	4 GB	eMMC 5.1, 16 GB	V2N: 4 TOPS DX-M1: 25 TOPS

Table 2 V2N-M1-family SKUs

All three SKUs share identical pinouts and silicon outside of the memory tier; carrier boards designed against one SKU work unmodified with the others.

3 Mechanical Information

3.1 Dimensions

- **Size:** 45 × 65 mm
- **Form factor:** Connectorless, solder-down LGA SoM
- **Courtyard:** 2.0 mm clearance around the module outline, 69.0 × 49.0 mm
- **Mounting:** never directly on the carrier. The module carries components on its bottom side, in the central cavity inside the pad band; mount it on a spacer PCB (soldered on both faces: module LGA to spacer, spacer to carrier), or over a through cut-out in the carrier the size of the cavity: 57.45 mm across × 39.45 mm down, R1.00 corners, 3.775 mm from the left and 2.775 mm from the top outline edge. With either option the carrier has no components inside the cavity outline. Spacer thickness and bottom-side component height: TBD.

The DX-M1 + LPDDR5X + SPI NAND additions to the V2N stack are all top-side components. The module carries components on its bottom side, in the central cavity, so it needs a spacer PCB or a carrier cut-out (see **Mounting** above).

For the full mechanical drawing including land pattern, keep-out zones and the mounting figure, see the **E1M-X V2N-M1 Datasheet** (DS-V2N-M1-001), Mechanical & Footprint Dimensions.

3.2 Handling and Assembly

- ESD-sensitive device. Use grounded handling equipment.
- Avoid mechanical stress after soldering.

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- Follow IPC J-STD-020 reflow profile (see DS-V2N-M1-001 §11.2).
- Maintain PCB flatness; warpage > TBD µm may compromise BGA solder joints under both the SoC and the DX-M1.

4 Power Architecture

4.1 Power Input

- **Input voltage:** 5 V DC, single rail on VDD_5V_IN
- All regulators, the PMIC, and sequencing are on-module
- No additional power rails must be supplied by the carrier

> **Warning:** Do **not** attempt to power individual rails (VIO_OUT, SD_VDD_OUT, etc.) externally. These pads are **outputs** from the module; sourcing them externally will fight the on-module regulator and may damage the PMIC.

4.2 Power Design Guidelines

- Place bulk capacitance (≥ 10 µF) near the 5 V input
- Use a solid ground plane covering the entire SoM footprint
- Keep high-current paths short and wide
- Nominal input voltage: 5.0 V; recommended tolerance: ±5%
- Connect **every** GND pad on the SoM to a low-impedance plane (105 pads on E1M-X)
- No external sequencing required; the on-module PMIC sequences the RZ/V2N rails once the power controller enables it. The DX-M1 rails are not part of that power-up sequence: the power controller sequences them later, on request from the RZ/V2N boot firmware (U-Boot on the Cortex-A55), see **§Boot**

> **Warning:** **DX-M1 rails and reset are not owned by the GD32 supervisor.** On V2N-M1, U-Boot on the Cortex-A55 requests the DX-M1 rails on M1_PWR_REQ, and the on-module power controller sequences them (core, NPU, VDD1, VDD2H, then VDDQ). U-Boot releases the DX-M1 reset only after the power-controller status register shows VDDQ on, plus 4 ms, and routes the PCIe multiplexer. Nothing else may drive the DX-M1 power sequence or the DX-M1 reset, or write the on-module PMIC: a second, uncoordinated PMIC writer can damage the DX-M1. See **§Boot**.

> **Note:** The V2N-M1 has measurably higher peak power than the V2N at the same workload because the DX-M1 + companion LPDDR5X + SPI NAND draw additional current during inference. Size the carrier supply for ≥ 5 A peak.

4.3 Power Controller and RTC

The module has an always-on domain, alive whenever VDD_5V_IN is present and independent of MODULE_EN: an always-on 3.3 V rail (+3V3_AON), an always-on 1.8 V rail (+1V8_AON, fed from +3V3_AON), the on-module RTC (RV-3028-C7) and the programmable power controller. The power controller is the module power latch, the self-off and wake logic and the DX-M1 / LPDDR5 power sequencer, and it is the only driver of the PMIC enable. The RTC (0x52) and the power controller (0x08) sit together on the always-on GP_I2C bus, which is also on pads AO3 / AP3 (**§Row-3 Module Pads**). The RTC interrupt wakes the module through the power controller and drives RTC_WAKE_N (AD3). The RTC backup input is the carrier +S_CAP pad (AQ25); the module has no backup capacitor of its own, so connect the carrier backup super-capacitor there. For the behaviour and the design timings of the v2n_ctl_v1 power-controller image see DS-V2N-M1-001, Power Controller and RTC.

- MODULE_EN (AA1) and MODULE_STBY (AB1) reach the power controller through on-module clamps (1 MΩ pull-ups to +1V8_AON behind the clamps). Drive them with an open-drain output and no pull-up, a switch to GND, or push-pull logic from 1.8 V to 5 V. Keep the carrier leakage on each pad at ≤ 0.1 µA, including ESD parts. Leave them floating if not used.
- PORn (Z1) is open drain at 1.8 V (10 kΩ pull-up to VDD1G_1P8 on the module). The carrier may pull it low to reset the RZ/V2N with the rails kept up. No carrier pull-up.
- Hold MODULE_EN low at least 150 ms before removing 5 V. Removing 5 V with the module on is for recovery only.

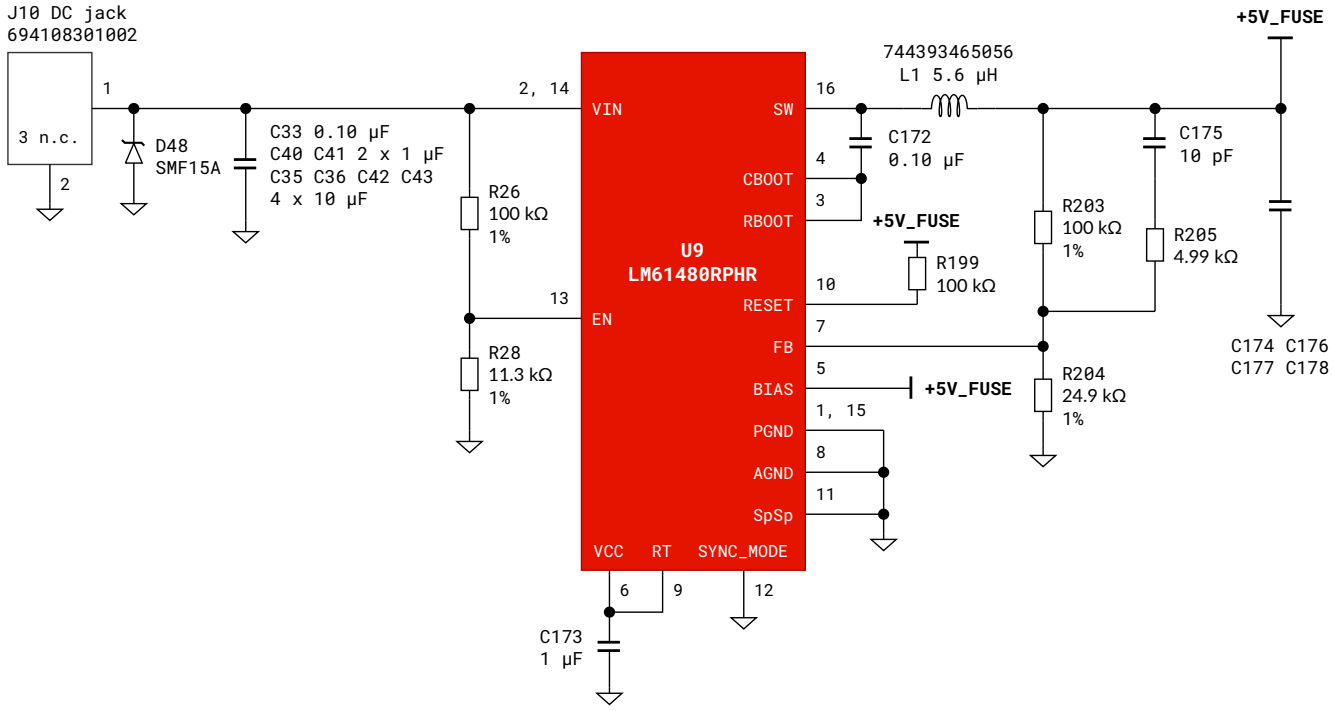
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- With a non-rechargeable backup cell on +S_CAP, firmware keeps the RTC trickle charger disabled.

> **Warning:** Never set the power controller's lock bit, never issue its soft reset, and never write its NVM or register `0xC7` from the application. Each of these takes every power-controller output high-impedance: the module powers off uncontrolled, and every DX-M1 rail is cut at once (an uncontrolled LPDDR5 power-off).

4.4 Carrier-Board 5 V Generation

A buck converter is the recommended way to generate the 5 V rail from the carrier-board input voltage. Choose a converter rated for transients up to **5 A** to cover worst-case AI (DRP-AI3 + DX-M1 in parallel) + dual-Ethernet + M.2 SSD activity simultaneously.



E1M-X development board. Capacitors drawn as one symbol are in parallel. Output: C174 0.10 µF, C176 / C177 10 µF, C178 100 µF 10 V polymer (875105242010). +5V_FUSE feeds the U11 eFuse (next figure). The U9 VIN node (J10 pin 1) is also fed from the USB-PD sink through D1 (next figure). RESET is pulled up and not used further.

Figure 2 V2N-M1 5 V buck-converter reference circuit (E1M-X development board)

Power-OR'ing using diodes or eFuses is supported. When multiplexed (e.g. between barrel jack and USB-PD on a carrier), use a unidirectional eFuse to avoid back-feeding the inactive source.

5 Memory and Boot Architecture

5.1 Internal Memory (SoC-Dependent)

- **On-chip SRAM:** 1.5 MB (RZ/V2N)
- **LPDDR4X DRAM:** 32-bit, 3.2 GT/s, up to 8 GB (per SKU)

5.2 On-Module Memory

- **eMMC 5.1** up to 16 GB (per SKU)
- **SPI NOR flash:** 512 Mbit, boot-supported (RZ/V2N boot path)
- **2 × LPDDR5X** companion memory for the DeepX DX-M1

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- **SPI NAND** companion storage for the DeepX DX-M1 (holds the DX-M1's factory-provisioned firmware)
- **I²C EEPROM:** optional, accessible via `I2C0`

> **Note:** The DX-M1 has its **own** memory subsystem (LPDDR5X + SPI NAND) that is not accessible from the carrier board. Loading models into the DX-M1 is a software-managed step from the RZ/V2N application cores via the PCIe link; see **§Software Support**.

5.3 Boot

The RZ/V2N samples four boot-strap pins at `PORn` release. The V2N-M1 boot flow is **identical to V2N** for the RZ/V2N itself. The DX-M1 does **not** come up with the SoC rails: in the Alp SDK™ Yocto image, U-Boot (on the Cortex-A55) requests the DX-M1 rails from the on-module power controller on `M1_PWR_REQ`, and the power controller sequences them. Once the power-controller status register shows VDDQ on, plus 4 ms, U-Boot routes the on-module PCIe multiplexer to the DX-M1 and releases it from reset, before Linux starts. The firmware enables the clock-generator `DIFF1` output, which clocks the DX-M1 and `PCIE0_CLK`, only while the DX-M1 rails are up. The DX-M1 then boots its factory-provisioned firmware from its SPI NAND.

The carrier boot straps are the same as on V2N: pull `BOOT2` (X1) up to `VIO_OUT` with 1 kΩ (the module has no `BOOT2` pull-up), and for a Cortex-A55 boot pull `BOOT3` (Y1) up to `VIO_OUT` with 1 kΩ (for a Cortex-M33 boot, pull it down to `GND` with 1 kΩ). `BOOT0` / `BOOT1` take a DIP switch to `VIO_OUT` with a 1 kΩ pull-down to `GND` on each line, or a 1 kΩ hard-strap. On the module `BOOT3` also reaches, through an on-module 0 Ω link, `GPIO5` of the PMIC, which is an input (high impedance), and pad `AI3` (`PMIC_GPIO5_10V`), so the carrier strap sets the level. Strap `BOOT3` on `Y1` only and leave `AI3` unconnected (**§Row-3 Module Pads**).

Strap every boot pin (`BOOT0`–`BOOT3`) on the carrier with a 1 kΩ resistor: a 1 kΩ pull-up to `VIO_OUT` for 1, a 1 kΩ pull-down to `GND` for 0. The RZ/V2N has internal pull-ups on its boot-strap pins, so a strap left open reads 1, but a carrier design must not rely on them.

The DX-M1 is not affected by the `BOOT*` pins. Its boot straps `M1_BOOT0`–`M1_BOOT2` are on pads `AK3`, `AL3` and `AM3`, each with a 10 kΩ pull-down on the module, so all three read 0 by default. Leave them floating for the default (**§Row-3 Module Pads**).

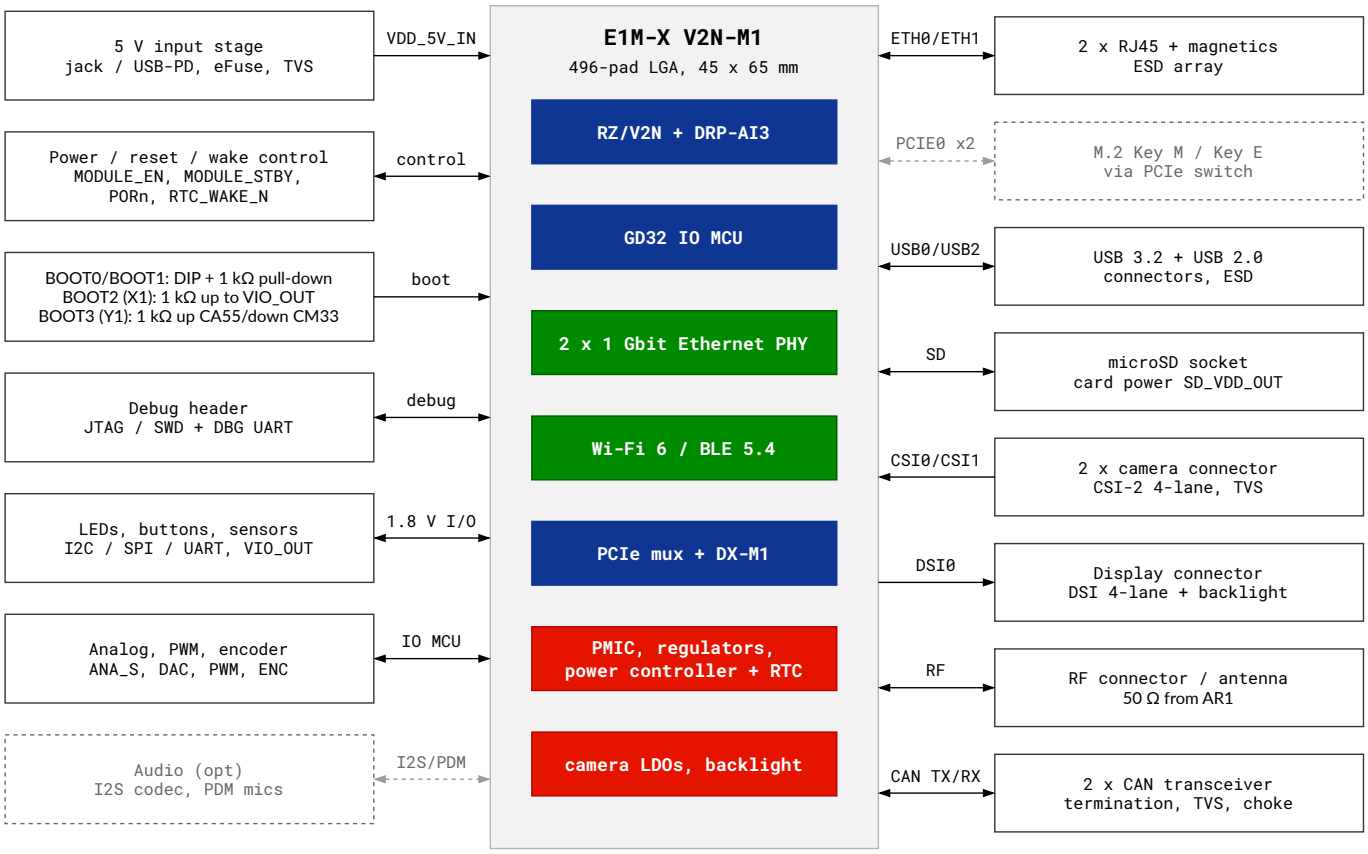
> **Warning:** Hardware-damage hazard. Keep this step in the Alp Lab-supplied U-Boot. Do not drive the DX-M1 power sequence or the DX-M1 reset from other software (a Cortex-M33 image, a Linux application, a custom boot loader or a bench tool), and do not write the on-module PMIC from it: a second, uncoordinated PMIC writer can damage the DX-M1. If you replace U-Boot, the replacement must request the rails on `M1_PWR_REQ`, release the DX-M1 reset only after the power-controller status register shows VDDQ on, plus 4 ms, and enable the clock-generator `DIFF1` only while the DX-M1 rails are up.

See the **E1M-X V2N-M1 Datasheet** (DS-V2N-M1-001) §4.1 for the full boot-mode truth table, and the **E1M-X V2N HW Design Guide** (HG-V2N-001) §6 for the carrier-side DIP-switch implementation.

6 Carrier-Board Reference Block Diagram

The carrier board has been designed for the **E1M-X** open standard. V2N-M1 routes the **same subset** of E1M-X pads as the V2N family, plus 14 DX-M1 GPIOs on the pads IO0– IO6, IO17– IO22 and IO24 (not connected on V2N). The DX-M1 PCIe link, memories and power are on-module.

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Dashed: optional (opt). The carrier provides the protection on every external interface except SD (on-module).
Arrowheads mark the receiving end (both ends: bidirectional). The module has no CAN transceiver fitted:
the carrier adds it.
PCIE0 x2: the stock Alp SDK image routes the PCIe lanes to the on-module DX-M1 on every boot.

Figure 3 Carrier-board reference block diagram for V2N-M1

6.1 System-Level Overview

Identical to the V2N family. See **HG-V2N-001** §5.

6.2 Design Philosophy

- Keep the carrier board simple and application-specific.
- **Reuse the V2N carrier design without changes.** The V2N-M1 is pin-compatible. Treat IO0– IO6, IO17– IO22 and IO24 as DX-M1 GPIOs on V2N-M1: do not drive them from the carrier unless the application uses them, and fit no carrier pull-ups on them (a pull-up back-powers the DX-M1 I/O while the DX-M1 rails are off).
- Pads AD3, AI3, AK3–AM3, AO3 and AP3 carry module signals, although the E1M-X standard lists them as NC; connect them only as **§Row-3 Module Pads** allows.
- Plan for higher peak power (≥ 5 A on the 5 V rail) and slightly higher thermal dissipation than V2N.

> **Warning:** Back-power hazard. Fit no carrier pull-ups on the DX-M1 GPIO pads (IO0– IO6, IO17– IO22, IO24). The DX-M1 I/O is powered only while the DX-M1 rails are up, and a carrier pull-up back-powers it while they are off.

7 Interfaces Overview

All interfaces are exposed through the standardised **E1M-X™ pinout**. The carrier-board rules in **HG-V2N-001** §6 apply unchanged for **every interface except PCIe**. This section gives a brief summary; for full details see the V2N HW Design Guide.

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> **Note:** See the **E1M-X V2N-M1 Datasheet** (DS-V2N-M1-001) and the **E1M Specification** (E1M-STD-1.0) for the canonical pad-list and pin-function mapping.

7.1 Ethernet, Wi-Fi/BLE, MIPI CSI/DSI, USB, CAN, Serial Buses, Audio, Analog, PWM, Encoder

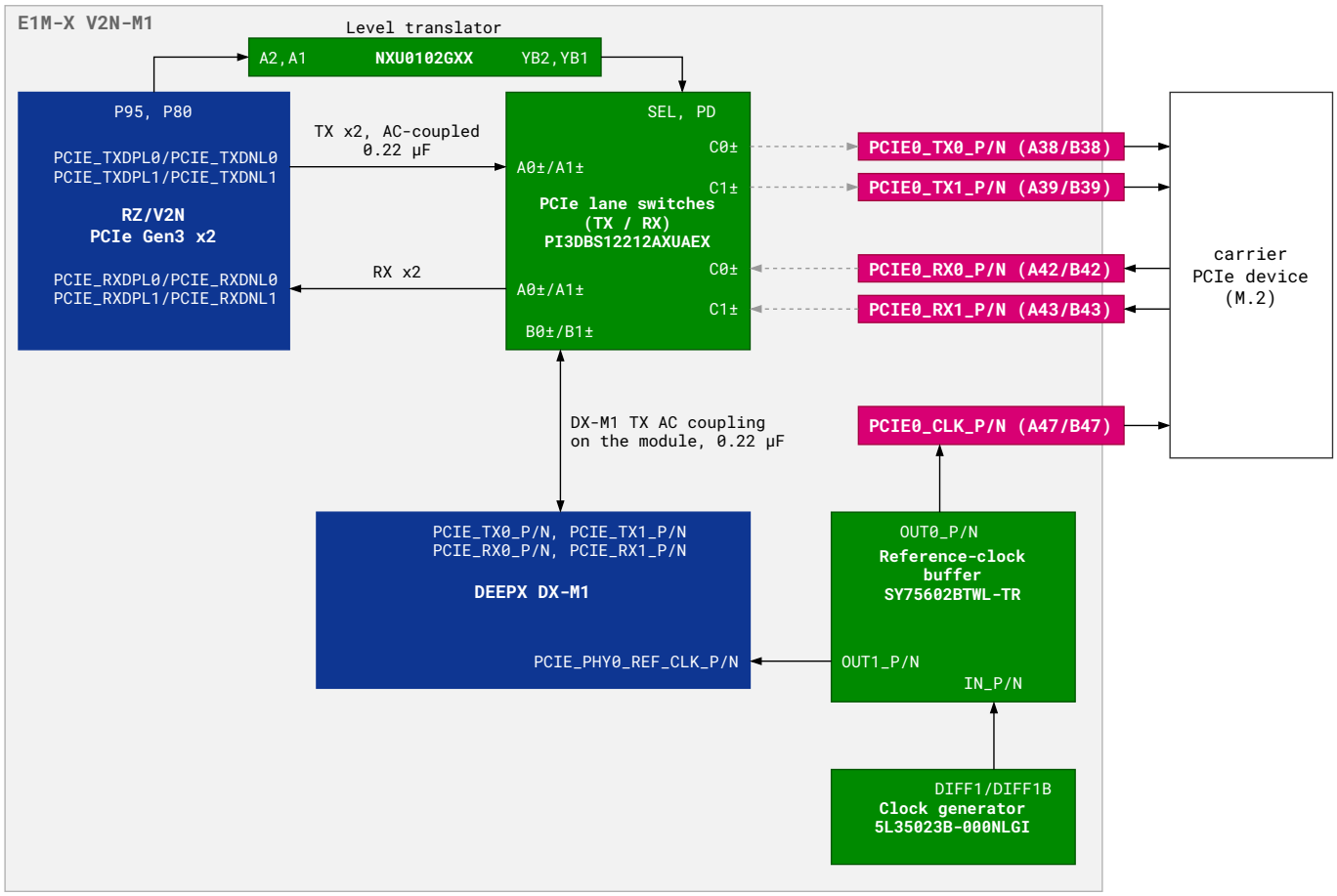
These interfaces are unchanged from V2N. Follow the rules in **HG-V2N-001** §6.1 – §6.10. The on-module components, routing requirements, and carrier-side ESD/EMI protection requirements are all identical (interface ESD/EMI protection is provided on the carrier board, except the SD-card interface which is protected on-module).

7.2 PCIe (V2N-M1 specifics)

This is the only interface where V2N-M1 design differs materially from V2N.

The RZ/V2N has **one** PCIe Gen3 × 2 controller. On the V2N-M1 SoM it reaches both the on-module DeepX DX-M1 and the `PCIE0_*` pads through two on-module `PI3DBS12212AXUAEX` 2:1 PCIe lane switches: one switches the TX lanes, the other the RX lanes. On both, port A connects to the RZ/V2N, port B to the DX-M1 and port C to the `PCIE0_*` pads. Port A is the common port: `SEL` low links the RZ/V2N to the DX-M1 (port B), `SEL` high links the RZ/V2N to the `PCIE0_*` pads (port C), and `PD` high puts all switches in high impedance. The lane switches are driven from RZ/V2N `P95` (`SEL`) and `P80` (`PD`) through an on-module level translator; an on-module 10 kΩ pull-up holds `PD` high and an on-module 10 kΩ pull-down holds `SEL` low; these control lines are not brought out to the E1M-X edge connector. In the Alp SDK™ Yocto image, U-Boot (on the Cortex-A55) routes it to the DX-M1 during boot, as part of requesting the DX-M1 rails from the power controller and releasing the DX-M1 from reset, before Linux starts.

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Port A (common) of the two 2:1 lane switches connects to the RZ/V2N, port B to the DX-M1, port C to the PCIE0 pads: SEL low links the RZ/V2N to the DX-M1, SEL high to the PCIE0 pads; PD high: all switches Hi-Z.
The level translator shifts P95 / P80 to SEL / PD; on-module 10 kΩ pull-up on PD (power-down), 10 kΩ pull-down on SEL.
Stock Alp SDK image: U-Boot on the Cortex-A55 sets SEL / PD and selects the DX-M1 on every boot; the port C links are then disconnected (dashed grey). PCIE0_TX0 / TX1 are AC-coupled on the module.
Clock generator DIFF1 / DIFF1B (33 Ω series) clocks the buffer, shared by the DX-M1 and PCIE0_CLK (a module output, running only while the DX-M1 rails are up). Arrowheads mark the receiving end (both ends: bidirectional).

Figure 4 V2N-M1 PCIe multiplexer block diagram

7.2.1 Routing rules

- Treat PCIE0_* exactly as in V2N: 85 Ω differential, lane-to-lane matching ±2 ps.
- PCIE0_TX0 / PCIE0_TX1 are AC-coupled on the module (0.22 µF); add AC coupling only on the PCIE0_RX* lanes, at the carrier device's transmitter.
- PCIE0_CLK is driven by the on-module reference-clock buffer (OUT0). The buffer is fed from the on-module clock-generator DIFF1 output, and its second output clocks the DX-M1, so the carrier PCIe device and the DX-M1 share one clock output; the RZ/V2N root complex uses DIFF2 of the same clock generator (common clock). Clock the carrier device from PCIE0_CLK and add no second reference-clock source.
- The firmware enables DIFF1 only while the DX-M1 rails are up, so on the V2N-M1 the carrier slot has a reference clock only while the DX-M1 is powered.
- The on-module mux adds < TBD ps of skew per lane – design margin TBD ps additional length-tuning allowance on the carrier compared to a direct connection.

Warning: Hardware-damage hazard. The reference-clock buffer has no output enable: while DIFF1 runs, it drives the DX-M1 reference-clock input. Enable DIFF1 (clock generator, I^2C 0x69) only while the DX-M1 rails are up; otherwise the buffer drives the unpowered DX-M1 input. Do not enable DIFF1 to clock a carrier PCIE0 device while the DX-M1 is off.

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7.2.2 Power and reset

- The DX-M1 has its own dedicated rails generated on-module; the carrier provides nothing extra.
- The DX-M1 resets when PORn is asserted to the SoC; no carrier-side reset is exposed for the DX-M1.

7.2.3 Routing ownership

The multiplexer is routed by the RZ/V2N boot firmware, not by a carrier-visible signal or an application API; application software does not switch it. Consult `docs/bring-up-v2n-m1.md` in the SDK for the full sequence.

Warning: Do **not** assume both endpoints can be active concurrently. The PCIe controller is single-instance; the multiplexer is exclusive. While the lanes serve the on-module DX-M1, the carrier `PCIE0_*` path is disconnected. The Alp SDK™ boot firmware routes the lanes to the DX-M1 on every V2N-M1 boot and exposes no API to switch them, so a carrier-side PCIe device on `PCIE0_*` is not reachable with the stock image.

7.3 Row-3 Module Pads

The E1M-X™ standard lists pads AD3–AP3 as NC. On the V2N-M1 module, AD3, AI3, AK3–AM3, AO3 and AP3 carry module signals (AE3–AH3, AJ3 and AN3 stay unconnected on the module). A carrier must not route its own nets through these pads; connect them only as below.

Pad	Signal	On the module	Carrier connection
AD3	RTC_WAKE_N	RTC wake output, active low, open drain (on-module transistor, driven from the RTC interrupt). Valid in every module state while 5 V is present.	Pull-up to a carrier always-on rail, ≤ 5.5 V, ≥ 10 kΩ. Leave unconnected if not used.
AI3	PMIC_GPIO5_10V	PMIC GPIO5, the PMIC in-circuit programming path (about 10 V). Joined through an on-module 0 Ω link to BOOT3 (Y1, RZ/V2N BOOTSELCPU): in normal use the same node as BOOT3.	Leave unconnected. Strap BOOT3 on Y1 only; a carrier that drives or straps AI3 also drives BOOT3. Programming: see below.
AK3 AL3 AM3	M1_BOOT0 M1_BOOT1 M1_BOOT2	DX-M1 boot straps (DX-M1 GPIO00_00 / GPIO00_01 / GPIO00_02), DX-M1 1.8 V I/O (M1_VDD_1V8). 10 kΩ pull-down on each (default 0); the 10 kΩ pull-up positions to M1_VDD_1V8 are not fitted.	Leave floating for the default (all 0). A carrier pull-up, for a non-default value set in an Alp Lab recovery procedure, only from a rail that is off whenever M1_VDD_1V8 is off.
AO3 AP3	GP_I2C.SCL GP_I2C.SDA	Always-on I^2C, 3.3 V, open drain: the power controller (0x08, also its programming port) and the RTC (0x52). 4.7 kΩ pull-ups to +3V3_AON on the module. While the module runs, on-module bus switches bridge it onto the 1.8 V on-module BRD_I2C.	No carrier pull-ups. Leave unconnected, or bring to a provisioning connector (3.3 V open-drain host) for programming the power controller with MODULE_EN held low. Keep both pads high-impedance whenever module 5 V is absent. Only the RZ/V2N addresses the power controller and the RTC in operation.

Table 3 Row-3 module pads: carrier connection

Warning: Back-power hazard. A carrier pull-up on M1_BOOT0–M1_BOOT2 (AK3–AM3) must come from a rail that is off whenever the DX-M1 I/O rail M1_VDD_1V8 is off; otherwise the DX-M1 I/O is back-powered through the pull-up. The module brings no rail that follows M1_VDD_1V8 out to the pads.

Warning: GP_I2C (AO3 / AP3): fit no carrier pull-ups (the module has 4.7 kΩ pull-ups to +3V3_AON), and keep both pads high-impedance whenever module 5 V is absent.

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7.3.1 PMIC programming through AI3

AI3 is the PMIC in-circuit programming path, which takes about 10 V. It is an Alp Lab provisioning and rework step, not a carrier function. The order is:

1. First, remove the on-module 0 Ω link that joins AI3 to BOOT3.
2. Then apply the programming voltage to AI3 (supply conditions and sequence: Alp Lab provisioning procedure, to be confirmed).
3. Whether the link is refitted after programming: to be confirmed.

Warning: Hardware-damage hazard. Apply 10 V to AI3 only with the on-module 0 Ω link to BOOT3 removed. With the link fitted, the 10 V reaches the RZ/V2N BOOTSELCPU input and destroys the RZ/V2N. In normal use AI3 is electrically the same node as BOOT3 (Y1).

8 Software Support

8.1 Alp SDK™

- Open-source, CMSIS-compliant
- Unified HAL across all E1M-X variants (V2N, V2N-M1, future SKUs)
- Vendor-agnostic software architecture

The SDK build targets for V2N-M1 are per SKU:

- RZ/V2N quad Cortex-A55 (1.8 GHz) — Linux via Yocto MACHINE `e1m-v2m101-a55` / `e1m-v2m102-a55` / `e1m-v2m103-a55`, **DX-M1-aware**: the DeepX driver and runtime layer is wired into these machines, not into the V2N-family `e1m-v2n10x-a55` machines
- RZ/V2N internal Cortex-M33 system manager (200 MHz) — Zephyr board target `alp_e1m_v2m101_m33_sm/r9a09g056n48gbg/cm33` on E1M-V2M101 (the E1M-V2M102 / E1M-V2M103 M33 board trees are not yet built)

The on-module GD32 supervisor (216 MHz) is not a customer build target: it runs bridge firmware that Alp Lab programs in production, reached from the RZ/V2N through `<alp/chips/gd32g553.h>` and updated in the field over the bridge link. Customer reflashing of the GD32 is supported only to recover a bricked module.

8.2 AI Acceleration

- Renesas DRP-AI3 (4 TOPS, integrated in the RZ/V2N)
- DeepX DX-M1 (25 TOPS, PCIe-attached on-module)
- Both accelerators can run at the same time: the application opens one `<alp/inference.h>` handle per backend (ALP_INFERENCE_BACKEND_DRPAI, ALP_INFERENCE_BACKEND_DEEPX_DXM1) and pins each model or stream to one of them. The SDK does not ship a cross-accelerator scheduler and does not split one inference graph across both. On a V2N-M1 build ALP_INFERENCE_BACKEND_AUTO resolves to the DX-M1, so a DRP-AI3 model must name its backend explicitly

8.2.1 DX-M1 model deployment

DeepX provides the **DX-COM™** tool which converts PyTorch / ONNX models into DX-M1-optimised executable code (`.dxnn`). Compiled models are stored on the RZ/V2N side (e.g. eMMC or SD card) and loaded by the RZ/V2N at runtime via the PCIe link into the DX-M1's companion LPDDR5X.

Warning: The on-module SPI NAND holds the DX-M1's **firmware**, an Alp Lab build for this SoM that is provisioned at the factory. It is not model storage. Do **not** update it with stock DEEPX firmware: that leaves the NPUs dead (`dxrt_polling_ack : timeout`), and recovery needs a boot-strap change on the module, which is not a field operation. The shipped `dxrt-cli` warns before its firmware-update (`-u`), firmware-upload (`-w`) and firmware-config (`-C`) options but does not block them; use them only with firmware supplied by Alp Lab for this module.

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9 Bring-Up Checklist

9.1 Pre-Power Checks

- Confirm the correct SoM variant (`E1M-V2M101`, `E1M-V2M102` or `E1M-V2M103`).
- Verify orientation and solder joints (A1 corner against carrier fiducial).
- Ensure only 5 V is connected to `VDD_5V_IN`.
- Check ground continuity across all 105 `GND` pads.
- Confirm DIP-switch state for the intended boot mode.

9.2 First Power-On

- Apply 5 V (recommend barrel jack; USB-PD also works).
- Monitor current consumption (expected idle: TBD mA; expect higher than V2N because of the DX-M1 supervisor power).
- Check for abnormal heating on the SoM — particularly over the DX-M1.
- Confirm `PWR` and `IO_EN` LEDs light within 100 ms.
- Open the console UART at 115 200 8N1 and watch for boot output.

9.3 Basic Validation

- UART boot / debug output on the SCIF console.
- Both Ethernet links coming up when cables are plugged in.
- GPIO or PWM toggle from a simple Zephyr build.
- `lspci` (on Linux) shows the DX-M1 enumerating as PCIe `1ff4:0000`, and `dxrt-cli -s` returns rc `0`.
- A first DX-M1 inference runs to completion on the A55 Yocto image, e.g. with DEEPX's `run_model` tool (installed in the `e1m-v2m10x-a55` image) and a `.dxnn` model built for the DX-M1 firmware version that `dxrt-cli -s` reports.

9.4 Common Issues

- Wrong DIP-switch position for the intended boot device (most common first-time failure).
- DX-M1 not enumerating because the boot firmware did not request the DX-M1 rails from the power controller, release its reset, or route the PCIe multiplexer to it – check the U-Boot log and `docs/bring-up-v2n-m1.md`.
- DX-M1 enumerating but inference failing because the model wasn't loaded – check `dxrt-cli -s` and `docs/bring-up-v2n-m1.md`.
- A55 image built for a V2N-family `MACHINE` (`e1m-v2n10x-a55`) instead of the module's `e1m-v2m10x-a55`; the DeepX driver and runtime are not in the image.
- Insufficient supply current under DRP-AI3 + DX-M1 + dual-Ethernet load.

10 Design Checklist (Summary)

Item	Status
Single 5 V supply, ≥ 5 A rated	OK
Bulk + decoupling capacitance close to `VDD_5V_IN`	OK
Ethernet magnetics + RJ45 on both ports	OK
Controlled-impedance MIPI and PCIe routing	OK
RF-clean antenna routing, ≥ 1 RF connector or PCB antenna	OK
CAN transceiver, termination + ESD on both CAN ports	OK
Every boot strap set by a 1 kΩ resistor (pull-up to `VIO_OUT` for 1, pull-down to `GND` for 0): `BOOT0` / `BOOT1` DIP switch with 1 kΩ pull-downs, or hard-strap; `BOOT2` (X1) 1 kΩ pull-up; `BOOT3` (Y1) 1 kΩ pull-up for CA55 boot or 1 kΩ pull-down for CM33 boot	OK

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Item	Status
PORn and MODULE_EN accessible (button or test-point)	OK
MODULE_EN / MODULE_STBY driven open drain, by a switch to GND or by 1.8 V to 5 V push-pull; leakage ≤ 0.1 µA per pad; no carrier pull-up on PORn	OK
AD3 RTC_WAKE_N: pull-up to a carrier always-on rail (≤ 5.5 V, ≥ 10 kΩ) or unconnected	OK
AI3 PMIC_GPIO5_10V unconnected; BOOT3 strapped on Y1 only; 10 V on AI3 only with the on-module 0 Ω link removed	OK
AK3–AM3 M1_BOOT0–M1_BOOT2 floating (default 0), or pulled up only from a rail that is off whenever M1_VDD_1V8 is off	OK
AO3 / AP3 GP_I2C: no carrier pull-ups; unconnected or to a 3.3 V provisioning connector; high-impedance whenever module 5 V is absent	OK
No carrier pull-ups on the DX-M1 GPIO pads (IO0– IO6, IO17– IO22, IO24)	OK
Carrier PCIE0 device clocked from PCIE0_CLK; no second reference-clock source	OK
Debug header on JTAG / SWD pins (optional but recommended)	OK
Module mounted on a spacer PCB (soldered on both faces), or over a carrier cut-out the size of the central cavity (57.45 × 39.45 mm, R1.00, 3.775 / 2.775 mm from the left / top outline edges); no carrier components inside the cavity outline; never directly on the carrier	OK
PCIe routing supports both on-module DX-M1 and external M.2 (or accepts that external M.2 is disabled when DX-M1 active)	OK
Thermal: copper pour or heatsink contact over the DX-M1 region of the SoM	OK
Correct firmware per SKU + target core (e1m-v2m10x-a55 Yocto MACHINE for DX-M1 access)	OK

Table 4 V2N-M1 carrier-board design checklist

11 Ordering Information

E1M-X V2N-M1 modules are ordered based on:

- Memory tier (4 GB / 8 GB LPDDR4X; 4 GB / 16 GB eMMC)
- Assembly options (lead finish, ball material)

Refer to the **E1M-X V2N-M1 Datasheet** (DS-V2N-M1-001) §15 for the complete ordering matrix and MPN decoder.

12 Notices

- Specifications subject to change without notice.
- Some features may be preliminary at this revision.
- Always verify against the latest **E1M-X V2N-M1 Datasheet** (DS-V2N-M1-001).
- This guide complements but does not replace the Renesas RZ/V2N PCB design guidelines or the DeepX DX-M1 hardware integration manual.

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