ALP LAB

E1M-X Development Board

User Guide

Document Number: UG-E1M-X-001 **Revision:** 0.1 **Date:** May 2026 **Status:** Draft

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Release History

Revision	Changes	Date
0.1	Initial draft. Structural mirror of UG-E1M-001 with V2N / V2N-M1 specifics; TBD callouts for carrier-board details pending authoritative HW writeup.	May 2026

Table 1 Release History

1 Purpose and Scope

This document is the schematic-level user guide for the **E1M-X Evaluation Kit** (45 × 65 mm carrier), targeting the **E1M-X V2N** and **E1M-X V2N-M1** SoM families based on the Renesas RZ/V2N vision-AI MPU (with the V2N-M1 family adding an on-module DeepX DX-M1 25-TOPS AI accelerator).

It complements:

- The **E1M-X V2N Datasheet** (DS-V2N-001) and **E1M-X V2N-M1 Datasheet** (DS-V2N-M1-001) — the canonical pin and electrical reference.
- The **E1M-X V2N HW Design Guide** (HG-V2N-001) and **E1M-X V2N-M1 HW Design Guide** (HG-V2N-M1-001) — carrier-board design rules.
- The **E1M EVK User Guide** (UG-E1M-001) — the smaller 35 × 35 mm sibling kit, structurally mirrored here.
- The **E1M Specification** (E1M-STD-1.0) — the open standard the form factor and pinout conform to.

This guide answers “where does each signal go on the E1M-X EVK carrier?” — it is not a tutorial; for that, see the **E1M-X EVK Getting Started Guide** (QS-E1M-X-EVK-001).

2 Safety, Handling, and ESD

- **ESD-sensitive**. Handle on a grounded mat with a wrist strap.
- **Hot-plug not supported** for the M.2 slots, USB host port, or display / camera FFCs.
- **No customer-rework** of the SoM is permitted; rework voids warranty.
- **Max ambient operating temperature**: +85 °C (S-grade SoM). Free-air convection is sufficient for hello-world workloads; full DRP-AI + DX-M1 + dual-Ethernet pushes the SoM towards its thermal limit and a heatsink is recommended.

> **Warning:** The on-module DeepX DX-M1 (V2N-M1 variants only) dissipates significant heat at full load. Plan for active cooling or a copper-pour heatsink contact when running sustained inference.

3 Functional Overview

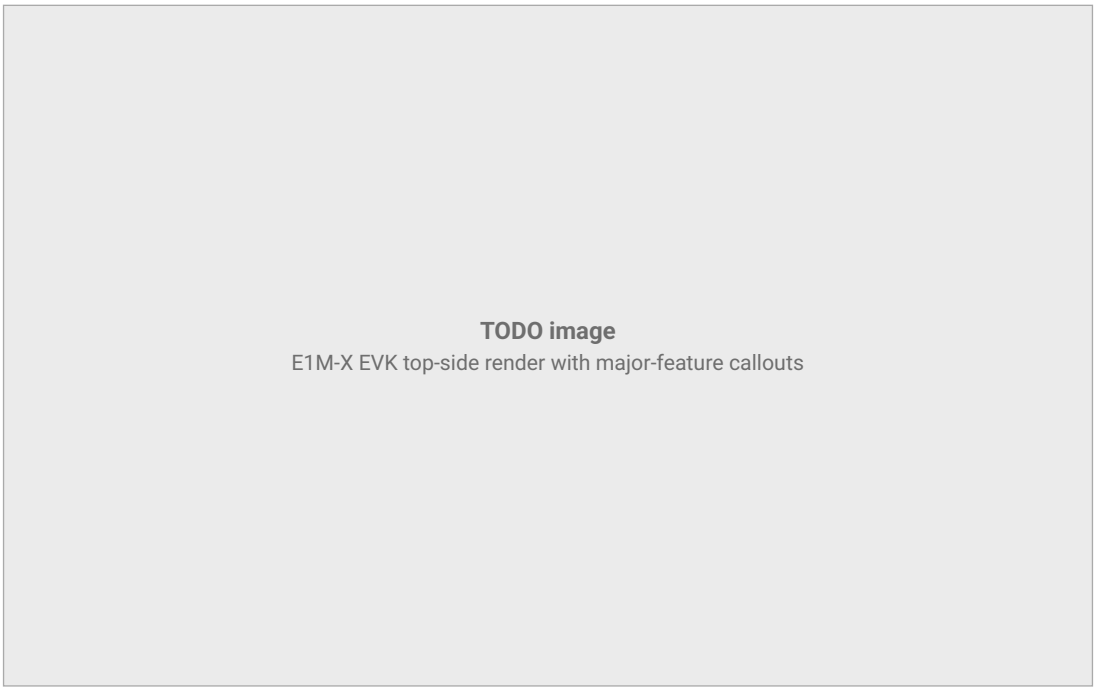

Figure 1 E1M-X EVK top-side render with major-feature callouts

The E1M-X EVK exposes every interface defined in the E1M-X form factor that the V2N family routes. Section §4 onward covers each block in detail.

Block	Description
Power	12 V barrel-jack + USB-PD on three USB-C ports. On-board protected 5 V rail to the SoM's `VDD_5V_IN` pads. INA236 current monitors per major rail for runtime power profiling.
Boot / Reset / Debug	4-position DIP switch for RZ/V2N `BOOT0`–`BOOT3` straps; `PORn` + `MODULE_EN` push-buttons; 10-pin Cortex SWD/JTAG header; on-board FTDI dual-channel USB-UART bridge.
USB	3 × USB-C (PWR / USB3 / CONSOLE), 1 × USB-A host port, ID-pin mux.
Ethernet	2 × RJ45 with integrated magnetics, routed to both on-module Realtek RTL8211FDI PHYs.
Storage	microSD socket on the SoM's SDIO interface; M.2 Key M (2280) for NVMe SSDs.
Display	2 × MIPI-DSI 40-pin FFC connectors (one per DSI lane set), optional MIPI-DSI → HDMI bridge.
Camera	2 × MIPI-CSI connectors (RPi-compatible pinout on `CSI0`).
CAN-bus	2 × screw-terminal connectors with 120 Ω termination jumpers (post-PHY, bus-level).
Audio	PDM microphone array, I^2S codec interface, amplified speaker output.
Expansion	mikroBUS click-board socket; M.2 Key E for Wi-Fi / cellular / co-processor cards.
Sensors	On-board temperature, light, IMU, and pressure sensors on the EVK's `alp_i2c0` bus.
Current monitoring	Per-rail INA236 monitors expose live current/voltage telemetry over the SDK's `alp_ina236` driver.

Table 2 Major functional blocks on the E1M-X EVK

4 Power System

4.1 Power Inputs

4.1.1 Barrel Jack (primary)

12 V DC, centre-positive, 5 A maximum. This is the recommended supply for the E1M-X EVK because the V2N family's peak power (full DRP-AI + dual-Ethernet + M.2 SSD + display + camera) exceeds the USB-PD ceiling on most hosts.

4.1.2 USB-C Inputs

Three USB-C ports accept USB-PD up to 100 W (5 A / 20 V class):

- **USB-C 0 (`PWR`)** — primary power-input port; also acts as the SoM's USB 3.2 Gen 2 device port.
- **USB-C 1 (`USB3`)** – second USB 3.x port (host or device per ID-pin), can also source power.
- **USB-C 2 (`CONSOLE / DEBUG`)** — console + FTDI bridge, can also source power.

> **Warning:** Do not supply power on more than one source simultaneously if one of them is below 5 V. Reverse current through a depleted source can damage the upstream supply.

4.2 Main 5 V Generation and Protection

A wide-input buck converter (TBD MPN) generates the protected 5 V rail to the SoM from any of the three power sources. Protection elements:

- ORing eFuse selects between barrel jack and USB-PD inputs.
- TVS diode array clamps surges on `VDD_5V_IN`.
- Inrush limiter softens turn-on so the SoM's PMIC sees a clean ramp.

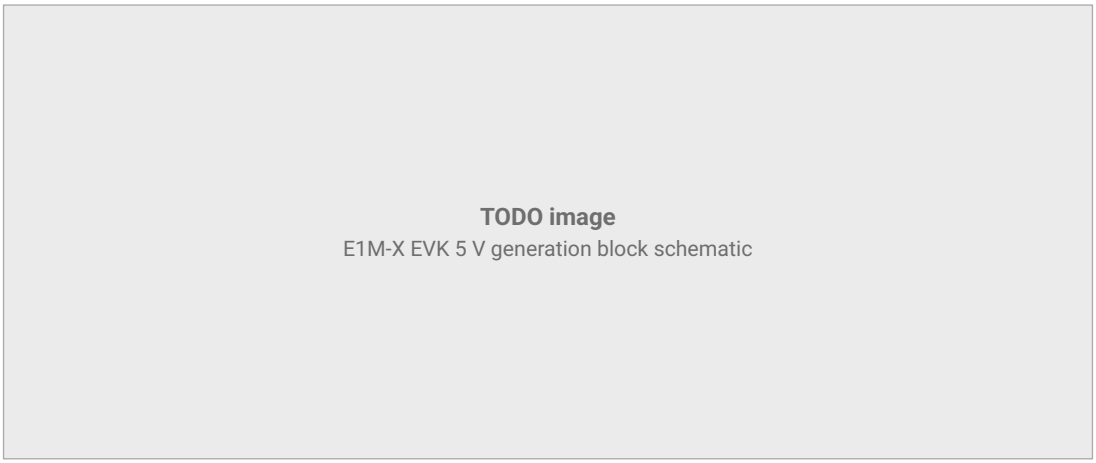

Figure 2 E1M-X EVK 5 V generation block schematic

4.3 Secondary Rails

The on-module Renesas DA9292 PMIC and ACT8760 PMIC generate every silicon-internal rail (LPDDR4X DRAM, RZ/V2N core, IO 1V8, etc.). The carrier supplies **only** the 5 V input.

Two output rails are sourced **from** the SoM to the carrier board:

- `VIO_OUT` (1V8) drives the I/O-reference rails of every level-shifter on the carrier (USB-C CC, I/O-expander logic, etc.).
- `SD_VDD_OUT` (1V8 / 3V3 selectable) supplies the microSD socket; the SoM auto-switches it for high-speed vs default-speed cards.

> **Warning:** `VIO_OUT` and `SD_VDD_OUT` are outputs from the module, not power inputs. Do not source them externally.

4.4 SuperCap Rail

The optional super-capacitor on +S_CAP provides hold-up for the RTC and DX-M1 model-context retention through a brief carrier-board brown-out. TBD — the V2N reference firmware does not yet exercise this path; see **bring-up-v2n.md** in the SDK.

5 Boot, Reset, and Debug

5.1 Debug Connectors

- **Cortex 10-pin SWD/JTAG header** (1.27 mm pitch) for external SEGGER J-Link or any CMSIS-DAP probe. Connects directly to the SoM's `JTAG_*` pads at 1V8 logic levels.
- **FTDI dual-channel USB-UART bridge** on USB-C 2:
  - Channel A: RZ/V2N SCIF console at 115 200 8N1 (default).
  - Channel B: GD32 supervisor-MCU debug UART; reserved for SDK developers.

5.2 Reset

The `PORn` push-button drives the SoM's `PORn` pad low through a 10 kΩ pull-up to 1V8.

- Press momentarily to issue a power-on reset to the entire SoM (RZ/V2N + GD32 + DX-M1).
- Held > TBD ms during boot it asserts `BOOT3` low (CM33 boot) regardless of DIP-switch position — useful for recovering a SoM stuck in a CA55 brick.

5.3 Boot Mode Selection

The 4-position DIP switch selects the RZ/V2N boot source. The mapping mirrors **DS-V2N-001 §4.1**:

BOOT1	BOOT0	Mode	Device	CA55 boot	CM33 boot
0	0	Mode 0	eSD (3.3 V execution)	Supported	Not supported
0	1	Mode 1	eMMC (1.8 V I/O) *(factory default)*	Supported	Not supported
1	0	Mode 2	QSPI NOR (1.8 V I/O)	Supported	Supported
1	1	Mode 3	SCIF download (USB)	Supported	Supported

Table 3 Boot DIP-switch mapping

BOOT2 is hard-strapped to 1 on the carrier. BOOT3 is exposed on the DIP and selects the boot CPU (high = CA55, low = CM33).

5.4 Module Enable / Standby

- `MODULE_EN` push-button + pull-up to 5 V; press momentarily to disable the module. Release to re-enable.
- `MODULE_STBY` test-point only (no front-panel button); accessible for low-power experiments. The reference firmware does not yet wire it; see **bring-up-v2n.md**.

5.5 Antenna

`ANT_2.4GHz`, `ANT_5GHz`, `ANT_6GHz` are routed from the SoM to a 3-position SMA / U.FL connector on the carrier edge. The reference EVK populates U.FL by default; SMA is an alternate fit. 50 Ω controlled-impedance trace.

6 USB Subsystem

6.1 USB-C Ports

The three USB-C ports map to the V2N's USB controllers:

Port	Silkscreen	SoC controller	Notes
USB-C 0	`PWR`	`USB0` (USB 3.2 Gen 2)	Primary power input; also acts as USB 3.x device. CC pins drive PD negotiation.
USB-C 1	`USB3`	`USB0` (alternate)	Lane-muxed onto the same `USB0_30_*` differential pairs; only one of `USB-C #0` and `USB-C #1` is active at a time, selected by the `USB0_30_ID` pin.
USB-C 2	`CONSOLE / DEBUG`	(FTDI bridge only)	Not an SoC USB port; routes the FTDI USB-UART bridge plus a third USB-PD input.

Table 4 USB-C ports on the E1M-X EVK

> **Note:** The V2N family has **one** USB 3.x controller (`USB0`). The two USB-C ports labelled `PWR` and `USB3` time-share that controller through the `PI3WVR648` lane mux. Software selects the active port via the `USB_MUX_SEL` I/O-expander bit; see **bring-up-v2n.md** in the SDK.

6.2 USB-A Host Port

A single USB-A 2.0 host port is routed from the SoM's `USB2_*` differential pair through a TVS array. Host or Function role is selected by tying `USB2_20_ID` low (Host) or leaving it NC (Function).

6.3 Data Mux and Host ID

The `PI3WVR648` high-bandwidth lane mux switches the `USB0_30_*` differential pair between the two USB-C ports. The `USB0_30_ID` pin acts as the role selector for the active port.

7 Ethernet

Two RJ45 jacks with integrated magnetics connect to the SoM's two on-module Realtek RTL8211FDI PHYs (mandatory on-module per **E1M Spec** §6.5). The PHYs sit on the SoM; the carrier provides **only** the magnetics and the connector.

Jack	SoM port	Notes
ETH0	ETH0_DA*–ETH0_DD*	Primary 1 GbE. LEDs driven by ETH0_LED0/1.
ETH1	ETH1_DA*–ETH1_DD*	Secondary 1 GbE. LEDs driven by ETH1_LED0/1.

Table 5 Ethernet jacks on the E1M-X EVK

Both ports support IEEE 1588 PTP (the V2N's MAC supports it; PHY pin-strap is set to enable PTP on power-up). Cable specifications: Cat-5e or better, 100 m max.

8 CAN Bus

8.1 Transceiver

Both CAN0 and CAN1 exit the SoM at the **bus level** (CANxH, CANxL) — the CAN-FD transceivers (TI TCAN1044AVDRBRQ1) are on-module per **E1M Spec** §6.5. The carrier provides only termination and the connector.

8.2 Headers and Jumpers

- Screw-terminal connectors on the front edge of the carrier (CANH / CANL / GND).
- 120 Ω termination resistors switchable via jumper headers (one per CAN port).
- TVS ESD-protection diodes on each bus.

Figure 3 E1M-X EVK CAN-bus connector + termination jumper layout

9 microSD and SDIO Muxing

9.1 microSD Socket

A standard push-push microSD socket on the SoM's SDIO interface (SD_CLK, SD_CMD, SD_D0–SD_D3, SD_DET, SD_RST). SD-card power comes from the SoM's SD_VDD_OUT rail (auto-switching 1V8 / 3V3).

The card-detect line (SD_DET) is open-drain; the socket includes the standard mechanical detect contact.

9.2 SDIO Multiplexing

Unlike the smaller E1M EVK, the E1M-X EVK does **not** multiplex SDIO to an alternate target — the V2N family's SDIO controller drives the microSD socket exclusively. The M.2 Key M slot uses PCIe, not SDIO.

10 Display (MIPI DSI)

The V2N family routes **two** 4-lane MIPI DSI interfaces (`DSI0`, `DSI1`). The E1M-X EVK exposes both to dedicated 40-pin FFC connectors, with an optional MIPI-DSI → HDMI bridge (ITE `IT6162`, populated by default on `DSI0`).

Output	DSI port	Notes
HDMI Type-A	`DSI0` via IT6162	Up to 1920 × 1200 @ 60 fps RGB888. EDID read over the IT6162's I^2C secondary.
DSI0 FFC (40-pin)	`DSI0` direct	Bypasses the IT6162; populate either-or via a 0 Ω series jumper.
DSI1 FFC (40-pin)	`DSI1` direct	Independent of the IT6162.

Table 6 Display outputs on the E1M-X EVK

The on-module backlight driver is fed by `BL_LED_A`, `BL_LED_K`, and `BL_PWM` (see **DS-V2N-001 §7.7**). The backlight feedback resistor is sized per the requested LED current:

$$I_{\mathrm{LED}} = 95 \frac{\mathrm{mV}}{R_{\mathrm{FB}}}$$

11 Camera Interfaces

The V2N family routes **two** 4-lane MIPI CSI-2 interfaces (`CSI0`, `CSI1`).

11.1 RPi-Compatible CSI

`CSI0` is exposed on a 22-pin RPi-compatible FFC connector. Compatible with Raspberry Pi V2 / HQ cameras and most third-party RPi-pinout modules. The on-module Mali-C55 ISP processes this stream.

11.2 Second MIPI CSI

`CSI1` is exposed on a standard MIPI CSI 30-pin B2B (or FFC, alternate fit) connector with the on-module `+V_CAM1` LDO providing camera-side power.

11.3 Camera Switching, Rails, and Level Shifting

Per-camera LDOs (`+V_CAM0`–`+V_CAM3`) are on the SoM. The feedback divider for each rail is placed on the **carrier** near the `CAM_VFBx` pin:

$$V_{\mathrm{CAM}} = 0.6\ \mathrm{V} \times \left(1 + \frac{R_1}{R_2}\right)$$

EMI and ESD protection on the MIPI CSI lanes is on-module; no external protection is required.

12 PCIe and M.2 Expansion

The V2N family has a single PCIe Gen3 × 2 controller (`PCIE0_*`). On V2N-M1 modules, this controller is permanently routed to the on-module DeepX DX-M1, **and** multiplexed out to the carrier on the same pads; software flips the mux at runtime (see **HG-V2N-M1-001 §6.7**).

12.1 M.2 Key M

A 2280 M.2 Key M slot accepts NVMe SSDs up to PCIe Gen3 × 2 (≈1.6 GB/s sustained). Active only when:

- On a V2N module: always (no mux).
- On a V2N-M1 module: when the PCIe mux is pointed at the carrier (M.2). When the mux points at the on-module DX-M1, this slot is inactive.

The slot is powered from the carrier's protected 3.3 V rail; the SSD-PWREN signal is gated by the SoM via the I/O expander.

12.2 M.2 Key E

A 2230 M.2 Key E slot accepts Wi-Fi / cellular / co-processor cards on a 1-lane PCIe Gen3 link. This shares PCIe lanes with the M.2 Key M slot via the PI3WVR648 lane mux; only one slot is active at a time.

12.3 PCIe Reference Clock and Switching

PCIe reference clock is generated on-module by the RZ/V2N; the carrier does not need to add a clock source. The PCIE0_CLK_N/P pair is routed differentially from the SoM to the lane mux, then to either M.2 slot.

12.4 PCIe I/O Expander

A Texas Instruments TCA9554 8-bit I/O expander on alp_i2c0 controls:

- M.2 Key M power gate (SSD_PWREN).
- M.2 Key E power gate (WIFI_PWREN).
- PCIe lane-mux select (PCIE_MUX_SEL).
- USB lane-mux select (USB_MUX_SEL).
- DX-M1 PCIe routing (V2N-M1 only; see **HG-V2N-M1-001 §6.7**).

The SDK driver is <alp/chips/tca9554.h>.

13 Audio

13.1 PDM Microphones

The V2N family routes 2 × PDM clock/data pairs (PDM_C0/D0, PDM_C1/D1), each supporting two microphones (stereo per PDM port). The carrier populates a 4-microphone array along the front edge for beamforming experiments.

13.2 Amplifiers and Speaker Outputs

A TI TAS5825M class-D amplifier (TBD) drives a 4 Ω speaker output via a 3.5 mm jack. Configured over alp_i2c0.

13.3 I²S Routing

Both I2S0 and I2S1 are routed to the amplifier and to a 3.5 mm headphone jack via a TBD codec (alternate fit; populate per BOM revision).

14 Sensors and I/O Expansion

14.1 Sensor Devices

The E1M-X EVK populates the same sensor lineup as the E1M EVK:

Sensor	Function	Bus / address	Driver
Bosch BME688	Temperature, humidity, pressure, gas	`alp_i2c0` @ `0x76`	`<alp/chips/bme688.h>`
ams AS7341	10-channel spectral / colour sensor	`alp_i2c0` @ `0x39`	`<alp/chips/as7341.h>`
TDK ICM-42688-P	6-axis IMU (gyro + accel)	`alp_i2c0` @ `0x68`	`<alp/chips/icm42688p.h>`
TI TMP117	High-accuracy temperature sensor	`alp_i2c0` @ `0x48`	`<alp/chips/tmp117.h>`

Table 7 On-board sensors on the E1M-X EVK

14.2 I²C Bus and Pullups

`alp_i2c0` is the EVK's primary sensor bus, routed from the SoM's `I2C0` pads. Pull-ups: 4.7 kΩ to `VIO_OUT` (1V8).

A secondary I²C bus (`alp_i2c1`) exits the SoM on `I2C1` pads and is exposed on the mikroBUS socket only.

14.3 I/O Expander

A second TCA9554 I/O expander on `alp_i2c0` @ `0x21` handles user-LED multiplexing, sensor-power gating, and the boot-LED indicators.

15 Current Measurement (Power Profiling)

The E1M-X EVK carries TI INA236 current monitors on every major rail:

- `VDD_5V_IN` (carrier-side, measures power into the SoM)
- `VIO_OUT` (1V8 to carrier-side level shifters)
- `SD_VDD_OUT` (microSD)
- `+V_CAM0`…`+V_CAM3` (4 × camera LDOs)
- Per-M.2-slot rails

All INA236 instances share `alp_i2c0` at addresses TBD. The SDK driver is `<alp/chips/ina236.h>`; an example script under `examples/iot-fleet-ota/` aggregates rail telemetry over MQTT.

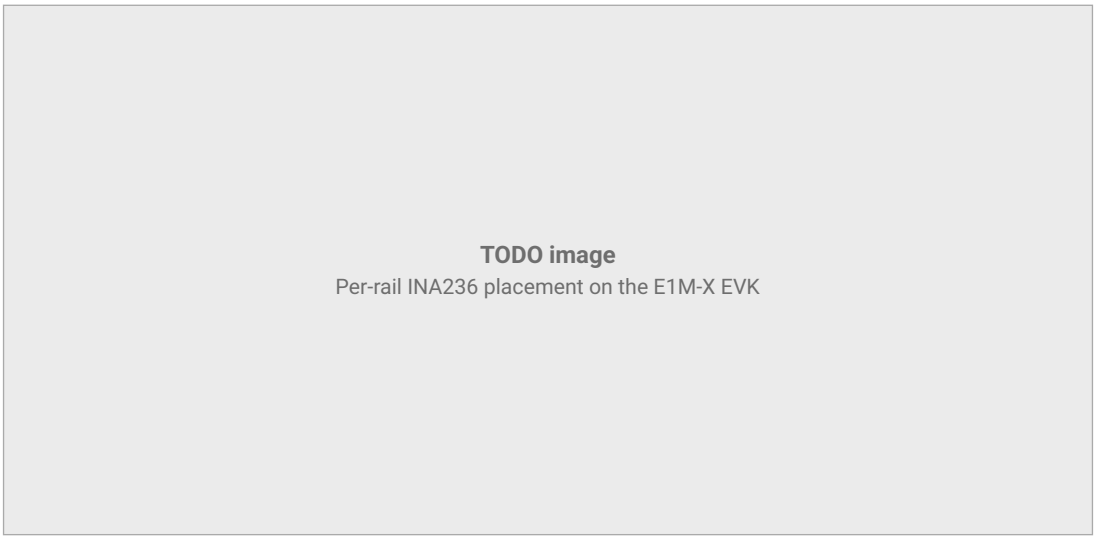

Figure 4 Per-rail INA236 placement on the E1M-X EVK

16 User Interface

The user-interface block on the front edge of the carrier carries:

- 3 × user LEDs (USR0, USR1, USR2), driven by GPIOs through the secondary I/O expander.
- 1 × user push-button (USR_BTN), connected to a SoM GPIO with internal pull-up.
- 4-position boot DIP switch (covers BOOT0, BOOT1, BOOT3; BOOT2 is hard-strapped on the carrier).
- 2 × reset push-buttons (PORn, MODULE_EN).
- 4 × status LEDs:
  - PWR (green) — 5 V rail valid.
  - IO_EN (green) — SoM IO_EN asserted (boot ROM running).
  - M1_RDY (V2N-M1 only, blue) — DeepX DX-M1 PCIe link up.
  - BL_PWM (white) — backlight driver active.

17 Expansion

17.1 mikroBUS

A single mikroBUS click-board socket exposes:

- SPI: SPI2_CS0, SPI2_SCLK, SPI2_MOSI, SPI2_MISO (V2N's third SPI controller, dedicated to expansion).
- I^{2}C: alp_i2c1 (I2C1_SCL, I2C1_SDA).
- UART: UART1_RX, UART1_TX.
- 1 × INT, 1 × RST, 1 × CS, 1 × PWM, 1 × ADC (routed via the on-module ADC mux).
- 3V3 and 5V power.

Compatible with the full Mikroe click-board catalogue.

> **Note:** The E1M-X EVK **does not** carry the Arduino UNO R3 header that the smaller E1M EVK exposes. If Arduino-shield compatibility is required for prototyping, use the E1M EVK or build a custom carrier.

17.2 M.2 Key E (secondary)

See the **M.2 Key E** subsection under **PCIe and M.2 Expansion** above.

18 Recommended Bring-Up Checklist

1. Verify the boot DIP switch matches the SoM SKU's intended boot mode (eMMC for factory image; SCIF for re-flash). See **Table 4**.
2. Connect the console USB-C cable to your host; confirm two FTDI virtual serial ports enumerate.
3. Apply 12 V via the barrel jack (preferred) or USB-PD on PWR.
4. Confirm PWR and IO_EN LEDs come on within 100 ms.
5. Open the console at 115 200 8N1 (Channel A) and watch for the SoM boot banner.
6. For V2N-M1: after first Linux boot, verify the DX-M1 enumerates with `lspci` (expected vendor:device `1c3c:0001`).

19 Known Design Notes

- The PCIe lane mux (PI3WVR648) adds ≈ TBD ps of insertion delay per lane; carriers cloning this design should add equivalent length-tuning if they don't use the mux.
- The IT6162 MIPI-DSI ⟶ HDMI bridge requires an EDID read over its I^{2}C secondary before issuing the first frame; the SDK driver handles this automatically.
- The boot DIP switch is sampled at PORn rising edge; changing it during runtime has no effect until the next reset.
- MODULE_STBY is wired but not yet exercised by the reference firmware. Low-power experiments using this signal require manual configuration of the GD32 supervisor.

Note: Sections marked **TBD** will be filled in as the EVK schematic Rev. 1.0 is finalised. Issue tracker for this guide: see github.com/alplabai/alp-product-docs/issues tagged `e1m-x-evk-user-guide`.