



E1M-X V2N HW Design Guide

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Table of Contents

Release History	2	7.3 MIPI CSI-2 Cameras	8
1 Introduction	3	7.4 MIPI DSI Displays	8
1.1 Purpose of This Document	3	7.5 CAN-Bus	9
1.2 Product Overview	3	7.6 PCIe	9
2 Supported SoC Variants	4	7.7 USB	9
3 Mechanical Information	4	7.8 Digital Communication	10
3.1 Dimensions	4	7.9 Audio and Sensor Interfaces	10
3.2 Handling and Assembly	4	7.10 Analog Interfaces	10
4 Power Architecture	4	7.11 PWM and Encoder Interfaces	10
4.1 Power Input	4	8 Software Support	10
4.2 Power Design Guidelines	4	8.1 Alp SDK™	10
4.3 Carrier-Board 5 V Generation	5	8.2 AI Acceleration	10
5 Memory and Boot Architecture	5	9 Bring-Up Checklist	11
5.1 Internal Memory (SoC-Dependent)	5	9.1 Pre-Power Checks	11
5.2 On-Module Memory	5	9.2 First Power-On	11
5.3 Boot	6	9.3 Basic Validation	11
6 Carrier-Board Reference Block Diagram	6	9.4 Common Issues	11
6.1 System-Level Overview	6	10 Design Checklist (Summary)	11
6.2 Design Philosophy	7	11 Ordering Information	12
7 Interfaces Overview	7	12 Notices	12
7.1 Ethernet Interfaces	7		
7.2 Wi-Fi and BLE	7		

List of Figures

Figure 1 E1M-X V2N Block Diagram	3	Figure 6 V2N RF antenna routing reference	8
Figure 2 5 V buck-converter reference circuit	5	Figure 7 MIPI CSI-2 routing example	8
Figure 3 eFuse / power-OR reference circuit	5	Figure 8 MIPI DSI routing example with backlight driver	9
Figure 4 Carrier-board reference block diagram for V2N	6	Figure 9 CAN-BUS reference termination and connector	9
Figure 5 V2N Ethernet PHY-to-magnetics reference connection	7		

List of Tables

Table 1 Release History	2	Table 3 V2N carrier-board design checklist	11
Table 2 V2N-family SKUs	4		

Release History

Revision	Changes	Date
0.1	Initial draft.	May 2026
0.2	Interface ESD/EMI protection moved to the carrier board (Ethernet, MIPI CSI, MIPI DSI); on-module protection retained only on the SD-card interface.	June 2026

Table 1 Release History

1 Introduction

1.1 Purpose of This Document

This guide provides practical guidance for developers and system integrators using the **E1M-X V2N System-on-Module (SoM)**.

It covers:

- Hardware integration and carrier-board design
- Power architecture and system bring-up
- Interface usage and pin functional intent
- Common pitfalls during first implementation

This guide complements:

- The **E1M-X V2N Datasheet** (DS-V2N-001)
- The **Renesas RZ/V2N** hardware reference manual and PCB design guidelines
- The **E1M Specification** (E1M-STD-1.0) for form-factor and pinout requirements
- The **Alp SDK™** documentation

1.2 Product Overview

The **E1M-X V2N** is a compact **45 × 65 mm Edge-AI System-on-Module** based on the **Renesas RZ/V2N** vision-AI MPU. It targets industrial vision, robotics, automotive driver-monitoring, and high-throughput AI inference applications.

The module follows the **E1M-X™ open-standard pin layout**, enabling drop-in compatibility with other E1M-X-conformant SoMs without redesigning the carrier board.

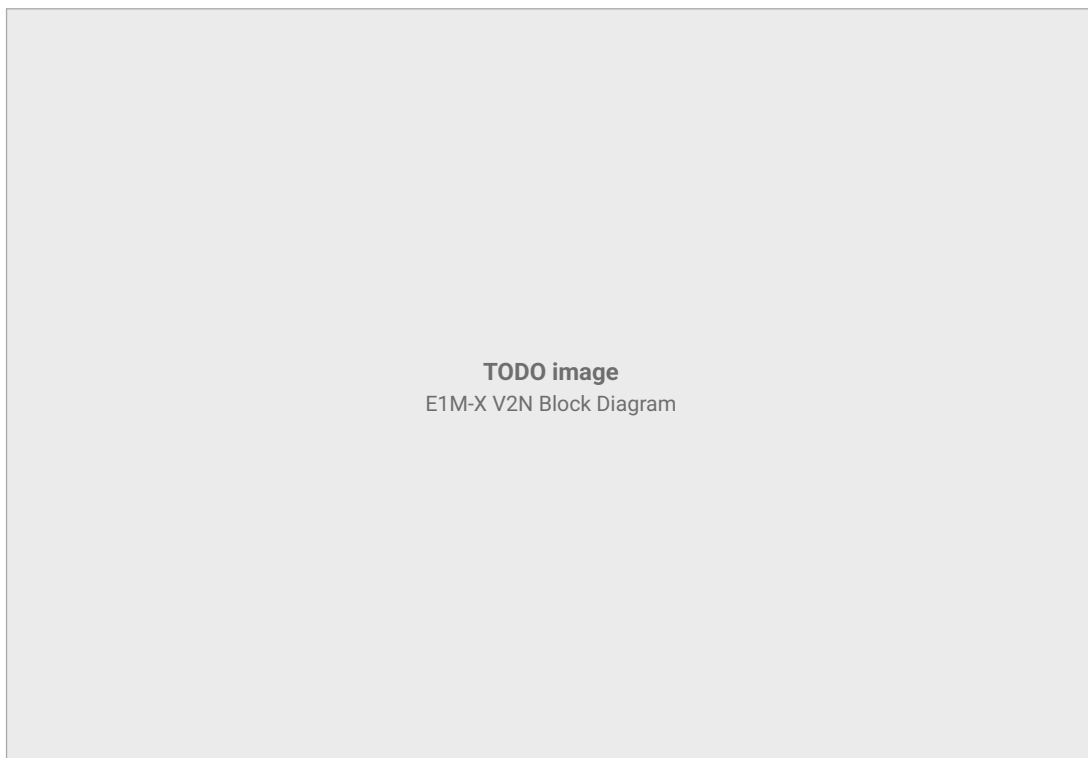


Figure 1 E1M-X V2N Block Diagram

Key characteristics:

- Unified E1M-X pinout, hardware-compatible with future RZ/V2N successors
- Quad Cortex-A55 @ 1.8 GHz + Cortex-M33 @ 200 MHz application + real-time cluster
- DRP-AI3 AI accelerator (4 TOPS)
- Arm Mali-C55 ISP + Mali-G31 GPU
- On-module 1 Gbit Ethernet PHYs (× 2), Wi-Fi 6 + BLE 5.4 combo, CAN-FD transceivers (× 2)

- On-module power management (Renesas DA9292 PMIC) plus GD32 supervisor MCU
- Single external **5 V supply**
- Long-term lifecycle orientation

2 Supported SoC Variants

SKU	Renesas Part	LPDDR4X	eMMC
E1M-V2N101	R9A09G056N44GBG#AC0	32 Gbit	eMMC 5.1, 32 Gbit
E1M-V2N102	R9A09G056N44GBG#AC0	64 Gbit	eMMC 5.1, 128 Gbit

Table 2 V2N-family SKUs

Both SKUs share identical pinouts and silicon outside of the memory tier; carrier boards designed against one SKU work unmodified with the other.

3 Mechanical Information

3.1 Dimensions

- **Size:** 45 × 65 mm
- **Form factor:** Connectorless, solder-down LGA SoM
- **Height profile:** Standard-height class per **E1M Spec** §5.2.1

For the full mechanical drawing including land pattern and keep-out zones, see the **E1M-X V2N Datasheet** (DS-V2N-001) §13.

3.2 Handling and Assembly

- ESD-sensitive device. Use grounded handling equipment.
- Avoid mechanical stress after soldering.
- Follow IPC J-STD-020 reflow profile (see DS-V2N-001 §11.2).
- Maintain PCB flatness per Renesas DA9292 PMIC requirements; warpage > TBD μm may compromise BGA solder joints under the SoC.

4 Power Architecture

4.1 Power Input

- **Input voltage:** 5 V DC, single rail on VDD_5V_IN
- All regulators, the PMIC, and sequencing are on-module
- No additional power rails must be supplied by the carrier

Warning: Do **not** attempt to power individual rails (VIO_OUT, SD_VDD_OUT, etc.) externally. These pads are **outputs** from the module; sourcing them externally will fight the on-module regulator and may damage the PMIC.

4.2 Power Design Guidelines

- Place bulk capacitance ($\geq 10 \mu\text{F}$) near the 5 V input
- Use a solid ground plane covering the entire SoM footprint
- Keep high-current paths (Ethernet PHY supplies, M.2 SSD slot supplies on the carrier) short and wide
- Do not power external loads from VIO_OUT unless validated; the rail is sized for level-shifters and small pull-ups only
- Nominal input voltage: 5.0 V; recommended tolerance: $\pm 5\%$

- Connect **every** GND pad on the SoM to a low-impedance plane (105 pads on E1M-X)
- No external sequencing required; the GD32 supervisor MCU handles the on-module rail order

4.3 Carrier-Board 5 V Generation

A buck converter is the recommended way to generate the 5 V rail from the carrier-board input voltage. Choose a converter rated for transients up to **5 A** to cover worst-case AI + dual-Ethernet + M.2 SSD activity simultaneously.

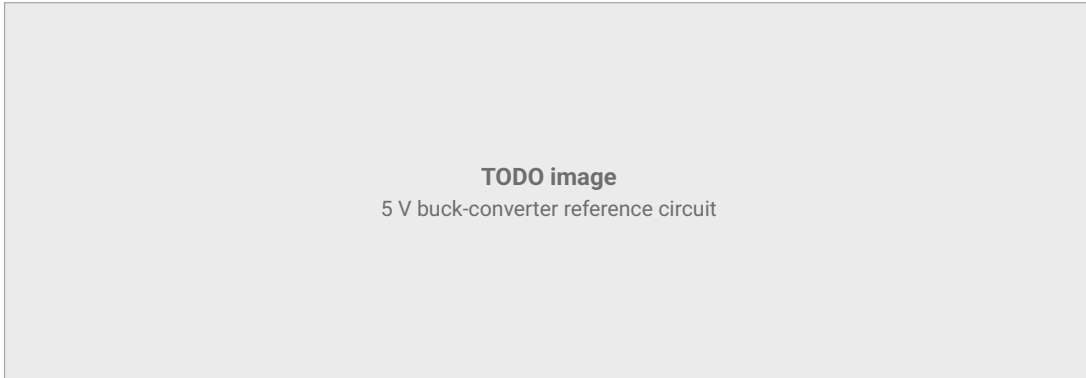


Figure 2 5 V buck-converter reference circuit

Power-OR'ing using diodes or eFuses is supported. When multiplexed (e.g. between barrel jack and USB-PD on a carrier), use a unidirectional eFuse to avoid back-feeding the inactive source.

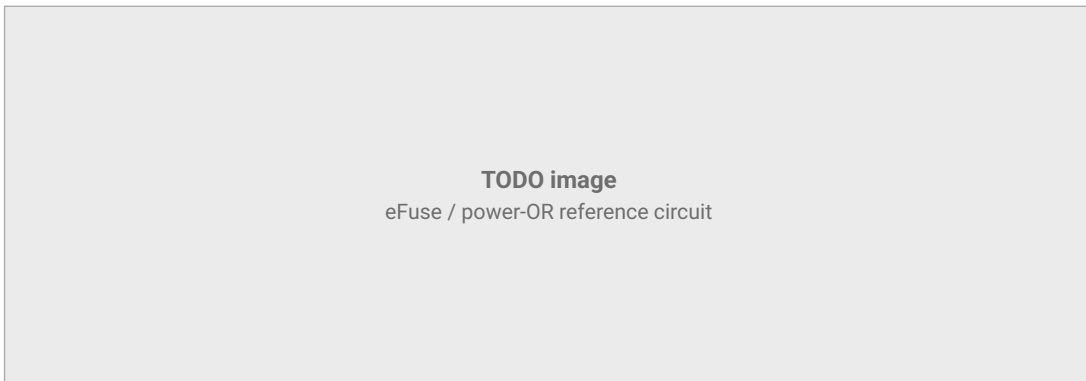


Figure 3 eFuse / power-OR reference circuit

5 Memory and Boot Architecture

5.1 Internal Memory (SoC-Dependent)

- **On-chip SRAM:** 1.5 MB (RZ/V2N)
- **LPDDR4X DRAM:** 32-bit, 3.2 GT/s, up to 8 GB (per SKU)

5.2 On-Module Memory

- **eMMC 5.1** up to 128 Gbit (per SKU)
- **SPI NOR flash:** 128 Mbit, boot-supported
- **I²C EEPROM:** optional, accessible via I2C0 for production-time configuration storage

Note: Contact Alp Lab for custom memory configurations (alternate eMMC sizes, NAND replacing NOR, expanded EEPROM).

5.3 Boot

The RZ/V2N samples four boot-strap pins at PORn release:

- B00T0, B00T1 select the boot device (eSD / eMMC / QSPI NOR / SCIF download).
- B00T2 is fixed at 1 on the V2N family.
- B00T3 selects the boot CPU (high = CA55, low = CM33).

See the **E1M-X V2N Datasheet** (DS-V2N-001) §4.1 for the full boot-mode truth table and DIP-switch interpretation on the reference EVK.

The carrier board **MUST** provide a way to drive B00T0 and B00T1. The simplest implementation is a 2-position DIP switch with 10 kΩ pull-downs on each line; the SoC pulls the line high when the switch is closed. Production carriers may hard-strap the pins to the desired boot mode.

Note: MODULE_EN is internally pulled up to 5 V; drive low to disable the module. Leave floating if not used. PORn is internally pulled up to 1.8 V; drive low for \geq TBD μ s to reset.

6 Carrier-Board Reference Block Diagram

The carrier board has been designed for the **E1M-X** open standard to support all E1M-X variants. The V2N family routes the following subset of the E1M-X pinout; carriers that target only V2N may leave the other pads unused.

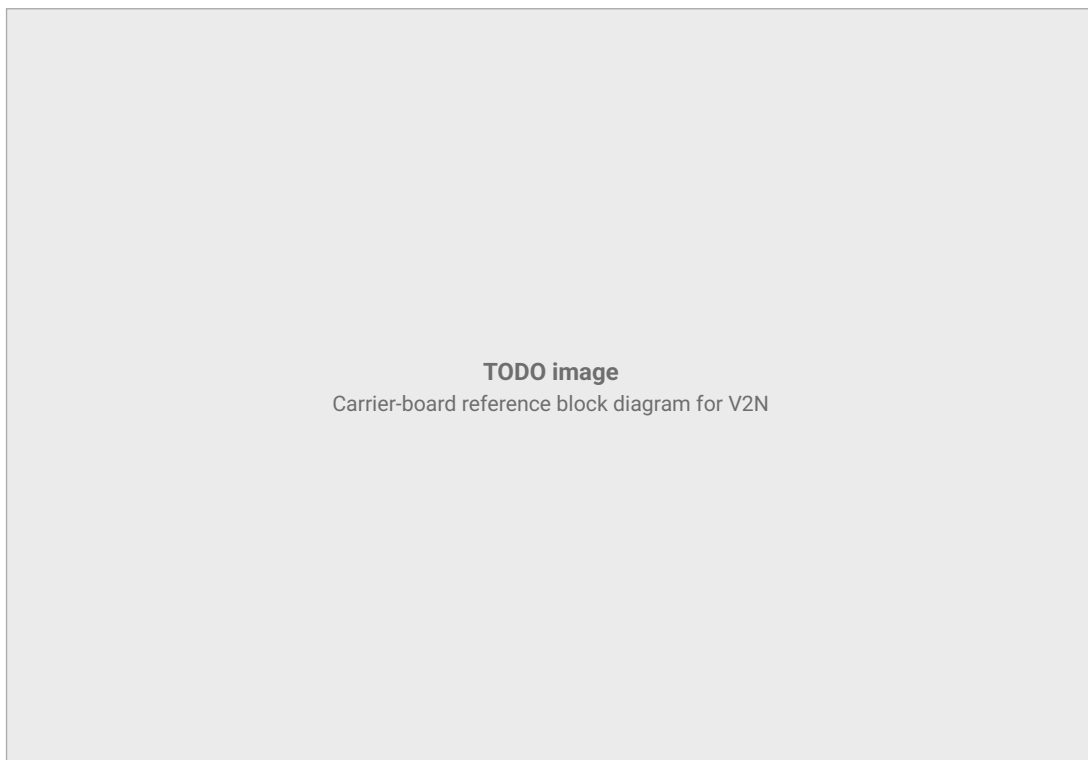


Figure 4 Carrier-board reference block diagram for V2N

6.1 System-Level Overview

The carrier board provides:

- 5 V power input and protection (barrel jack, USB-PD)
- External connectors and signal conditioning
- Magnetics + RJ45 for both Ethernet ports
- Termination + connectors for both CAN ports
- M.2 Key M / Key E slots for PCIe + Wi-Fi expansion
- Display + camera FFC connectors

- User-interface peripherals (LEDs, push-buttons, DIP switches)

All complex power, RF, EMI, and processing functions are integrated **into the E1M-X V2N module**.

6.2 Design Philosophy

- Keep the carrier board simple and application-specific.
- Avoid duplicating functionality already on-module (PMIC, Ethernet PHYs, Wi-Fi, CAN PHYs).
- Maintain reuse across V2N and V2N-M1 SoMs; both families share the same pinout subset.
- Minimise RF, power, and EMI risk on the carrier board.

7 Interfaces Overview

All interfaces are exposed through the standardised **E1M-X™ pinout**. The remainder of this section captures the carrier-board design rules per interface.

Note: See the **E1M-X V2N Datasheet** (DS-V2N-001) and the **E1M Specification** (E1M-STD-1.0) for the canonical pad-list and pin-function mapping.

7.1 Ethernet Interfaces

- 2 × 1 Gbit Ethernet via on-module PHYs (Realtek RTL8211FDI)
- External magnetics and RJ45 required on the carrier
- Auto-negotiation enabled by default
- EMI / ESD protection required on the carrier board

Route both Ethernet pairs as 100 Ω differential. Match the lengths within each pair to within ± 2 ps; match across the four pairs of one port to within TBD ps. The module does not integrate Ethernet ESD/EMI protection – add a low-capacitance ESD/TVS array (and common-mode choke as needed) on the MDI lines between the magnetics and each connector.

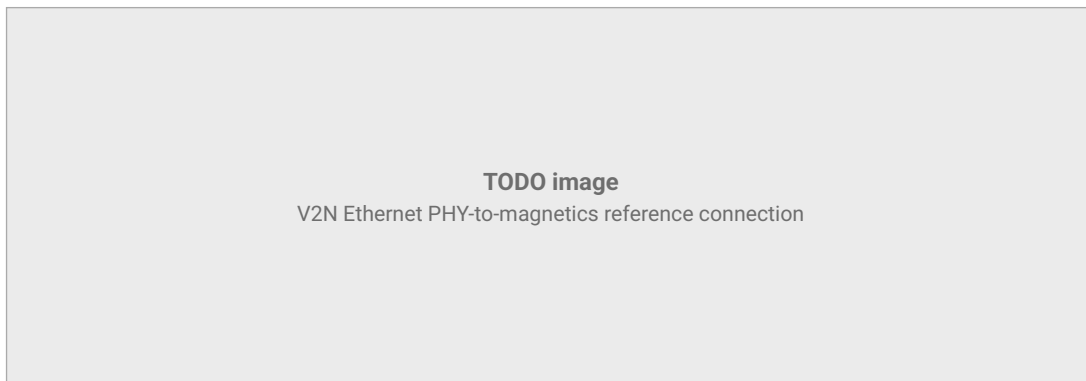


Figure 5 V2N Ethernet PHY-to-magnetics reference connection

Warning: Carrier-board designers **SHALL NOT** add an external Ethernet PHY between the SoM and the magnetics. The on-module PHYs are mandatory per **E1M Spec** §6.5; adding a second PHY breaks conformance and may damage the on-module driver.

7.2 Wi-Fi and BLE

- Wi-Fi 6 (2.4 / 5 / 6 GHz, 802.11 a/b/g/n/ac/ax) + BLE 5.4 via on-module Murata LBEE5HY2FY (Infineon CYW55513)
- Three antenna pads: ANT_2 . 4GHz, ANT_5GHz, ANT_6GHz
- 50 Ω impedance-controlled RF routing required on the carrier
- Keep digital noise away from RF paths; via stitching strongly recommended

Route each RF trace as 50 Ω controlled-impedance microstrip or coplanar waveguide. Maximum antenna gain to maintain regulatory compliance is TBD dBi per band.



Figure 6 V2N RF antenna routing reference

7.3 MIPI CSI-2 Cameras

- 2 × 4-lane MIPI CSI-2 interfaces (CSI0, CSI1)
- Up to 4K @ 30 fps per interface, 4 virtual channels
- Controlled-impedance differential routing required
- Minimise vias and stubs

Route each CSI lane as 100 Ω differential, ±10%. Match lengths within each pair and across the four lanes + clock of one camera. The module does not integrate CSI ESD/EMI protection – protect the lanes with a low-capacitance TVS array on the carrier board.



Figure 7 MIPI CSI-2 routing example

Per-camera LDOs (+V_CAM0...+V_CAM3) are available on-module. Place the divider feedback resistors close to the CAM_VFBx pins. The output voltage is set by:

$$V_{CAM} = 0.6 \text{ V} \times \left(1 + \frac{R_1}{R_2} \right)$$

7.4 MIPI DSI Displays

- 2 × 4-lane MIPI DSI interfaces (DSI0, DSI1)
- Up to 1920 × 1200 RGB888 @ 60 fps per interface
- DSI signals require EMI / ESD protection (low-capacitance TVS array) on the carrier board
- On-module backlight driver supports up to 10 LEDs in series or 2P6S

Route each DSI lane as 100 Ω differential, ±10%. The backlight feedback resistor for the on-module driver is computed as:

$$I_{LED} = 95 \frac{\text{mV}}{R_{FB}}$$



Figure 8 MIPI DSI routing example with backlight driver

7.5 CAN-Bus

- 2 × CAN-FD transceivers (TI TCAN1044AVDRBRQ1)
- Bus-level pads exposed to the carrier (CAN0H/L, CAN1H/L)
- The carrier **SHALL NOT** add an external transceiver

Add 120 Ω termination at each end of the bus and standard ESD / EMI protection at the connector.

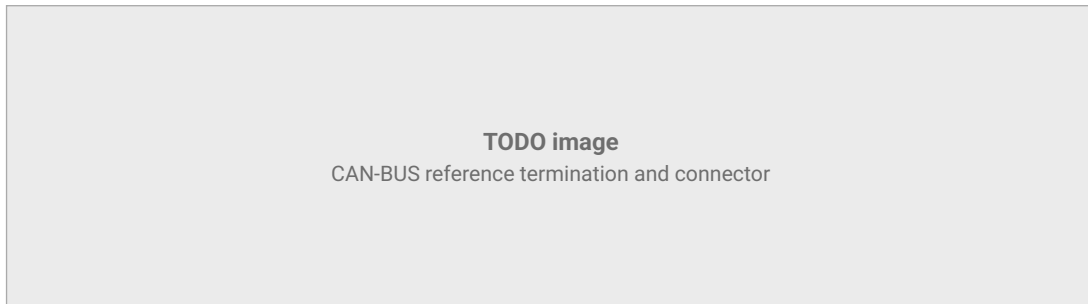


Figure 9 CAN-BUS reference termination and connector

Warning: The CAN-bus transceivers are **populated by default** on the V2N family. If isolation is required for the end application, the user must route the bus through an external isolated transceiver **after** the on-module transceiver, accepting the double-PHY topology.

7.6 PCIe

- PCIe Gen3, 2 lanes (PCIE0_*)
- Differential signalling, controlled-impedance routing required
- Carrier-board reference clock optional (on-module clock by default)

Route the four data pairs + clock as 85 Ω differential, matched ±2 ps within each pair. PCIe is single-instance on V2N; M.2 Key M and Key E on the reference carrier share this controller via a switch (see **E1M-X EVK User Guide** (UG-E1M-X-001) for the switching scheme).

Note: For the V2N-M1 family the PCIe controller is multiplexed with the on-module DeepX DX-M1. See **E1M-X V2N-M1 HW Design Guide** (HG-V2N-M1-001) §6.7 for the bring-up details.

7.7 USB

- 1 × USB 3.2 Gen 2 (USB0_30_*) – Host or Function
- 1 × USB 2.0 (USB2_*) – Host or Function via USB2_ID
- USB-C connector with CC pins (USB_CC1, USB_CC2)

Route the USB 3.2 differential pairs as 85 Ω the USB 2.0 pair as 90 Ω. Match lengths within each pair to within ±2 ps.

7.8 Digital Communication

- UART (× 2), SPI (× 3), I²C (× 4), I³C (× 1), I²S (× 2)
- Pin-mux configured in software via the Alp SDK™
- I²C / I³C **require** external pull-ups (TBD kΩ) on the carrier
- SPI chip-selects handled on the carrier

E1M-X uses a fixed pin-mux at the standard level. Use the relevant default function in your application; tertiary functions are silicon-specific and must be declared in the per-SoM manifest per **E1M Spec §8.4**.

7.9 Audio and Sensor Interfaces

- 2 × I²S, 2 × PDM (up to 4 digital microphones)
- Audio master clock available on AUDIO_CLK
- Keep audio clocks clean and isolated from switching power planes

7.10 Analog Interfaces

- 8 × ADC inputs via the secondary MCU (ANA_S0...ANA_S7)
- 2 × DAC outputs via the secondary MCU (DAC0, DAC1)
- All analog signals are 1V8-referenced
- Keep analog routing short and isolated from digital aggressors

7.11 PWM and Encoder Interfaces

- 8 × PWM outputs
- 4 × quadrature-encoder inputs
- Suitable for motor and control applications
- Software configuration via Alp SDK™

8 Software Support

8.1 Alp SDK™

- Open-source, CMSIS-compliant
- Unified HAL across all E1M-X variants (V2N, V2N-M1, future SKUs)
- Vendor-agnostic software architecture

The SDK exposes three board targets for V2N:

- `alp_e1m_v2n_m33_io` – on-module GD32 supervisor (216 MHz)
- `alp_e1m_v2n_m33_rt` – RZ/V2N internal Cortex-M33 (200 MHz)
- `alp_e1m_v2n_a55` – RZ/V2N quad Cortex-A55 (1.8 GHz, Zephyr SMP or Linux/Yocto)

8.2 AI Acceleration

- Renesas DRP-AI3, 4 TOPS dense, integrated in the RZ/V2N silicon
- Mali-C55 ISP for camera pre-processing
- Optimised for vision workloads (driver monitoring, object detection, classification)

For inference exceeding 4 TOPS, see the **E1M-X V2N-M1 HW Design Guide** (HG-V2N-M1-001) which adds the on-module DeepX DX-M1 25-TOPS accelerator.

9 Bring-Up Checklist

9.1 Pre-Power Checks

- Confirm the correct SoM variant (E1M-V2N101 vs E1M-V2N102).
- Verify orientation and solder joints (A1 corner against carrier fiducial).
- Ensure only 5 V is connected to VDD_5V_IN.
- Check ground continuity across all 105 GND pads.
- Confirm DIP-switch state for the intended boot mode.

9.2 First Power-On

- Apply 5 V.
- Monitor current consumption (expected idle: TBD mA).
- Check for abnormal heating on the SoM.
- Confirm PWR and IO_EN LEDs light within 100 ms.
- Open the console UART at 115 200 8N1 and watch for boot output.

9.3 Basic Validation

- UART boot / debug output on the SCIF console.
- Both Ethernet links coming up when cables are plugged in.
- GPIO or PWM toggle from a simple Zephyr build.
- Peripheral enumeration via the SDK (`west alp-list-peripherals`).

9.4 Common Issues

- Wrong DIP-switch position for the intended boot device (most common first-time failure).
- Missing Ethernet magnetics or RJ45 with wrong wiring.
- Wrong firmware image (built for the wrong core / wrong SKU).
- USB-C cable that doesn't support data lines (power-only cables are common).
- Insufficient supply current under PCIe SSD + AI load.

10 Design Checklist (Summary)

Item	Status
Single 5 V supply, ≥ 5 A rated	OK
Bulk + decoupling capacitance close to VDD_5V_IN	OK
Ethernet magnetics + RJ45 on both ports	OK
Controlled-impedance MIPI and PCIe routing	OK
RF-clean antenna routing, ≥ 1 RF connector or PCB antenna	OK
CAN-bus termination + ESD on both connectors	OK
Boot-mode DIP switch or hard-strap	OK
PORn and MODULE_EN accessible (button or test-point)	OK
Debug header on JTAG / SWD pins (optional but recommended)	OK
Correct firmware per SKU + target core	OK

Table 3 V2N carrier-board design checklist

11 Ordering Information

E1M-X V2N modules are ordered based on:

- Memory tier (32 Gbit / 64 Gbit LPDDR4X; 32 / 128 Gbit eMMC)
- Assembly options (lead finish, ball material)

Refer to the **E1M-X V2N Datasheet** (DS-V2N-001) §15 for the complete ordering matrix and MPN decoder.

12 Notices

- Specifications subject to change without notice.
- Some features may be preliminary at this revision.
- Always verify against the latest **E1M-X V2N Datasheet** (DS-V2N-001).
- This guide complements but does not replace the Renesas RZ/V2N PCB design guidelines ([r01an7339ej0100-rzv2n-pcb-design-guidelines.pdf](#)) for SoC-internal routing.

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