



E1M-X V2N-M1 – RENESAS RZ/V2N + DEEPX DX-M1

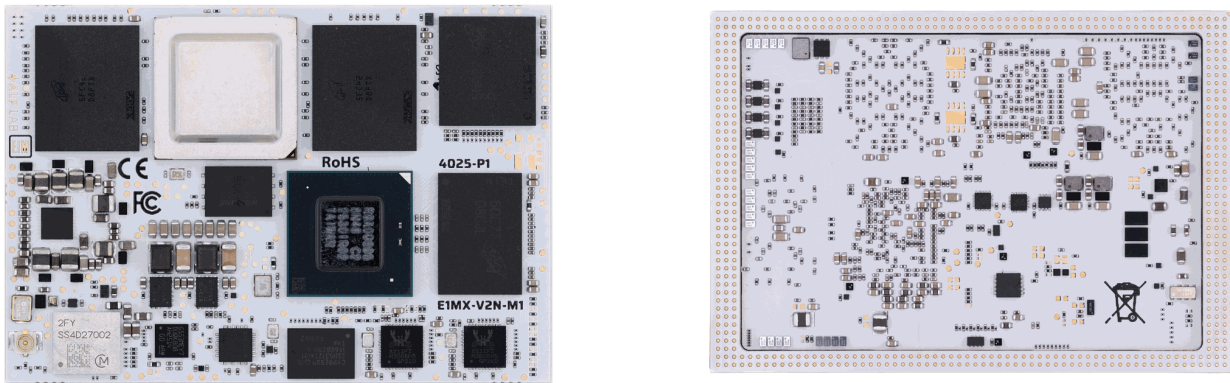


Figure 1 E1M-X V2N-M1 module – front (left) and back (right)

The E1M-X V2N-M1 module uses the open-source Edge-1 AI Module (E1M™) form factor, with a unified pin layout and hardware functionality. This footprint allows users to interchange MPU modules seamlessly while keeping hardware compatible. E1M™ is designed for flexibility, functionality, and longevity in high- and medium-range MCU/MPUs.

0.1 Features

- **Renesas RZ/V2N**
 - ▶ Quad Arm® Cortex®-A55 (1.8 GHz)
 - ▶ Arm Cortex-M33 (200 MHz)
 - ▶ Arm Mali™-C55 ISP (Image Signal Processor)
 - ▶ Arm Mali™-G31 GPU
 - ▶ AI Accelerator DRP-AI3 – 4 dense TOPS
 - ▶ H.264 / H.265 codec
- **DeepX DX-M1 standalone AI accelerator**
 - ▶ Up to **25 TOPS** AI performance
 - ▶ PCIe-attached on-module to the RZ/V2N
 - ▶ 2 × LPDDR5X companion memory
 - ▶ SPI NAND companion storage
- **Dedicated I/O MCU**
 - ▶ Arm® Cortex®-M33 (216 MHz)
- **Various memory options**
 - ▶ LPDDR4X 32-bit 3.2 GT/s, up to 8 GB
 - ▶ eMMC – 4 GB to 256 GB
 - ▶ SPI NOR – 128 Mbit, boot-supported
- **MIPI Display output** – 4 lanes
 - ▶ 1920 × 1200 RGB888 @ 60 fps
 - ▶ 1280 × 1024 RGB888 @ 120 fps
- **H.264 / H.265 codec**
 - ▶ H.264 1920 × 1080 × 60 fps
 - ▶ H.265 3840 × 2160p × 30 fps
- 2 × CSI-2 camera inputs – 4 lanes, up to 4K @ 30 fps, 4 virtual channels
- 2.4 GHz / 5 GHz / 6 GHz Wi-Fi® + Bluetooth® module
 - ▶ 802.11 a/b/g/n/ac/ax, 143 Mbps
 - ▶ Bluetooth® 5.4 BR/EDR/LE, 3 Mbps
- 2 × 1 Gbps Ethernet PHY
- 2 × CAN-BUS PHY
- PCIe Express® 3.0 – 2 lanes (multiplexed between on-module DeepX M1 and external)
- Assembly variants available for cost reduction
- Smallest size in the industry: 45 × 65 mm

0.2 Applications

IoT, industrial, robotics, motor drive, drones, mobile PoS, smart speakers, object detection, medical devices, vending machines, smart home, process control, smart appliances, scanners.

Table of Contents

| | | | | | |
|----------|---|-----------|-----------|--|-----------|
| 0.1 | Features | 1 | 8.8 | Microphone – PDM | 25 |
| 0.2 | Applications | 1 | 8.9 | Analog Inputs | 25 |
| 1 | General Description | 4 | 8.10 | Analog Outputs | 25 |
| 1.1 | Highlights | 4 | 9 | Components | 25 |
| 1.2 | Block Diagram | 4 | 9.1 | Wireless Module & Antenna | 25 |
| 1.3 | Module Variants | 4 | 9.1.1 | RF Characteristics | 25 |
| 1.4 | Renesas RZ/V2N MPU | 4 | 9.1.2 | Antenna Options | 26 |
| 1.5 | DeepX DX-M1 – Standalone AI Accelerator | 5 | 9.1.3 | Regulatory Information | 26 |
| 2 | Pin Diagram and List | 6 | 9.2 | Memories | 26 |
| 2.1 | Power & Control Pins | 7 | 9.3 | TPM 2.0 Module | 27 |
| 2.2 | Analog Pins | 8 | 9.4 | Real-Time Clock (RTC) | 27 |
| 2.3 | Digital Pins | 9 | 9.5 | PCB Temperature Sensor | 27 |
| 2.4 | Not Connected Pins | 13 | 10 | Environmental & Reliability | 27 |
| 2.5 | Reserved Pins | 16 | 10.1 | Operating & Storage Conditions | 27 |
| 3 | Specifications | 16 | 10.2 | Reflow Profile | 27 |
| 3.1 | Absolute Maximum Ratings | 16 | 10.3 | Reliability Data | 28 |
| 3.2 | Recommended Operating Conditions | 16 | 11 | Software & Operating System Support | 28 |
| 3.3 | Electrical Characteristics | 16 | 12 | Reference Schematic | 29 |
| 3.4 | ESD & Latch-up Ratings | 17 | 13 | Compliance & Certifications | 30 |
| 3.5 | Thermal Characteristics | 17 | 13.1 | Environmental Compliance | 30 |
| 4 | Power | 18 | 13.2 | Wireless Certifications | 30 |
| 4.1 | Power Architecture | 18 | 13.3 | Functional Safety & Industry-specific Compliance | 30 |
| 4.2 | Power-Up & Reset Sequence | 18 | 14 | Mechanical & Footprint Dimensions | 30 |
| 4.3 | Power Consumption | 19 | 14.1 | Module Dimensions | 30 |
| 4.4 | Boot Settings | 19 | 14.2 | Recommended PCB Land Pattern | 31 |
| 5 | Boot Modes | 20 | 14.3 | Keep-Out Zones | 31 |
| 6 | Reset & Module Enable | 20 | 14.4 | Module Marking | 32 |
| 7 | JTAG / SWD Debug | 21 | 15 | Packaging | 32 |
| 8 | Interfaces | 21 | 15.1 | Tape & Reel | 32 |
| 8.1 | Ethernet | 22 | 15.2 | Tray | 33 |
| 8.2 | USB | 22 | 15.3 | MSL & Handling | 33 |
| 8.3 | PCIe | 22 | 16 | Ordering Information | 34 |
| 8.4 | Serial Interfaces | 23 | 16.1 | MPN Decoder | 34 |
| 8.4.1 | I ² C | 23 | 16.2 | Ordering Matrix | 34 |
| 8.4.2 | I ³ C | 23 | 17 | References & Related Documents | 34 |
| 8.4.3 | UART | 23 | 18 | Revision History | 35 |
| 8.4.4 | SPI | 23 | 19 | Legal Notices | 35 |
| 8.4.5 | I ² S | 23 | 19.1 | Disclaimer | 35 |
| 8.4.6 | CAN Bus | 23 | 19.2 | Trademarks | 36 |
| 8.5 | SD Card | 23 | 19.3 | Export Control | 36 |
| 8.6 | MIPI DSI Display & Backlight Controller | 24 | 19.4 | Contact | 36 |
| 8.7 | MIPI CSI Camera | 24 | | | |

List of Figures

| | | | | | |
|-----------|--|----|-----------|--|----|
| Figure 1 | E1M-X V2N-M1 module – front (left) and back (right) | 1 | Figure 15 | E1M-X V2N-M1 SD Card Interface | 23 |
| Figure 2 | E1M-X V2N-M1 Block Diagram | 4 | Figure 16 | E1M-X V2N-M1 Display Connection with Backlight Driver | 24 |
| Figure 3 | Renesas RZ/V2N MPU Block Diagram | 5 | Figure 17 | E1M-X V2N-M1 Camera Connection with LDO | 24 |
| Figure 4 | DeepX DX-M1 Block Diagram | 6 | Figure 18 | E1M-X V2N-M1 PDM Connection Diagram | 25 |
| Figure 5 | E1M-X V2N-M1 Pin-out (top view, 496-pad LGA) | 7 | Figure 19 | E1M-X V2N-M1 Antenna Connection | 25 |
| Figure 6 | V2N-M1 power-dissipation derating curve (DRP-AI3 + DX-M1 combined) | 17 | Figure 20 | E1M-X V2N-M1 Memory Options | 26 |
| Figure 7 | E1M-X V2N-M1 Power Architecture Diagram | 18 | Figure 21 | E1M-X V2N-M1 Recommended Reflow Profile (Pb-free, SAC) | 28 |
| Figure 8 | V2N-M1 Power-Up Timing Diagram | 19 | Figure 22 | E1M-X V2N-M1 Minimum Reference Schematic | 29 |
| Figure 9 | E1M-X V2N-M1 Boot Flow | 20 | Figure 23 | E1M-X V2N-M1 Module Top & Side View | 30 |
| Figure 10 | V2N-M1 Reset Timing Diagram | 21 | Figure 24 | E1M-X V2N-M1 Recommended Land Pattern | 31 |
| Figure 11 | Reference JTAG / SWD Header Pinout | 21 | Figure 25 | E1M-X V2N-M1 Keep-Out Zones | 32 |
| Figure 12 | E1M-X V2N-M1 Ethernet PHY Connection | 22 | Figure 26 | E1M-X V2N-M1 Module Marking Layout | 32 |
| Figure 13 | E1M-X V2N-M1 PCIe MUX Connection | 22 | Figure 27 | Tape & Reel Drawing | 33 |
| Figure 14 | E1M-X V2N-M1 CAN-BUS Connection | 23 | Figure 28 | Tray Drawing | 33 |

List of Tables

| | | | | | |
|----------|---|----|----------|---|----|
| Table 1 | E1M-X V2N-M1 Variant Summary | 4 | Table 17 | E1M-X V2N-M1 USB Interface | 22 |
| Table 2 | E1M-X V2N-M1 Power & Control Pins | 7 | Table 18 | E1M-X V2N-M1 Wi-Fi 6 / BLE RF Characteristics | 25 |
| Table 3 | E1M-X V2N-M1 Analog Pins | 8 | Table 19 | Wireless Regulatory Approvals | 26 |
| Table 4 | E1M-X V2N-M1 Digital Pins | 9 | Table 20 | Environmental Conditions | 27 |
| Table 5 | E1M-X V2N-M1 Not-connected Pins | 13 | Table 21 | Reflow Profile Parameters (Pb-free) | 28 |
| Table 6 | E1M-X V2N-M1 Reserved Pins | 16 | Table 22 | Reliability Targets | 28 |
| Table 7 | E1M-X V2N-M1 Absolute Maximum Ratings | 16 | Table 23 | Software Support Matrix | 28 |
| Table 8 | E1M-X V2N-M1 Recommended Operating Conditions | 16 | Table 24 | Environmental Compliance | 30 |
| Table 9 | E1M-X V2N-M1 Electrical Characteristics | 16 | Table 25 | E1M-X V2N-M1 Mechanical Dimensions | 31 |
| Table 10 | E1M-X V2N-M1 ESD & Latch-up Ratings | 17 | Table 26 | Land Pattern Parameters | 31 |
| Table 11 | E1M-X V2N-M1 Thermal Characteristics | 17 | Table 27 | Tape & Reel Specifications | 33 |
| Table 12 | Module Output Rails | 18 | Table 28 | E1M-X V2N-M1 MPN Convention | 34 |
| Table 13 | E1M-X V2N-M1 Power Consumption (typical) | 19 | Table 29 | Ordering Information | 34 |
| Table 14 | E1M-X V2N-M1 Boot Options | 19 | Table 30 | Related Documents | 34 |
| Table 15 | Reset & Module Enable Signals | 20 | Table 31 | Revision History | 35 |
| Table 16 | JTAG / SWD Pinout | 21 | | | |

1 General Description

1.1 Highlights

The Alp Lab E1M-X V2N-M1 SoM (System-on-Module) is a high-performance, cost-effective solution designed for a range of AI-driven vision applications. Powered by the Renesas RZ/V2N processor **and** the DeepX standalone AI accelerator, it features an Arm® Quad Cortex®-A55 (1.8 GHz) CPU, an integrated AI accelerator, and a 4K encoder/decoder, making it optimised for vision-based tasks. The E1M-X V2N-M1 SoM supports up to two cameras via 2 × 4-lane MIPI CSI-2 connections and offers customisable options such as on-board Wi-Fi / Bluetooth, multiple memory and storage capacities, and PHY configurations.

1.2 Block Diagram

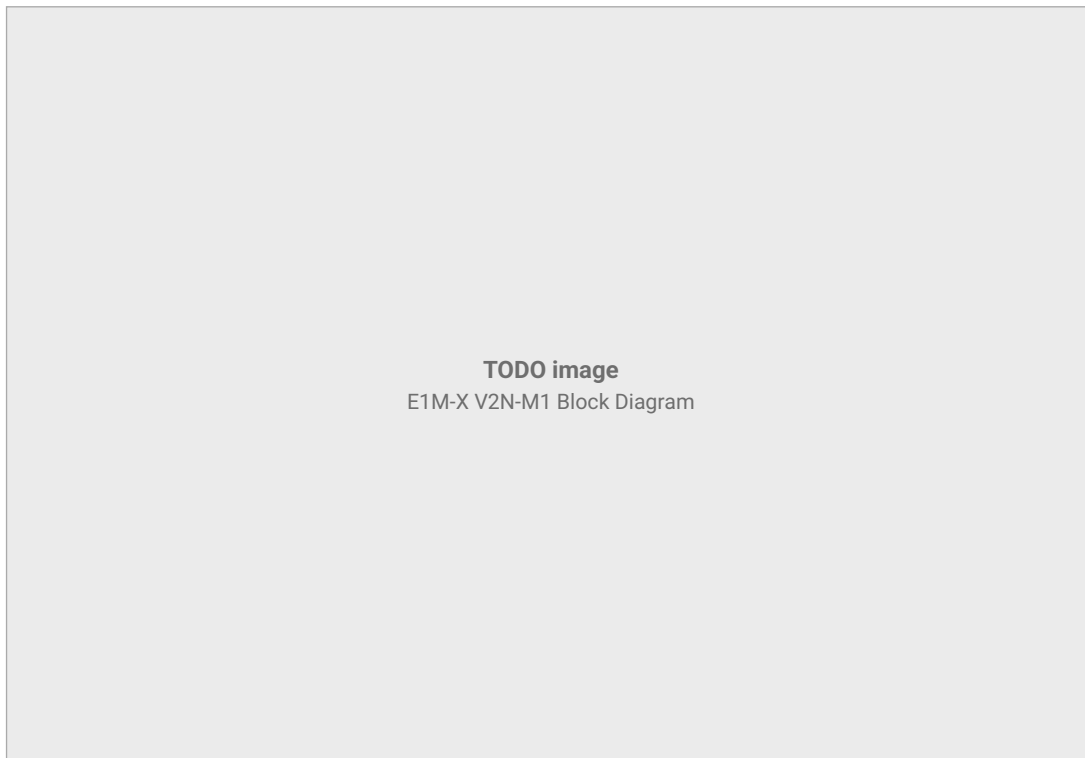


Figure 2 E1M-X V2N-M1 Block Diagram

1.3 Module Variants

The E1M-X V2N-M1 family ships in two MPN variants. Both populate the full V2N silicon stack **plus** the on-module DeepX DX-M1 accelerator and its companion memory; they differ only in the main-memory tier. See Section 16 for the full ordering matrix and MPN decoder.

| MPN | Renesas part | LPDDR4X | eMMC | AI capability |
|------------|---------------------|---------|--------------------|------------------------------|
| E1M-V2M101 | R9A09G056N44GBG#AC0 | 32 Gbit | eMMC 5.1, 32 Gbit | V2N: 4 TOPS + DX-M1: 25 TOPS |
| E1M-V2M102 | R9A09G056N44GBG#AC0 | 64 Gbit | eMMC 5.1, 128 Gbit | V2N: 4 TOPS + DX-M1: 25 TOPS |

Table 1 E1M-X V2N-M1 Variant Summary

1.4 Renesas RZ/V2N MPU

The RZ/V2N is a vision-AI microprocessor (MPU) with Renesas’ proprietary AI accelerator (DRP-AI3) supporting up to 15 TOPS of AI performance. Its CPUs are quad Arm® Cortex®-A55 (1.8 GHz) and Arm Cortex-M33 (200 MHz). The RZ/V2N is equipped with

an ISP (Image Signal Processor) and dual-channel MIPI® CSI-2® camera interfaces for supporting dual-camera signal processing, which is crucial for realising vision systems. It is also equipped with high-speed interfaces such as PCIe® and USB 3.2, allowing for the expansion of external devices. The RZ/V2N is an ideal microprocessor for applications requiring both low power consumption and advanced AI inference, such as DMS (Driver Monitoring System), monitoring cameras, mobile robots, and more.

This document should be read together with the V2N datasheet from Renesas.

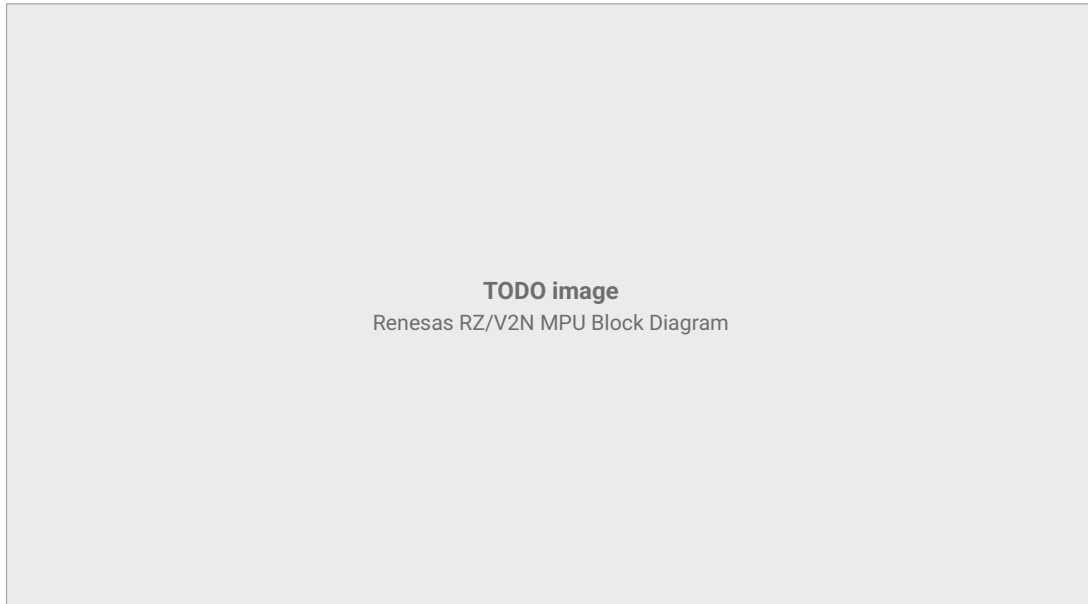


Figure 3 Renesas RZ/V2N MPU Block Diagram

Key MPU features:

- Cortex-A55 (1.8 GHz) × 4 cores
- Cortex-M33 (200 MHz) × 1 core
- AI Accelerator DRP-AI
- Arm Mali™-C55 ISP (option)
- 1.5 MB on-chip SRAM
- LPDDR4 / LPDDR4X memory interface
- Gigabit Ethernet 2 ch
- USB 2.0 interface 1 ch (Host/Function)
- USB 3.2 (Gen2) interface 1 ch (Host only)
- PCIe interface (Gen3, 2-lane) 1 ch
- MIPI CSI-2 camera interface 2 ch
- CAN interface (CAN FD) 6 ch
- AD converter 24 ch

1.5 DeepX DX-M1 – Standalone AI Accelerator

The DX-M1 is a 25 TOPS AI processor with class-leading power efficiency. DeepX designed the DX-M1 with the highest IPS (inference-per-second) per watt as a main goal. It is used as an AI accelerator with a host. The DX-M1 NPU is designed for deep-learning algorithm coverage including computer-vision tasks such as image classification, object detection, and identification of audio streams (e.g. keyword spotting). To speed up software development, DeepX provides a comprehensive software environment that includes an SDK and a model-zoo verified on DX-M1. The DX-COM™ tool automatically converts neural networks built in popular frameworks (PyTorch, ONNX, ...) into optimised executable code for the DX-M1.

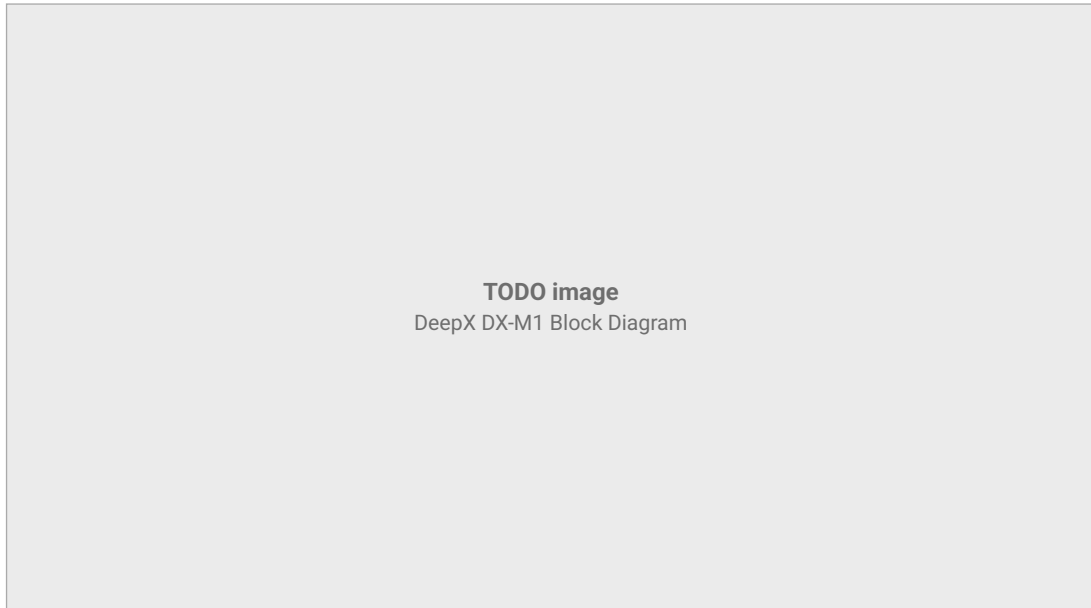


Figure 4 DeepX DX-M1 Block Diagram

2 Pin Diagram and List

The E1M-X™ standard defines the primary pin functions; the pin-out below follows that standard. Pins can be reassigned to alternate functions in software, but hardware compatibility with other E1M-X variants will no longer hold because each MCU/MPU has a different pin structure and peripheral mapping.

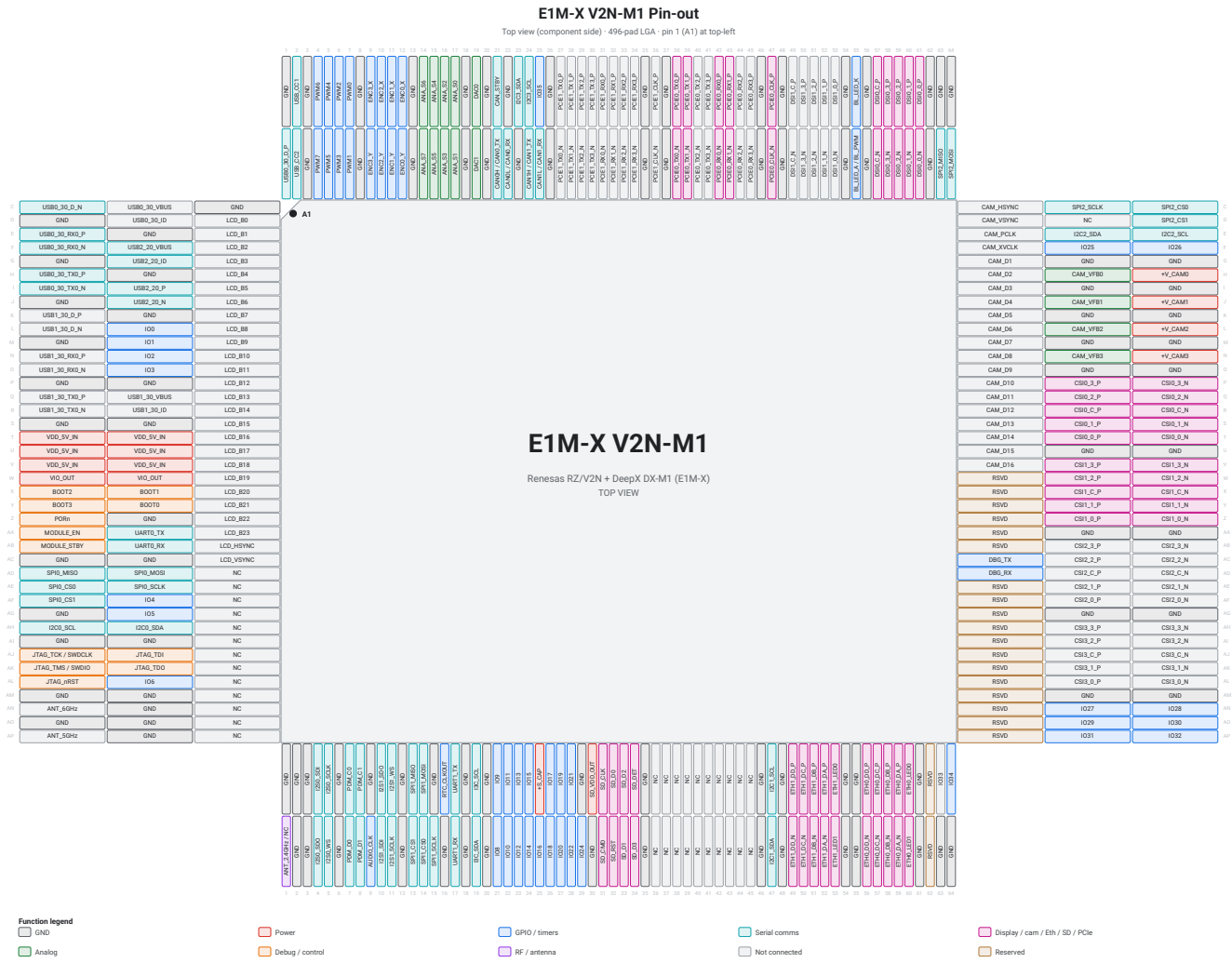


Figure 5 E1M-X V2N-M1 Pin-out (top view, 496-pad LGA)

2.1 Power & Control Pins

| Pin Number | Pin Name | Description |
|---|-----------|--|
| A13, K63, AQ15, M1, M63, O63, A18, AQ18, P1, A20, AQ20, S1, A22, U63, A26, AA63, AQ29, AC1, AQ6, D1, A35, AG1, AG63, AQ35, A37, AI1, AM1, AM63, A01, AQ1, A46, AQ46, AR63, A48, AQ48, A8, A54, AQ54, AQ55, A56, AQ61, A62, AQ9, G1, G63, I63, AQ12, J1, A1, A3, A63, AQ3, C3, K64, M64, O64, U64, AA64, AG64, AM64, AR64, G64, I64, A64, AR16, AR18, AR20, AR30, AR6, AR35, AR46, AR48, AR54, AR55, AR61, AR12, AR3, B13, K2, B18, P2, B20, S2, B23, B26, Z2, AC2, B35, AI2, B37, AM2, AN2, A02, E2, AP2, AQ2, AR2, B46, B48, B8, B54, B56, B62, H2, B3 | GND | Connect to ground. |
| W1, W2 | VIO_OUT | +1V8 output for I/O power. Up to TBD mA. |
| T1, U1, V1, T2, U2, V2 | VDD_5V_IN | +5 V main supply input to the module. |
| AQ25 | +S_CAP | External super-capacitor connection. |

| Pin Number | Pin Name | Description |
|------------|-------------------|---|
| Y2 | B00T0 | Boot selection for Renesas RZ/V2N. See Section 4.4. |
| X2 | B00T1 | |
| X1 | B00T2 | Not connected. Leave floating. |
| Y1 | B00T3 | Boot CPU selection. High: RZ/V2N internal CA55 boot. Low: RZ/V2N internal CM33 boot. |
| AL1 | JTAG_nRST | JTAG / SWD pins for programming and debug. |
| AJ1 | JTAG_TCK / SWDCLK | |
| AJ2 | JTAG_TDI | |
| AK2 | JTAG_TDO | |
| AK1 | JTAG_TMS / SWDIO | |
| AA1 | MODULE_EN | Module enable. Open-drain. Pulled up internally to VDD. Connect to GND to disable the module; leave floating if not used. |
| Z1 | PORn | Reset input. Open-drain. Pulled up internally to 1V8. Pull low to reset the module; leave floating if not used. |
| AB1 | MODULE_STBY | Module stand-by request. Open-drain, pulled up internally to 1V8. Leave floating if not used. |
| A2 | USB_CC1 | USB Type-C Configuration Channel 1. |
| B2 | USB_CC2 | USB Type-C Configuration Channel 2. |
| AQ30 | SD_VDD_OUT | SD-card voltage output. Connect to SD card VDD. |
| H64 | +V_CAM0 | CAM0 LDO output. 0.6 V to 3.3 V, 300 mA max. |
| J64 | +V_CAM1 | CAM1 LDO output. 0.6 V to 3.3 V, 300 mA max. |
| L64 | +V_CAM2 | CAM2 LDO output. 0.6 V to 3.3 V, 300 mA max. |
| N64 | +V_CAM3 | CAM3 LDO output. 0.6 V to 3.3 V, 300 mA max. |
| H63 | CAM_VFB0 | Feedback node for +V_CAM0. Place divider close to the module pin. |
| J63 | CAM_VFB1 | Feedback node for +V_CAM1. Place divider close to the module pin. |
| L63 | CAM_VFB2 | Feedback node for +V_CAM2. Place divider close to the module pin. |
| N63 | CAM_VFB3 | Feedback node for +V_CAM3. Place divider close to the module pin. |
| B55 | BL_LED_A / BL_PWM | BL_LED_A: anode of backlight. BL_PWM: connect to backlight driver. |
| A55 | BL_LED_K | Cathode of backlight. Leave floating if BL_PWM is used. |

Table 2 E1M-X V2N-M1 Power & Control Pins

2.2 Analog Pins

| Pin Number | Pin Name | Peripheral | Description |
|------------|----------|------------|--|
| A17 | ANA_S0 | AIN | Analogue input channels, referenced to 1V8. |
| B17 | ANA_S1 | | |
| A16 | ANA_S2 | | |
| B16 | ANA_S3 | | |
| A15 | ANA_S4 | | |
| B15 | ANA_S5 | | |
| A14 | ANA_S6 | | |
| B14 | ANA_S7 | | |
| A19 | DAC0 | DAC0 | Analogue output channels, referenced to 1V8. |
| B19 | DAC1 | DAC1 | |

| Pin Number | Pin Name | Peripheral | Description |
|------------|-----------------|------------|--|
| AR1 | ANT_2.4GHz / NC | | ANT: module antenna output for Wi-Fi 6 and BLE. Route 50 Ω trace. NC: leave floating. |

Table 3 E1M-X V2N-M1 Analog Pins

2.3 Digital Pins

| Pin Number | Pin Name | Peripheral | Description |
|------------|------------|-------------|--|
| AR21 | I08 | GPIO / SMCU | General purpose I/O, controlled by the secondary MCU on E1M-X. |
| AQ21 | I09 | | |
| AR22 | I010 | | |
| AQ22 | I011 | | |
| AR23 | I012 | | |
| AQ23 | I013 | | |
| AR24 | I014 | | |
| AQ24 | I015 | | |
| AR25 | I016 | | |
| F63 | I025 | | |
| F64 | I026 | | |
| AN63 | I027 | | |
| AN64 | I028 | | |
| A063 | I029 | | |
| A064 | I030 | | |
| AP63 | I031 | | |
| AP64 | I032 | | |
| AQ64 | I034 | | |
| A25 | I035 | | |
| AQ16 | RTC_CLKOUT | RTC | Real-time clock output. |
| AC62 | DBG_TX | DBG | On-module debug UART transmit. |
| AD62 | DBG_RX | DBG | On-module debug UART receive. |
| L2 | I00 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| M2 | I01 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| N2 | I02 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| O2 | I03 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AF2 | I04 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AG2 | I05 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AL2 | I06 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AQ26 | I017 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AR26 | I018 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AQ27 | I019 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AR27 | I020 | GPIO | General-purpose I0. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |

| Pin Number | Pin Name | Peripheral | Description |
|------------|-----------------|------------|--|
| AQ28 | I021 | GPIO | General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AR28 | I022 | GPIO | General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AR29 | I024 | GPIO | General-purpose IO. Routed to the on-module DX-M1; available as carrier GPIO after a DeepX software patch. |
| AR9 | AUDIO_CLK | – | Audio clock output. |
| AQ7 | PDM_C0 | PDM0 | Digital microphone interface. PDM_C is the clock, PDM_D is the data line. |
| AR7 | PDM_D0 | | |
| AQ8 | PDM_C1 | PDM1 | Digital microphone interface. |
| AR8 | PDM_D1 | | |
| AQ5 | I2S0_SCLK | I2S0 | I ² S interface. |
| AQ4 | I2S0_SDI | | |
| AR4 | I2S0_SDO | | |
| AR5 | I2S0_WS | | |
| AR11 | I2S1_SCLK | I2S1 | I ² S interface. |
| AR10 | I2S1_SDI | | |
| AQ10 | I2S1_SDO | | |
| AQ11 | I2S1_WS | | |
| AH1 | I2C0_SCL | I2C0 | I ² C interface. |
| AH2 | I2C0_SDA | | |
| AQ47 | I2C1_SCL | I2C1 | I ² C interface. |
| AR47 | I2C1_SDA | | |
| E64 | I2C2_SCL | I2C2 | I ² C interface. |
| E63 | I2C2_SDA | | |
| A24 | I2C3_SCL | I2C3 | I ² C interface, controlled by the secondary MCU on E1M-X. |
| A23 | I2C3_SDA | | |
| AQ19 | I3C_SCL | I3C | I ³ C interface. |
| AR19 | I3C_SDA | | |
| AE1 | SPI0_CS0 | SPI0 | SPI interface. |
| AF1 | SPI0_CS1 | | |
| AD1 | SPI0_MISO | | |
| AD2 | SPI0_MOSI | | |
| AE2 | SPI0_SCLK | | |
| AR14 | SPI1_CS0 | SPI1 | SPI interface. |
| AR13 | SPI1_CS1 | | |
| AQ13 | SPI1_MISO | | |
| AQ14 | SPI1_MOSI | | |
| AR15 | SPI1_SCLK | | |
| C64 | SPI2_CS0 | SPI2 | SPI interface. |
| D64 | SPI2_CS1 | | |
| B63 | SPI2_MISO | | |
| B64 | SPI2_MOSI | | |
| C63 | SPI2_SCLK | | |
| AB2 | UART0_RX | UART0 | UART interface. |
| AA2 | UART0_TX | | |
| AR17 | UART1_RX | UART1 | UART interface. |
| AQ17 | UART1_TX | | |
| B21 | CAN0H / CAN0_TX | CAN0 | CAN-BUS interface. |
| B22 | CAN0L / CAN0_RX | | |

| Pin Number | Pin Name | Peripheral | Description |
|------------|-----------------|------------|---|
| B24 | CAN1H / CAN1_TX | CAN1 | CAN-BUS interface. |
| B25 | CAN1L / CAN1_RX | | |
| A21 | CAN_STBY | CAN | Standby control for CAN-BUS. |
| A7 | PWM0 | PWM | PWM output, controlled by the secondary MCU on E1M-X. |
| B7 | PWM1 | | |
| A6 | PWM2 | | |
| B6 | PWM3 | | |
| A5 | PWM4 | | |
| B5 | PWM5 | | |
| A4 | PWM6 | | |
| B4 | PWM7 | | |
| A12 | ENC0_X | ENC0 | Encoder input. |
| B12 | ENC0_Y | | |
| A11 | ENC1_X | ENC1 | Encoder input. |
| B11 | ENC1_Y | | |
| A10 | ENC2_X | ENC2 | Encoder input. |
| B10 | ENC2_Y | | |
| A9 | ENC3_X | ENC3 | Encoder input. |
| B9 | ENC3_Y | | |
| AR56 | ETH0_DD_N | ETH0 | Ethernet interface. 1 Gbit PHY connection. |
| AQ56 | ETH0_DD_P | | |
| AR57 | ETH0_DC_N | | |
| AQ57 | ETH0_DC_P | | |
| AR58 | ETH0_DB_N | | |
| AQ58 | ETH0_DB_P | | |
| AR59 | ETH0_DA_N | | |
| AQ59 | ETH0_DA_P | | |
| AQ60 | ETH0_LED0 | | |
| AR60 | ETH0_LED1 | | |
| AR49 | ETH1_DD_N | ETH1 | Ethernet interface. 1 Gbit PHY connection. |
| AQ49 | ETH1_DD_P | | |
| AR50 | ETH1_DC_N | | |
| AQ50 | ETH1_DC_P | | |
| AR51 | ETH1_DB_N | | |
| AQ51 | ETH1_DB_P | | |
| AR52 | ETH1_DA_N | | |
| AQ52 | ETH1_DA_P | | |
| AQ53 | ETH1_LED0 | | |
| AR53 | ETH1_LED1 | | |
| AQ31 | SD_CLK | SD0 | SD card or eMMC interface. |
| AR31 | SD_CMD | | |
| AQ32 | SD_D0 | | |
| AR33 | SD_D1 | | |
| AQ33 | SD_D2 | | |
| AR34 | SD_D3 | | |
| AQ34 | SD_DET | | |
| AR32 | SD_RST | | |
| T64 | CSI0_0_N | CSI0 | MIPI CSI camera interface. |
| T63 | CSI0_0_P | | |
| S64 | CSI0_1_N | | |

| Pin Number | Pin Name | Peripheral | Description |
|------------|---------------|------------|---|
| S63 | CSI0_1_P | | |
| Q64 | CSI0_2_N | | |
| Q63 | CSI0_2_P | | |
| P64 | CSI0_3_N | | |
| P63 | CSI0_3_P | | |
| R64 | CSI0_C_N | | |
| R63 | CSI0_C_P | | |
| Z64 | CSI1_0_N | CSI1 | MIPI CSI camera interface. |
| Z63 | CSI1_0_P | | |
| Y64 | CSI1_1_N | | |
| Y63 | CSI1_1_P | | |
| W64 | CSI1_2_N | | |
| W63 | CSI1_2_P | | |
| V64 | CSI1_3_N | | |
| V63 | CSI1_3_P | | |
| X64 | CSI1_C_N | | |
| X63 | CSI1_C_P | | |
| B61 | DSI0_0_N | DSI0 | MIPI DSI display interface. |
| A61 | DSI0_0_P | | |
| B60 | DSI0_1_N | | |
| A60 | DSI0_1_P | | |
| B59 | DSI0_2_N | | |
| A59 | DSI0_2_P | | |
| B58 | DSI0_3_N | | |
| A58 | DSI0_3_P | | |
| B57 | DSI0_C_N | | |
| A57 | DSI0_C_P | | |
| B47 | PCIE0_CLK_N | PCIE0 | PCIe interface (multiplexed with on-module DeepX M1). |
| A47 | PCIE0_CLK_P | | |
| B42 | PCIE0_RX0_N | | |
| A42 | PCIE0_RX0_P | | |
| B43 | PCIE0_RX1_N | | |
| A43 | PCIE0_RX1_P | | |
| B38 | PCIE0_TX0_N | | |
| A38 | PCIE0_TX0_P | | |
| B39 | PCIE0_TX1_N | | |
| A39 | PCIE0_TX1_P | | |
| C1 | USB0_30_D_N | USB0 | USB 3.0 interface. |
| B1 | USB0_30_D_P | | |
| F1 | USB0_30_RX0_N | | |
| E1 | USB0_30_RX0_P | | |
| I1 | USB0_30_TX0_N | | |
| H1 | USB0_30_TX0_P | | |
| G2 | USB2_20_ID | USB2 | USB 2.0 interface. |
| J2 | USB2_20_N | | |
| I2 | USB2_20_P | | |
| F2 | USB2_20_VBUS | | |

Table 4 E1M-X V2N-M1 Digital Pins

2.4 Not Connected Pins

These pins carry an E1M-X™ standard function that is not implemented on the V2N-M1 module. They retain their standard name for cross-variant compatibility and must be left floating.

| Pin Number | Pin Name | Description |
|------------|-------------|-----------------|
| A27 | PCIE1_TX0_P | Leave floating. |
| A28 | PCIE1_TX1_P | Leave floating. |
| A29 | PCIE1_TX2_P | Leave floating. |
| A30 | PCIE1_TX3_P | Leave floating. |
| A31 | PCIE1_RX0_P | Leave floating. |
| A32 | PCIE1_RX1_P | Leave floating. |
| A33 | PCIE1_RX2_P | Leave floating. |
| A34 | PCIE1_RX3_P | Leave floating. |
| A36 | PCIE1_CLK_P | Leave floating. |
| A40 | PCIE0_TX2_P | Leave floating. |
| A41 | PCIE0_TX3_P | Leave floating. |
| A44 | PCIE0_RX2_P | Leave floating. |
| A45 | PCIE0_RX3_P | Leave floating. |
| A49 | DSI1_C_P | Leave floating. |
| A50 | DSI1_3_P | Leave floating. |
| A51 | DSI1_2_P | Leave floating. |
| A52 | DSI1_1_P | Leave floating. |
| A53 | DSI1_0_P | Leave floating. |
| AA3 | LCD_B23 | Leave floating. |
| AB3 | LCD_HSYNC | Leave floating. |
| AB63 | CSI2_3_P | Leave floating. |
| AB64 | CSI2_3_N | Leave floating. |
| AC3 | LCD_VSYNC | Leave floating. |
| AC63 | CSI2_2_P | Leave floating. |
| AC64 | CSI2_2_N | Leave floating. |
| AD3 | NC | Leave floating. |
| AD63 | CSI2_C_P | Leave floating. |
| AD64 | CSI2_C_N | Leave floating. |
| AE3 | NC | Leave floating. |
| AE63 | CSI2_1_P | Leave floating. |
| AE64 | CSI2_1_N | Leave floating. |
| AF3 | NC | Leave floating. |
| AF63 | CSI2_0_P | Leave floating. |
| AF64 | CSI2_0_N | Leave floating. |
| AG3 | NC | Leave floating. |
| AH3 | NC | Leave floating. |
| AH63 | CSI3_3_P | Leave floating. |
| AH64 | CSI3_3_N | Leave floating. |
| AI3 | NC | Leave floating. |
| AI63 | CSI3_2_P | Leave floating. |
| AI64 | CSI3_2_N | Leave floating. |
| AJ3 | NC | Leave floating. |
| AJ63 | CSI3_C_P | Leave floating. |
| AJ64 | CSI3_C_N | Leave floating. |
| AK3 | NC | Leave floating. |
| AK63 | CSI3_1_P | Leave floating. |

| Pin Number | Pin Name | Description |
|------------|--------------|-----------------|
| AK64 | CSI3_1_N | Leave floating. |
| AL3 | NC | Leave floating. |
| AL63 | CSI3_0_P | Leave floating. |
| AL64 | CSI3_0_N | Leave floating. |
| AM3 | NC | Leave floating. |
| AN1 | ANT_6GHz | Leave floating. |
| AN3 | NC | Leave floating. |
| A03 | NC | Leave floating. |
| AP1 | ANT_5GHz | Leave floating. |
| AP3 | NC | Leave floating. |
| AQ36 | NC | Leave floating. |
| AQ37 | NC | Leave floating. |
| AQ38 | NC | Leave floating. |
| AQ39 | NC | Leave floating. |
| AQ40 | NC | Leave floating. |
| AQ41 | NC | Leave floating. |
| AQ42 | NC | Leave floating. |
| AQ43 | NC | Leave floating. |
| AQ44 | NC | Leave floating. |
| AQ45 | NC | Leave floating. |
| AQ63 | I033 | Leave floating. |
| AR36 | NC | Leave floating. |
| AR37 | NC | Leave floating. |
| AR38 | NC | Leave floating. |
| AR39 | NC | Leave floating. |
| AR40 | NC | Leave floating. |
| AR41 | NC | Leave floating. |
| AR42 | NC | Leave floating. |
| AR43 | NC | Leave floating. |
| AR44 | NC | Leave floating. |
| AR45 | NC | Leave floating. |
| B27 | PCIE1_TX0_N | Leave floating. |
| B28 | PCIE1_TX1_N | Leave floating. |
| B29 | PCIE1_TX2_N | Leave floating. |
| B30 | PCIE1_TX3_N | Leave floating. |
| B31 | PCIE1_RX0_N | Leave floating. |
| B32 | PCIE1_RX1_N | Leave floating. |
| B33 | PCIE1_RX2_N | Leave floating. |
| B34 | PCIE1_RX3_N | Leave floating. |
| B36 | PCIE1_CLK_N | Leave floating. |
| B40 | PCIE0_TX2_N | Leave floating. |
| B41 | PCIE0_TX3_N | Leave floating. |
| B44 | PCIE0_RX2_N | Leave floating. |
| B45 | PCIE0_RX3_N | Leave floating. |
| B49 | DSI1_C_N | Leave floating. |
| B50 | DSI1_3_N | Leave floating. |
| B51 | DSI1_2_N | Leave floating. |
| B52 | DSI1_1_N | Leave floating. |
| B53 | DSI1_0_N | Leave floating. |
| C2 | USB0_30_VBUS | Leave floating. |

| Pin Number | Pin Name | Description |
|------------|---------------|-----------------|
| C62 | CAM_HSYNC | Leave floating. |
| D2 | USB0_30_ID | Leave floating. |
| D3 | LCD_B0 | Leave floating. |
| D62 | CAM_VSYNC | Leave floating. |
| D63 | NC | Leave floating. |
| E3 | LCD_B1 | Leave floating. |
| E62 | CAM_PCLK | Leave floating. |
| F3 | LCD_B2 | Leave floating. |
| F62 | CAM_XVCLK | Leave floating. |
| G3 | LCD_B3 | Leave floating. |
| G62 | CAM_D1 | Leave floating. |
| H3 | LCD_B4 | Leave floating. |
| H62 | CAM_D2 | Leave floating. |
| I3 | LCD_B5 | Leave floating. |
| I62 | CAM_D3 | Leave floating. |
| J3 | LCD_B6 | Leave floating. |
| J62 | CAM_D4 | Leave floating. |
| K1 | USB1_30_D_P | Leave floating. |
| K3 | LCD_B7 | Leave floating. |
| K62 | CAM_D5 | Leave floating. |
| L1 | USB1_30_D_N | Leave floating. |
| L3 | LCD_B8 | Leave floating. |
| L62 | CAM_D6 | Leave floating. |
| M3 | LCD_B9 | Leave floating. |
| M62 | CAM_D7 | Leave floating. |
| N1 | USB1_30_RX0_P | Leave floating. |
| N3 | LCD_B10 | Leave floating. |
| N62 | CAM_D8 | Leave floating. |
| O1 | USB1_30_RX0_N | Leave floating. |
| O3 | LCD_B11 | Leave floating. |
| O62 | CAM_D9 | Leave floating. |
| P3 | LCD_B12 | Leave floating. |
| P62 | CAM_D10 | Leave floating. |
| Q1 | USB1_30_TX0_P | Leave floating. |
| Q2 | USB1_30_VBUS | Leave floating. |
| Q3 | LCD_B13 | Leave floating. |
| Q62 | CAM_D11 | Leave floating. |
| R1 | USB1_30_TX0_N | Leave floating. |
| R2 | USB1_30_ID | Leave floating. |
| R3 | LCD_B14 | Leave floating. |
| R62 | CAM_D12 | Leave floating. |
| S3 | LCD_B15 | Leave floating. |
| S62 | CAM_D13 | Leave floating. |
| T3 | LCD_B16 | Leave floating. |
| T62 | CAM_D14 | Leave floating. |
| U3 | LCD_B17 | Leave floating. |
| U62 | CAM_D15 | Leave floating. |
| V3 | LCD_B18 | Leave floating. |
| V62 | CAM_D16 | Leave floating. |
| W3 | LCD_B19 | Leave floating. |

| Pin Number | Pin Name | Description |
|------------|----------|-----------------|
| X3 | LCD_B20 | Leave floating. |
| Y3 | LCD_B21 | Leave floating. |
| Z3 | LCD_B22 | Leave floating. |

Table 5 E1M-X V2N-M1 Not-connected Pins

2.5 Reserved Pins

| Pin Number | Pin Name | Description |
|--|----------|---|
| W62, X62, Y62, Z62, AA62, AB62, AE62, AF62, AG62, AH62, AI62, AJ62, AK62, AL62, AM62, AN62, AO62, AP62, AQ62, AR62 | RSVD | Do not connect. Used for production purposes. |

Table 6 E1M-X V2N-M1 Reserved Pins

3 Specifications

3.1 Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|----------------------|--------------|-------|------|------|
| Power-supply voltage | VDDIN to GND | - 0.3 | 6.0 | V |
| Analog input voltage | V(ANA_Sx) | - 0.3 | 1.98 | V |
| Digital IO (1V8) | | - 0.3 | 1.98 | V |

Table 7 E1M-X V2N-M1 Absolute Maximum Ratings

Warning: Stresses beyond Absolute Maximum Ratings may cause permanent damage. Operation at these conditions is not implied.

3.2 Recommended Operating Conditions

The module is specified to meet the Electrical Characteristics in Section 3.3 over the conditions below. Operation outside this range is not guaranteed.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|----------------|------|-----|-----|------|
| Module supply voltage | VDDIN | 4.5 | 5.0 | 5.5 | V |
| Ambient operating temperature | T _A | - 40 | - | +85 | °C |
| Junction operating temperature | T _J | - | - | TBD | °C |
| Relative humidity (operating, non-condensing) | RH | TBD | - | TBD | % |

Table 8 E1M-X V2N-M1 Recommended Operating Conditions

3.3 Electrical Characteristics

| Symbol | Description | Min | Nom | Max | Unit |
|----------------------|----------------------------------|-----|-----|-----|------|
| Power supply | | | | | |
| VDDIN | Module power supply | 4.5 | 5.0 | 5.5 | V |
| I _{DDMAX} | Maximum I _{DD} current | | | TBD | |
| SD_VDD_OUT | SD-card supply (high-speed mode) | | 1.8 | | V |
| SD_VDD_OUT | SD-card supply (low-speed mode) | | 3.3 | | V |
| Analog inputs | | | | | |
| V(AINx) | Input voltage | 0 | - | 1.8 | V |
| Digital IOs | | | | | |

| Symbol | Description | Min | Nom | Max | Unit |
|--------------------|---------------------------|-----|-----|-----|------|
| V _{OL} | Low-level output voltage | | | | |
| V _{OH} | High-level output voltage | | | | |
| V _{IL} | Low-level input voltage | | | | |
| V _{IH} | High-level input voltage | | | | |
| Camera LDOs | | | | | |
| +V_CAM0 | CAM0 LDO output | 0.6 | – | 3.3 | V |
| +V_CAM1 | CAM1 LDO output | 0.6 | – | 3.3 | V |
| +V_CAM2 | CAM2 LDO output | 0.6 | – | 3.3 | V |
| +V_CAM3 | CAM3 LDO output | 0.6 | – | 3.3 | V |

Table 9 E1M-X V2N-M1 Electrical Characteristics

3.4 ESD & Latch-up Ratings

ESD ratings apply at module-level – i.e. directly to the LGA pads as exposed to a carrier-board assembly process. Customer ESD protection requirements on the carrier board are described in the relevant interface sub-sections.

| Parameter | Standard | Min | Max | Unit |
|----------------------------|------------------------|-----|-----|------|
| Human Body Model (HBM) | ANSI/ESDA/JEDEC JS-001 | – | TBD | V |
| Charged Device Model (CDM) | ANSI/ESDA/JEDEC JS-002 | – | TBD | V |
| Latch-up | JESD78 | – | TBD | mA |

Table 10 E1M-X V2N-M1 ESD & Latch-up Ratings

3.5 Thermal Characteristics

The E1M-X V2N-M1 dissipates heat through both the Renesas RZ/V2N SoC and the on-module DeepX DX-M1 accelerator. Sustained AI workloads run both heat sources concurrently; an active heatsink or forced-air cooling is recommended above 50% DX-M1 utilisation at +25 °C ambient. Thermal-resistance figures below assume a 45 × 65 mm module mounted on a 4-layer FR4 carrier with a ground-plane heatsink.

| Parameter | Symbol | Typ | Max | Unit |
|---|-------------------------|-----|-----|-------|
| Thermal resistance, junction-to-ambient (RZ/V2N, still air) | $\theta_{JA, V2N}$ | TBD | – | °C/W |
| Thermal resistance, junction-to-ambient (DX-M1, still air) | $\theta_{JA, M1}$ | TBD | – | °C/W |
| Maximum junction temperature (RZ/V2N) | T _{J,max, V2N} | – | TBD | °C |
| Maximum junction temperature (DX-M1) | T _{J,max, M1} | – | TBD | °C |
| Power dissipation derating (above +85 °C) | P _D | TBD | – | mW/°C |

Table 11 E1M-X V2N-M1 Thermal Characteristics



Figure 6 V2N-M1 power-dissipation derating curve (DRP-AI3 + DX-M1 combined)

4 Power

4.1 Power Architecture

All power rails on the module are generated and managed on-board from a single externally-supplied 5 V input on VDD_5V_IN. On-module power management is performed by an I²C-controlled PMIC (Renesas DA9292) plus a GD32 supervisor MCU (Cortex-M33 @ 216 MHz) that orchestrates rail sequencing for the RZ/V2N, the DeepX DX-M1, and the M1's companion LPDDR5X memory.

The E1M-X V2N-M1 includes all necessary decoupling capacitors. Additional decoupling capacitors on the carrier board may improve performance further.

The module exposes two regulated output rails to the carrier:

| Rail | Pins | Voltage | Max current | Purpose |
|------------|--------|------------------|-------------|--|
| VIO_OUT | W1, W2 | 1.8 V ± 5% | TBD mA | I/O reference for carrier-side level shifters. |
| SD_VDD_OUT | AQ30 | 1.8 / 3.3 V auto | 300 mA | microSD slot supply; auto-switches for high/low-speed modes. |

Table 12 Module Output Rails



Figure 7 E1M-X V2N-M1 Power Architecture Diagram

Note: The DX-M1's internal power rails (LPDDR5X, NPU core, SPI NAND) are entirely on-module and not exposed to the carrier. The GD32 supervisor brings them up sequentially after VDD_5V_IN stabilises.

4.2 Power-Up & Reset Sequence

The recommended power-up sequence is:

1. Apply 5 V to VDD_5V_IN.
2. Release MODULE_EN (let internal pull-up hold high).
3. Release PORn (let internal pull-up hold high).
4. Wait for the on-module power-up to complete. Internal rails (including the DX-M1 sub-system) stabilise within TBD ms of MODULE_EN release (longer than V2N because of the M1's LPDDR5X bring-up). The module exposes no ready-strobe output, so allow this fixed delay before driving signals into the module.
5. Begin communication with the module.



Figure 8 V2N-M1 Power-Up Timing Diagram

Note: For power-down, drive MODULE_EN low and remove VDD_5V_IN. The module does not require a controlled power-down sequence at the carrier-board level.

4.3 Power Consumption

Numbers below are typical at $T_A = +25\text{ }^\circ\text{C}$, VDDIN = 5.0 V. The DX-M1 baseline draw (always on once the module has powered up) is the main delta vs the V2N family.

| Mode | Description | Min | Typ | Max | Unit |
|--|----------------------------------|-----|-----|-----|---------------|
| Active | | | | | |
| A55 quad + DRP-AI3 + DX-M1 @ full load | Combined AI inference at 29 TOPS | – | TBD | TBD | mA |
| A55 quad + DX-M1 only | Single-NPU offload | – | TBD | TBD | mA |
| A55 quad + DRP-AI3 only (DX-M1 idle) | V2N-equivalent workload | – | TBD | TBD | mA |
| A55 quad @ 1.8 GHz, no AI | General Linux compute | – | TBD | TBD | mA |
| Active, with dual Ethernet + PCIe SSD + display + camera | Full-feature workload | – | TBD | TBD | mA |
| Low-power | | | | | |
| Idle (DX-M1 in reset) | Cores halted, M1 gated | – | TBD | – | mA |
| Sleep | Retention only, RTC running | – | TBD | – | μA |
| Shutdown (MODULE_EN low) | Module disabled | – | TBD | – | μA |

Table 13 E1M-X V2N-M1 Power Consumption (typical)

4.4 Boot Settings

E1M-X V2N-M1 supports several boot options selected by the BOOT0–BOOT3 strap pins on the carrier.

| BOOT1 | BOOT0 | Boot mode | Device | CA55 boot | CM33 boot |
|-------|-------|-----------|------------------------------|-----------|---------------|
| 0 | 0 | Mode 0 | eSD (3.3 V for execution) | Supported | Not supported |
| 0 | 1 | Mode 1 | eMMC (I/O voltage 1.8 V) | Supported | Not supported |
| 1 | 0 | Mode 2 | QSPI NOR (I/O voltage 1.8 V) | Supported | Supported |
| 1 | 1 | Mode 3 | SCIF download | Supported | Supported |

Table 14 E1M-X V2N-M1 Boot Options

Note: BOOT2 is fixed at 1.

5 Boot Modes

The Renesas RZ/V2N samples the four boot-strap pins (BOOT0–BOOT3) at the rising edge of PORn. BOOT0/BOOT1 select the boot source; BOOT2 is fixed at 1 on the V2N family; BOOT3 selects the boot CPU (high = CA55, low = CM33). See Section 4.4 for the full mapping.

The carrier-board **MUST** drive BOOT0/BOOT1 (typically via a 2-position DIP switch with 10 kΩ pull-downs). The other two strap pins may be hard-strapped.

The DeepX DX-M1 has **no carrier-visible boot configuration** – it boots autonomously under control of the GD32 supervisor whenever the SoM 5 V rail is up and MODULE_EN is high. The M1 is not affected by the BOOT* pins.

Note: For details on the secure-boot signing flow, see **AN-010: Secure Boot and Code Signing**. For the DX-M1 first-inference walkthrough see **AN-009: DeepX DX-M1 First Inference**.



Figure 9 E1M-X V2N-M1 Boot Flow

6 Reset & Module Enable

The E1M-X V2N-M1 exposes the same control signals as V2N. Asserting PORn resets **both** the RZ/V2N and the on-module DX-M1; software does not need to manage the M1 reset separately.

| Pin | Direction | Description |
|-------------|-------------------|---|
| MODULE_EN | Input, open-drain | Internally pulled up to VDDIN. Pull low to disable the module (forces shutdown of both V2N and DX-M1). Leave floating if unused. |
| PORn | Input, open-drain | Internally pulled up to 1V8. Pull low to issue a power-on reset to both the RZ/V2N and the DX-M1. Minimum low-pulse width: TBD μs. |
| MODULE_STBY | Input, open-drain | Standby request. Reference firmware enters RTC-only standby; the DX-M1 enters its lowest-power retention state. |

Table 15 Reset & Module Enable Signals



Figure 10 V2N-M1 Reset Timing Diagram

7 JTAG / SWD Debug

The E1M-X V2N-M1 exposes a 5-pin JTAG / SWD interface for programming and debug of the RZ/V2N. Signals operate at 1.8 V; carrier-board level shifters are required for 3.3 V debug probes. The DeepX DX-M1’s debug interface is **not** exposed to the carrier – its bring-up is autonomous and software-debuggable from the RZ/V2N host over PCIe.

| Pin | Signal | Description |
|-----|-------------------|---|
| AL1 | JTAG_nRST | Active-low reset to the SoC debug logic. |
| AJ1 | JTAG_TCK / SWDCLK | Test clock (JTAG) or serial-wire clock (SWD). |
| AJ2 | JTAG_TDI | Test data in (JTAG only). |
| AK2 | JTAG_TDO | Test data out (JTAG only). |
| AK1 | JTAG_TMS / SWDIO | Test mode select (JTAG) or serial-wire I/O (SWD). |

Table 16 JTAG / SWD Pinout

Note: Alp Lab recommends exposing the JTAG/SWD pins on a 10-pin Cortex-M debug header on the carrier board. Refer to **UG-E1M-X-001** §5.1 for the reference connector pinout.

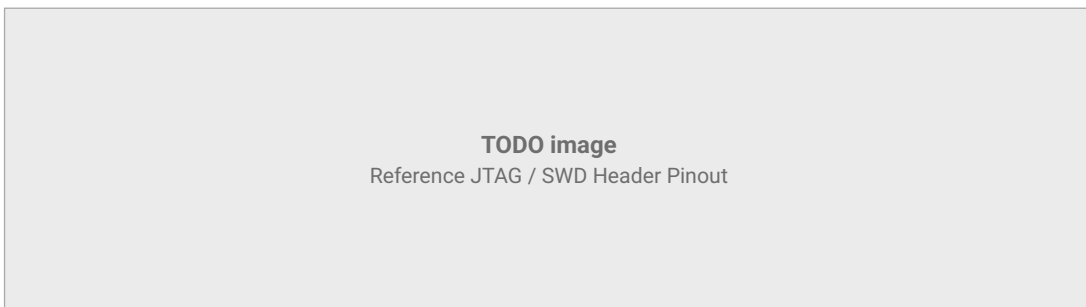


Figure 11 Reference JTAG / SWD Header Pinout

8 Interfaces

The E1M-X offers a wide set of interfaces to accommodate diverse system requirements:

- General-purpose digital I/O (GPIO)
- I²C, I³C, SPI, and UART serial buses
- USB 2.0 / 3.2 Gen 2 ports
- CAN FD (Flexible Data-rate)
- PCI Express Gen 3
- MIPI CSI and DSI for camera and display connectivity
- Dual Gigabit Ethernet with IEEE 1588 support

8.1 Ethernet

E1M-X V2N-M1 has two 1 Gbit Ethernet PHYs: the Realtek RTL8211FDI. The interfaces do not include on-module EMI or ESD protection; the user must provide external magnetics transformers, connectors, and EMI/ESD protection on the carrier board.

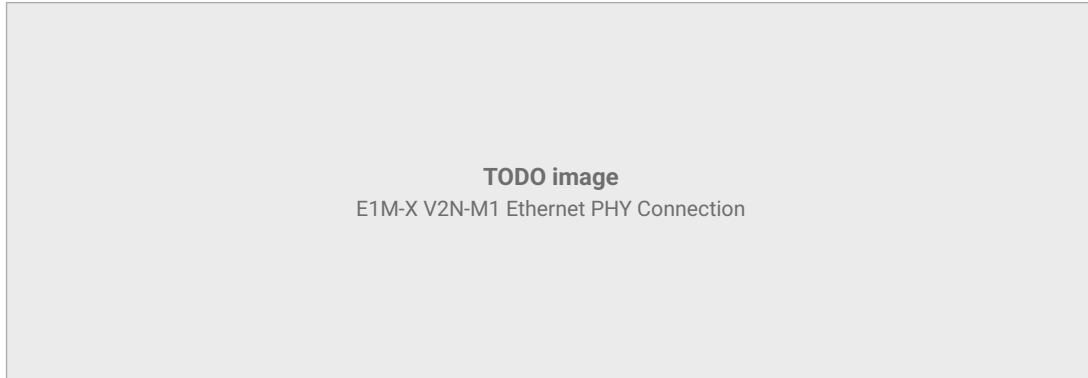


Figure 12 E1M-X V2N-M1 Ethernet PHY Connection

8.2 USB

E1M-X V2N-M1 has one USB 2.0 and one USB 3.2 Gen 2 interface. USB 2.0 supports Host/Function; USB 3.2 is Host-only.

| Pin Number | Pin Name | Peripheral | Description |
|------------|---------------|------------|---|
| C1 | USB0_30_D_N | USB0 | Route USB_N and USB_P as a differential pair with 90 Ω impedance. |
| B1 | USB0_30_D_P | | |
| F1 | USB0_30_RX0_N | | |
| E1 | USB0_30_RX0_P | | |
| I1 | USB0_30_TX0_N | | |
| H1 | USB0_30_TX0_P | | |
| G2 | USB2_20_ID | USB2 | Low: Host mode. NC: Device mode. |
| J2 | USB2_20_N | | Route USB_N and USB_P as a differential pair with 90 Ω impedance. |
| I2 | USB2_20_P | | |
| F2 | USB2_20_VBUS | | Connect to USB VBUS 5 V. |

Table 17 E1M-X V2N-M1 USB Interface

8.3 PCIe

Renesas RZ/V2N has one PCIe® Gen3 2-lane interface. The PCIe interface is used to communicate with the standalone AI accelerator DeepX-M1 to sustain AI-computation performance. However, to increase user flexibility, the PCIe interface is multiplexed to work either with DeepX-M1 or exit the module for external connections.

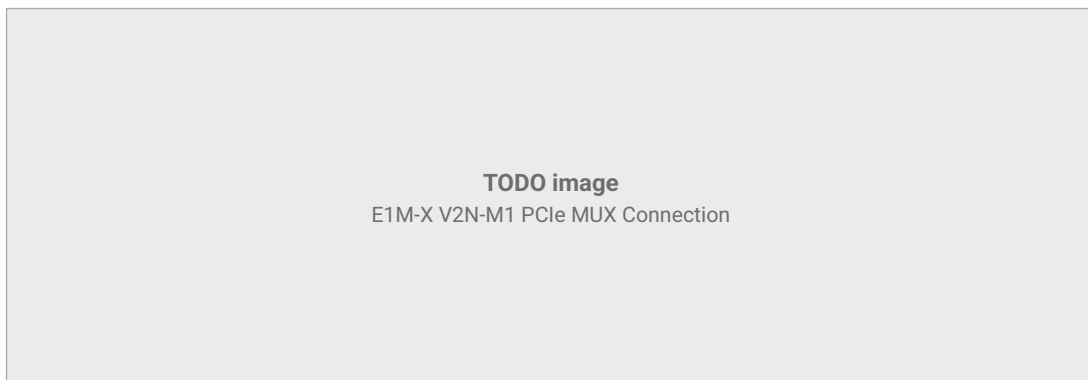


Figure 13 E1M-X V2N-M1 PCIe MUX Connection

8.4 Serial Interfaces

8.4.1 I²C

E1M-X has four I²C interfaces. Refer to the Renesas RZ/V2N series datasheet for full details. External pull-ups are required.

Note: The I2C3 interface is connected to the secondary MCU on E1M-X. It is handled by the Alp SDK™ from the main MPU.

8.4.2 I³C

E1M-X has one I³C interface. Refer to the Renesas RZ/V2N series datasheet for full details. External pull-ups are required.

8.4.3 UART

E1M-X has two UART interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.4 SPI

E1M-X has three SPI interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.5 I²S

E1M-X has two I²S interfaces. Refer to the Renesas RZ/V2N series datasheet for full details.

8.4.6 CAN Bus

E1M-X includes two optional CAN-BUS PHYs to simplify carrier-board hardware design. When the internal PHY is used, the user must add termination, ESD, and EMI protection components on the carrier board.

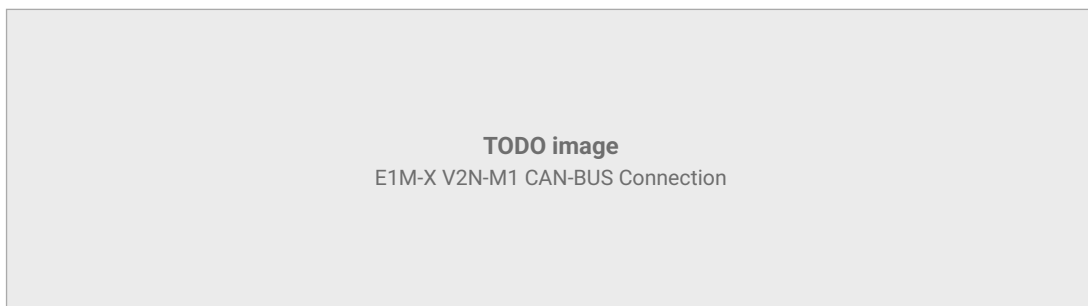


Figure 14 E1M-X V2N-M1 CAN-BUS Connection

8.5 SD Card

E1M-X supports an external μ SD card over the SDIO interface. The SDIO lines have ESD protection and 22 Ω series resistors on the module, plus 1 M Ω pull-ups. SD-card power is supplied by E1M-X via SD_VDD_OUT; the voltage switches automatically between high-speed and low-speed modes.

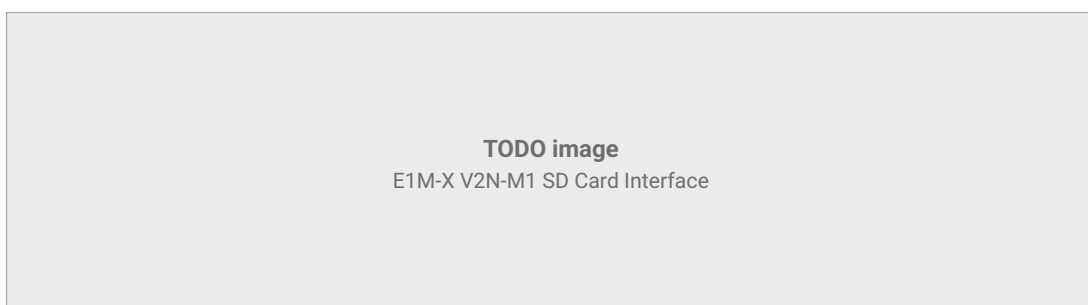


Figure 15 E1M-X V2N-M1 SD Card Interface

8.6 MIPI DSI Display & Backlight Controller

Renesas RZ/V2N has a 4-lane MIPI DSI interface for an external display, supporting up to FHD resolution. The RZ/V2N also includes an internal 3D GPU (Arm Mali™-G31) that can accelerate display rendering.

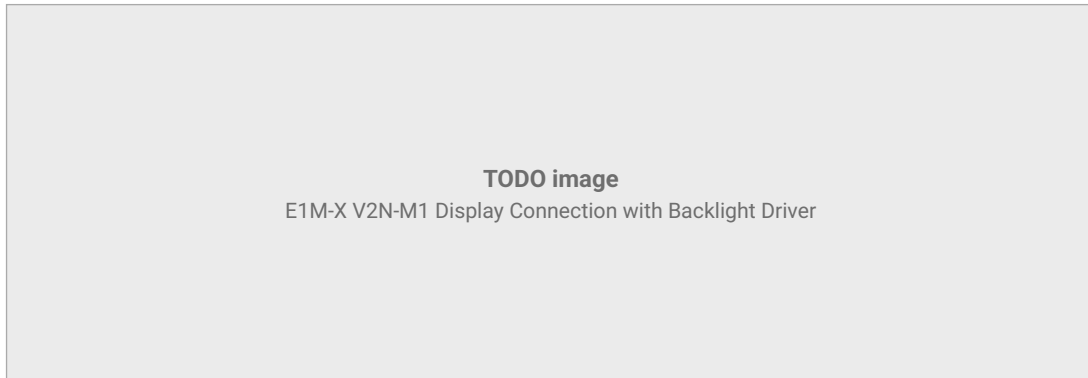


Figure 16 E1M-X V2N-M1 Display Connection with Backlight Driver

E1M-X has a backlight driver for external screens, controlled directly from the Alp SDK™. The driver is optional; outputs are configured via the BL_LED_A and BL_LED_K pins. The driver supports up to 10 LEDs in series, or 2P6S.

If the backlight driver is not needed, the BL_PWM signal can be exposed directly to drive an external backlight driver. The MIPI DSI interface does not include on-module EMI or ESD protection; protect the DSI lanes with a low-capacitance TVS array on the carrier board.

The feedback resistor value can be computed from the required LED current:

$$I_{LED} = 95 \frac{mV}{R_{FB}}$$

8.7 MIPI CSI Camera

Renesas RZ/V2N has two 4-lane MIPI CSI interfaces for external cameras. The RZ/V2N also includes an internal ISP (Arm Mali™-C55) that can accelerate image processing.

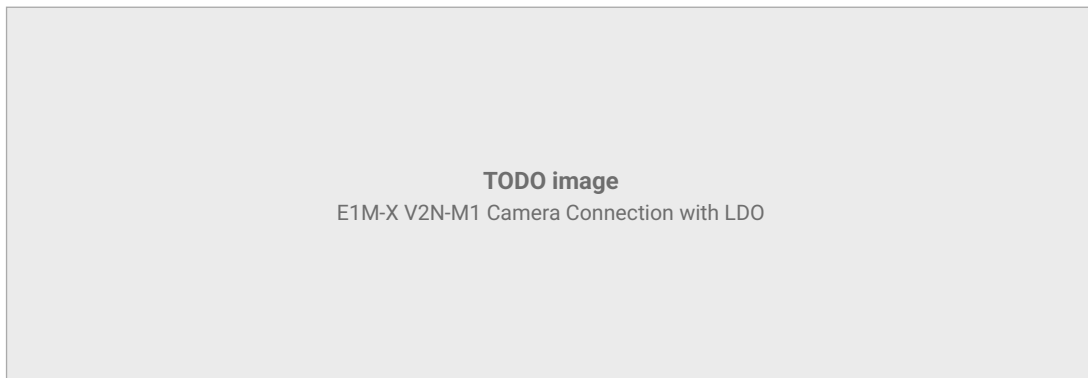


Figure 17 E1M-X V2N-M1 Camera Connection with LDO

E1M-X supports direct camera implementation via on-board LDOs. Place the feedback resistors as close as possible to the CAM_VFBx pins. The MIPI CSI interface does not include on-module EMI or ESD protection; protect the CSI lanes with a low-capacitance TVS array on the carrier board.

The output voltage is set by the divider:

$$V_{CAM} = 0.6 \text{ V} \times \left(1 + \frac{R_1}{R_2} \right)$$

To minimise feedback-pin current error, set the divider current to $100 \times$ the maximum feedback-pin current. The resulting series resistance limit is:

$$R_1 + R_2 \leq \frac{V_{OUT}}{I_{FB} \times 100}$$

8.8 Microphone – PDM

E1M-X supports up to 4 digital microphones over 2 PDM interfaces.

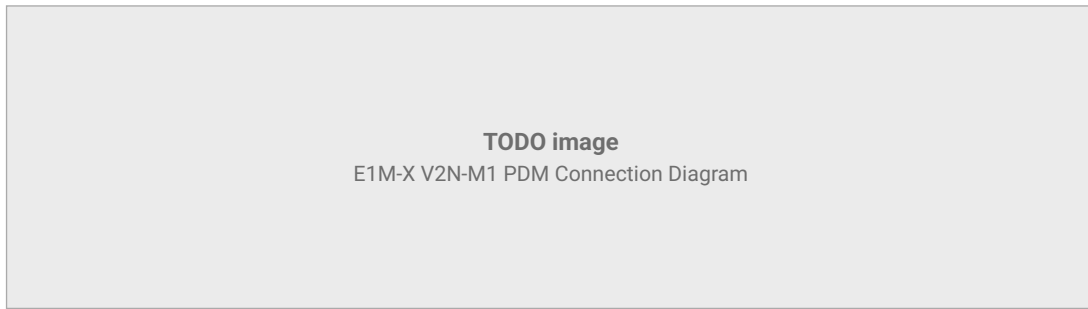


Figure 18 E1M-X V2N-M1 PDM Connection Diagram

Refer to the E1M-X hardware design guide for full details.

8.9 Analog Inputs

E1M-X has 8 analog input channels (ADC). The analog inputs are connected to the secondary MCU, which has a 12-bit ADC with a 5.3 Msps sampling rate. Analog inputs are referenced to 1V8.

Refer to the secondary-MCU datasheet for electrical characteristics. TBD.

8.10 Analog Outputs

E1M-X has 2 analog output channels (DAC). The analog outputs are connected to the secondary MCU, which has a 12-bit DAC with a 1 kHz sampling rate. Analog outputs are referenced to 1V8.

Refer to the secondary-MCU datasheet for electrical characteristics. TBD.

9 Components

9.1 Wireless Module & Antenna

E1M-X V2N-M1 integrates the Murata LBEE5HY2FY Wi-Fi 6 + BLE 5.4 combo module (based on Infineon CYW55513) on-module per **E1M Spec** §6.5. The antenna pads exit on a 50 Ω controlled-impedance trace; the carrier provides either a U.FL connector or a PCB antenna.

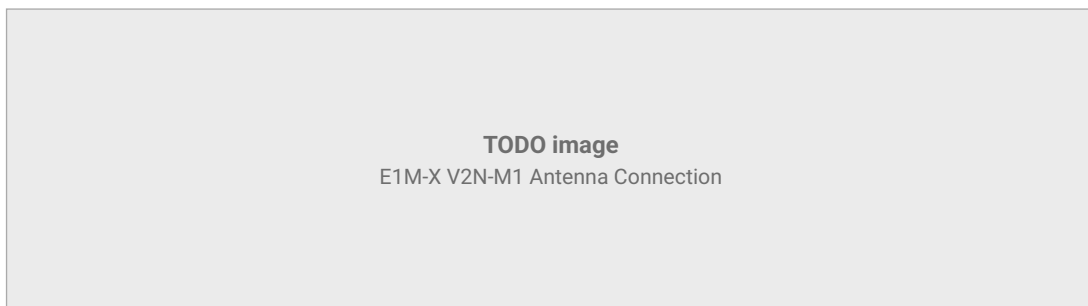


Figure 19 E1M-X V2N-M1 Antenna Connection

9.1.1 RF Characteristics

| Symbol | Description | Min | Typ | Max | Unit |
|---------------------------|------------------------------|------|-----|--------|------|
| Wi-Fi 6 (802.11ax) | | | | | |
| $f_{op,2.4}$ | 2.4 GHz band operating range | 2400 | – | 2483.5 | MHz |
| $f_{op,5}$ | 5 GHz band operating range | 5150 | – | 5850 | MHz |

| Symbol | Description | Min | Typ | Max | Unit |
|-------------------------|------------------------------------|------|-----|------|------|
| $f_{op,6}$ | 6 GHz band operating range | 5945 | – | 7125 | MHz |
| P_{TX} | TX output power (MCS0, 2.4 GHz) | – | TBD | TBD | dBm |
| P_{RX} | RX sensitivity (MCS0) | TBD | – | – | dBm |
| η | Max PHY throughput (single stream) | – | 143 | – | Mbps |
| Bluetooth LE 5.4 | | | | | |
| $f_{op,BLE}$ | Operating frequency range | 2402 | – | 2480 | MHz |
| $P_{TX,BLE}$ | TX output power | – | TBD | TBD | dBm |
| $P_{RX,BLE}$ | RX sensitivity (1 Mbps) | TBD | – | – | dBm |

Table 18 E1M-X V2N-M1 Wi-Fi 6 / BLE RF Characteristics

9.1.2 Antenna Options

The E1M-X V2N-M1 has **three** antenna pads (one per band):

- On-module U.FL connector** – connect an external antenna directly to the module.
- Carrier-board PCB antenna** – route each ANT_* pad as a 50 Ω controlled-impedance trace to a chip / PCB antenna.
- Carrier-board RF connector** – extend the 50 Ω trace to a U.FL / IPEX / SMA connector on the carrier.

Maximum antenna gain to maintain regulatory compliance is TBD dBi per band.

9.1.3 Regulatory Information

The on-module combo radio is pre-certified for the regions below. Reusing the module’s certifications on the customer’s end product requires following the integration guidelines (antenna gain, RF trace, enclosure) from the certification report.

| Region | Standard | Certificate ID | Notes |
|---------------|--------------|----------------|------------------------|
| United States | FCC Part 15 | TBD | Modular grant pending. |
| Europe | RED / CE | TBD | – |
| Canada | ISED RSS-247 | TBD | – |
| Japan | MIC (Japan) | TBD | – |

Table 19 Wireless Regulatory Approvals

Warning: Certifications apply only when the module is used with the antenna(s) listed in the certification report. Using an unlisted antenna voids the modular grant and requires re-certification on the customer’s end product.

9.2 Memories

E1M-X offers several memory options:

- **eMMC** – up to 256 GB.
- **LPDDR4X** – up to 8 GB.
- **NOR Flash** – on-module, boot-supported.

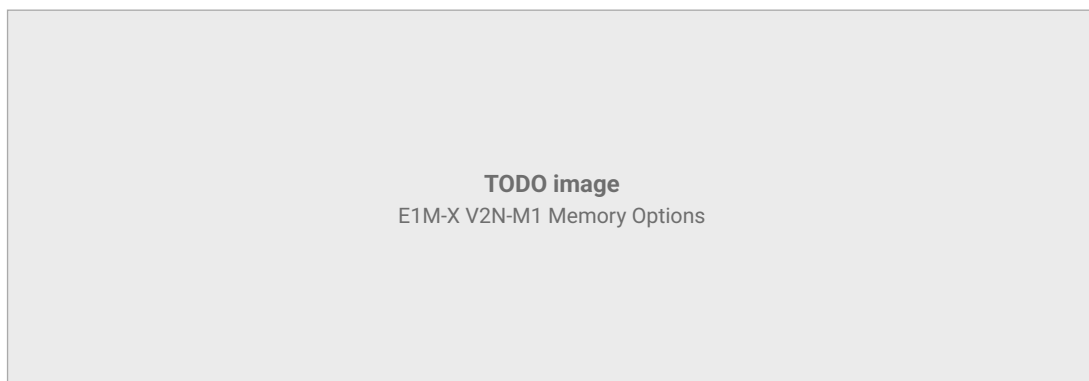


Figure 20 E1M-X V2N-M1 Memory Options

An optional EEPROM (N24S128C4DYT3G from onsemi) is also available on the board, connected through I2C0 on E1M-X. It can be flashed in production. I2C0 is also accessible on the E1M-X pinout. Refer to the E1M hardware design guide for details.

9.3 TPM 2.0 Module

E1M-X V2N-M1 includes a Trusted Platform Module (TPM 2.0) for secure-boot and key-storage applications.

9.4 Real-Time Clock (RTC)

A battery-backed real-time clock is available on-module; its 32 kHz output is exposed on RTC_CLKOUT.

9.5 PCB Temperature Sensor

An on-board PCB temperature sensor (TI TMP112D or equivalent) is available.

10 Environmental & Reliability

10.1 Operating & Storage Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|-----------|------|------|------|
| Ambient operating temperature | T_A | - 40 | +85 | °C |
| Storage temperature | T_{STG} | - 40 | +125 | °C |
| Relative humidity (operating, non-condensing) | RH | TBD | TBD | % |

Table 20 Environmental Conditions

Warning: Sustained AI workloads (DRP-AI3 + DX-M1 running concurrently) push the SoM toward its thermal envelope at +85 °C ambient. Active cooling or a copper-pour heatsink contact is recommended above 50% DX-M1 utilisation at the high end of the temperature range.

10.2 Reflow Profile

The E1M-X V2N-M1 is qualified per IPC/JEDEC J-STD-020 to MSL TBD. The recommended lead-free reflow profile is shown in Figure 21, measured on a JTR1000 convection reflow oven using ALPHA OM338 (SAC, Pb-free) solder paste. Peak package temperature is 241–244 °C. Customers must follow the reflow profile below and the dry-pack handling instructions in Section 15.3.

E1M-X V2N-M1 Reflow Profile – Pb-free (SAC)

Measured production profile · ALPHA OM338 paste · peak ≈ 243 °C · per IPC/JEDEC J-STD-020

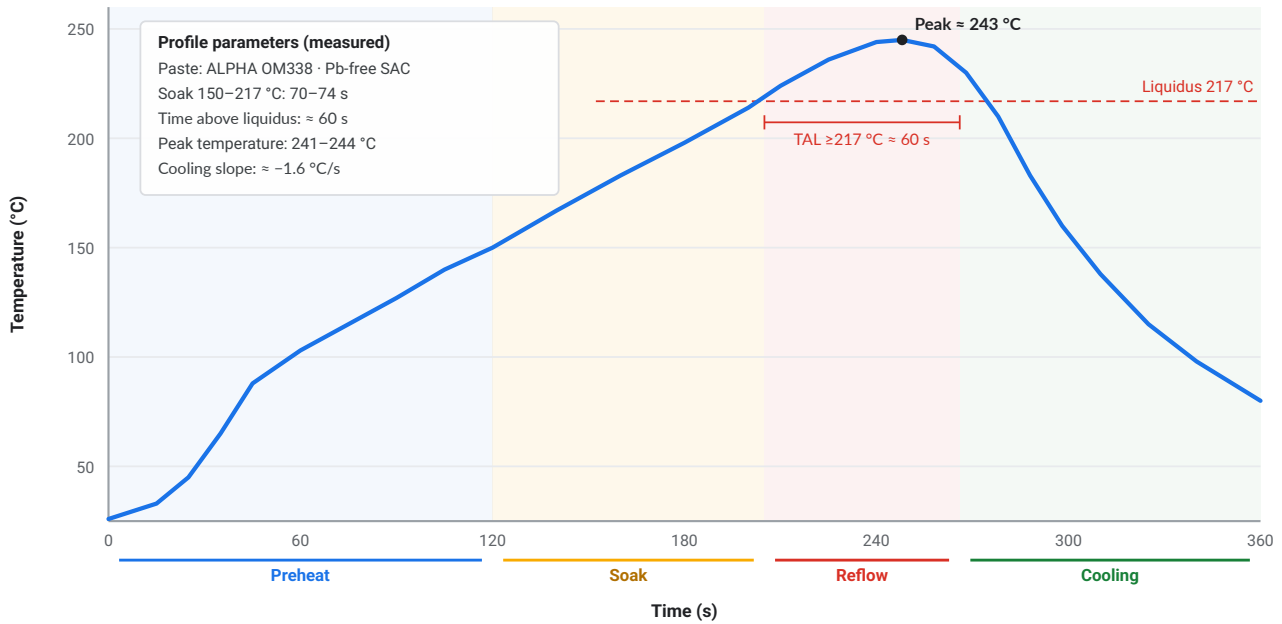


Figure 21 E1M-X V2N-M1 Recommended Reflow Profile (Pb-free, SAC)

| Parameter | Symbol | Min | Max | Unit |
|---|--------|-------|-----|------|
| Average ramp-up rate (T_L to T_P) | – | – | 3 | °C/s |
| Preheat / soak time (150–217 °C) | t_s | 60 | 120 | s |
| Time above liquidus (≥ 217 °C) | t_L | 45 | 90 | s |
| Peak package temperature | T_P | 241 | 244 | °C |
| Average ramp-down rate (T_P to T_L) | – | – 1.6 | – | °C/s |
| Time 25 °C to peak | – | – | 8 | min |

Table 21 Reflow Profile Parameters (Pb-free)

10.3 Reliability Data

| Parameter | Symbol | Value | Unit |
|---|--------|-------|--------|
| Mean Time Between Failures (Telcordia SR-332, $T_A = +25$ °C) | MTBF | TBD | h |
| Moisture Sensitivity Level | MSL | TBD | – |
| Qualified shelf life (in dry-pack) | – | TBD | months |

Table 22 Reliability Targets

11 Software & Operating System Support

The E1M-X V2N-M1 is supported by the open-source **Alp SDK™**. Out of the box, the SDK supports:

- **Bare-metal** application development on the RZ/V2N’s internal Cortex-M33 (200 MHz) or the on-module GD32 I/O-MCU (216 MHz).
- **Zephyr RTOS** on the Cortex-M33 cores and on the Cortex-A55 cluster (SMP).
- **Linux** (Yocto / buildroot BSP) on the quad Cortex-A55 application cluster, **with DX-M1 driver enabled** via the `alp_e1m_v2m_a55` board target.

| Target / Runtime | Bare-metal | Zephyr | Linux | DX-M1 driver |
|-------------------------------------|------------|--------|-------|--------------|
| GD32 I/O-MCU (Cortex-M33 @ 216 MHz) | Yes | Yes | – | – |

| Target / Runtime | Bare-metal | Zephyr | Linux | DX-M1 driver |
|-------------------------------------|------------|--------|-------|--------------|
| RZ/V2N internal M33 (200 MHz) | Yes | Yes | – | – |
| RZ/V2N Cortex-A55 (alp_e1m_v2n_a55) | Yes | Yes | Yes | – |
| RZ/V2N Cortex-A55 (alp_e1m_v2m_a55) | Yes | Yes | Yes | Yes |

Table 23 Software Support Matrix

Warning: Using the alp_e1m_v2n_a55 board target on a V2N-M1 module leaves the DX-M1 in reset. Always select alp_e1m_v2m_a55 to access the DX-M1.

Note: See the Alp SDK™ repository (docs/firmware-quickstart.md and docs/soms/v2n-m1.md) for the per-target build instructions. For deeper integration patterns, see AN-001 through AN-010; for DX-M1 specifically, AN-009.

12 Reference Schematic

The minimum carrier-board design below brings up an E1M-X V2N-M1 with a single 5 V input, reset push-button, boot-mode DIP switch, and JTAG/SWD debug header. The DX-M1 needs no carrier-side wiring – it lives entirely on the SoM behind the on-module PCIe mux.

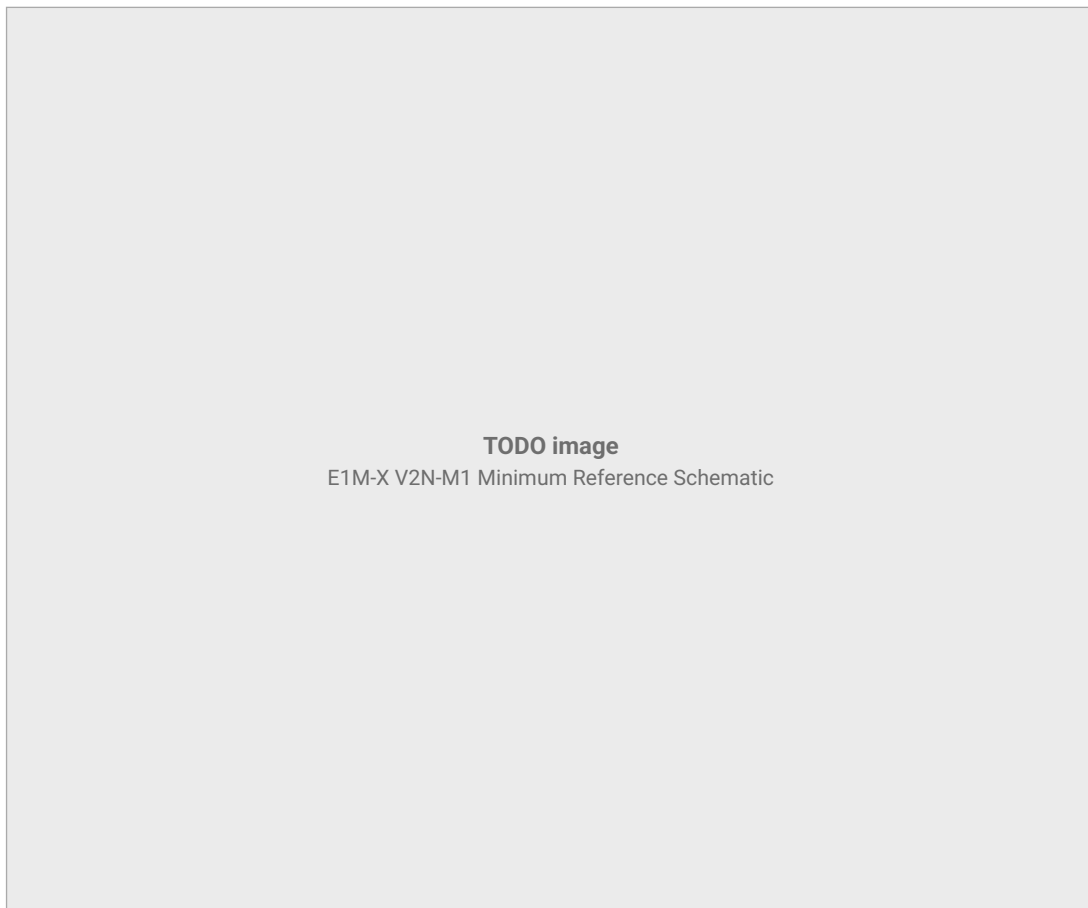


Figure 22 E1M-X V2N-M1 Minimum Reference Schematic

Required external components:

- 5 V power source (≥ 5 A peak) to VDD_5V_IN (T1, T2, U1, U2, V1, V2). Size for the higher peak (DRP-AI3 + DX-M1 + dual-Ethernet) compared to a V2N-only carrier.
- Bulk decoupling: $1 \times 10 \mu\text{F} + 1 \times 100 \text{ nF}$ close to VDD_5V_IN.
- Boot-mode 2-position DIP switch driving BOOT0, BOOT1 (with $10 \text{ k}\Omega$ pull-downs).
- Reset push-button between PORn (Z1) and GND.

- 10-pin Cortex SWD/JTAG header on JTAG_* pads (optional, for development).

Optional carrier-board components are described per interface in Section 8, and in detail in **HG-V2N-M1-001**.

13 Compliance & Certifications

13.1 Environmental Compliance

| Standard | Description | Status |
|--------------------------------------|--|-----------|
| RoHS 3 (EU 2015/863) | Restriction of hazardous substances | Compliant |
| REACH (EC 1907/2006) | Substances of very high concern | Compliant |
| Halogen-free (IEC 61249-2-21) | Br + Cl content limits | TBD |
| Conflict minerals (Dodd-Frank §1502) | Tin, tungsten, tantalum, gold sourcing | TBD |

Table 24 Environmental Compliance

13.2 Wireless Certifications

See Section 9.1.3 for the per-region wireless certification IDs.

13.3 Functional Safety & Industry-specific Compliance

The E1M-X V2N-M1 is not currently certified for safety-critical applications (IEC 61508, ISO 26262, IEC 62304, etc.). Contact Alp Lab for the most recent qualification status.

14 Mechanical & Footprint Dimensions

All dimensions are in mm unless otherwise noted.

14.1 Module Dimensions

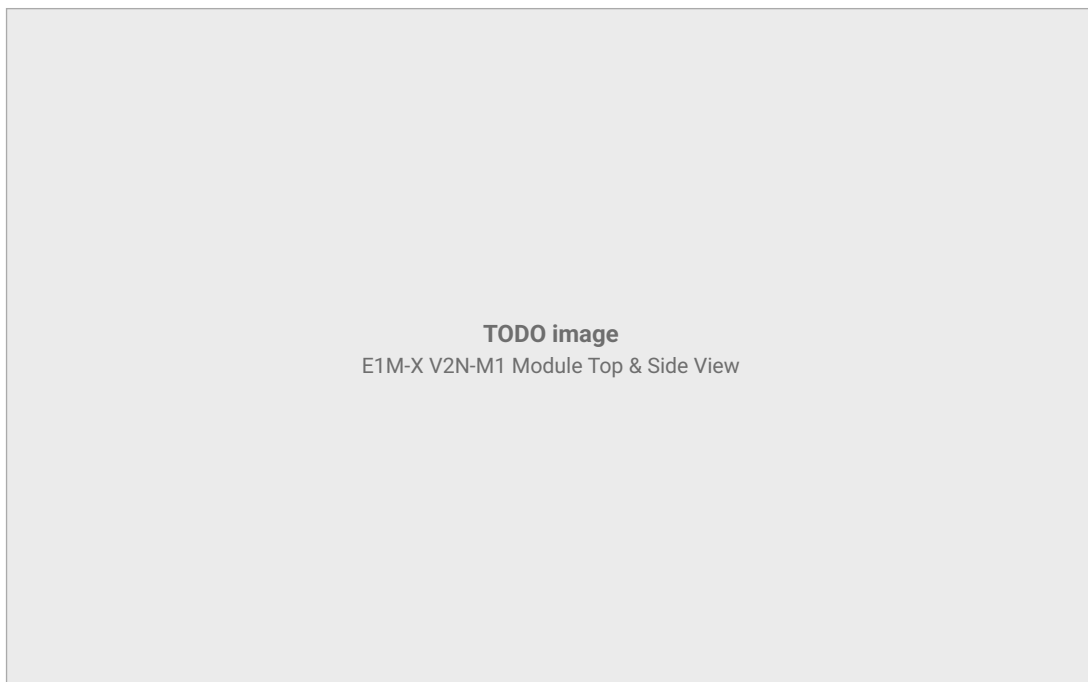


Figure 23 E1M-X V2N-M1 Module Top & Side View

| Parameter | Symbol | Min | Max | Unit |
|---|--------|------|------|------|
| Module length | L | 64.9 | 65.1 | mm |
| Module width | W | 44.9 | 45.1 | mm |
| Module height (PCB + tallest component) | H | – | TBD | mm |
| Module mass | m | – | TBD | g |

Table 25 E1M-X V2N-M1 Mechanical Dimensions

14.2 Recommended PCB Land Pattern

The recommended carrier-board land pattern follows IPC-7351 nominal density for LGA packages. Identical to the V2N family – V2N and V2N-M1 are **pin-compatible**.

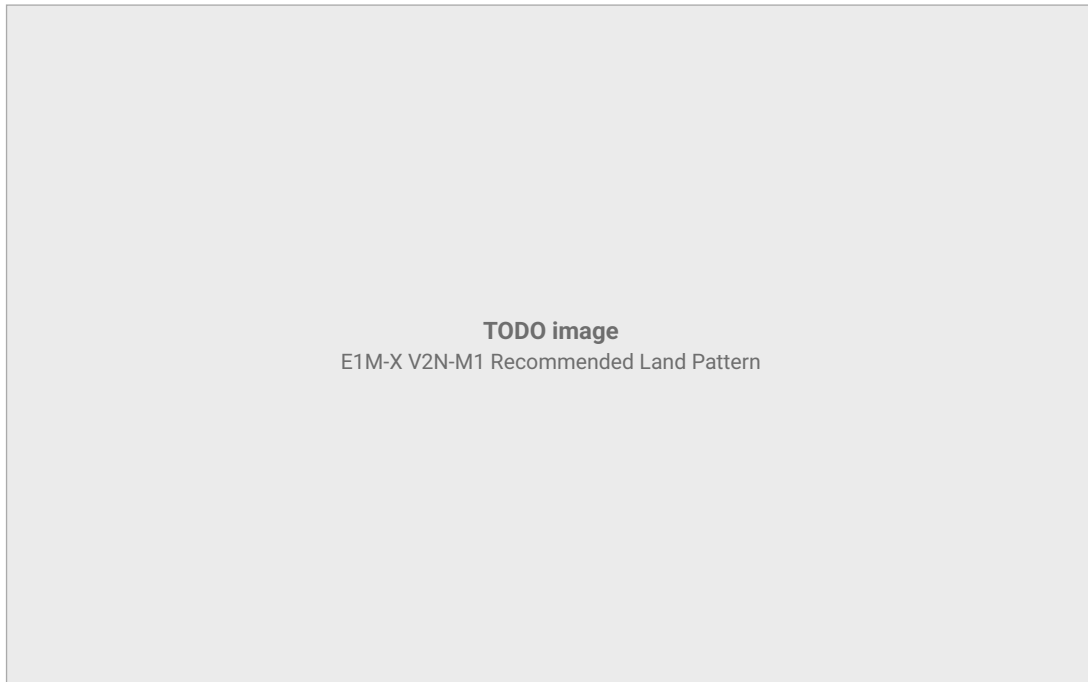


Figure 24 E1M-X V2N-M1 Recommended Land Pattern

| Parameter | Symbol | Value | Unit |
|---------------------------------|--------|-------------------------|------|
| Pad pitch (signal grid) | p | TBD | mm |
| Pad size (signal) | – | TBD × TBD | mm |
| Pad size (GND ring) | – | TBD × TBD | mm |
| Stencil material | – | Nano-coated steel mesh | – |
| Stencil thickness (recommended) | t | 80 | µm |
| Solder-mask opening | – | Non-solder-mask-defined | – |

Table 26 Land Pattern Parameters

14.3 Keep-Out Zones

Carrier boards must keep the area directly beneath the module clear of components taller than TBD mm. RF traces (especially the three antenna feeds) must be routed away from high-current digital paths.

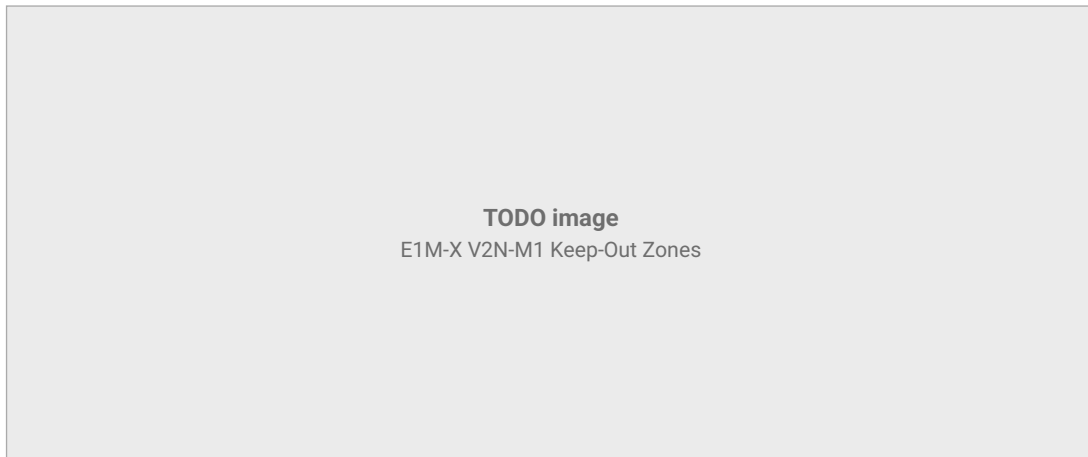


Figure 25 E1M-X V2N-M1 Keep-Out Zones

14.4 Module Marking

Each module is laser-marked on the top side with:

- Manufacturer logo (Alp Lab)
- Full MPN (e.g. E1M-V2M101)
- Production date code (YYWW)
- Serial number (10 characters)
- FCC ID, ISED IC, MIC marks (where applicable)
- Wi-Fi MAC address (last 4 digits)
- DX-M1 firmware version code

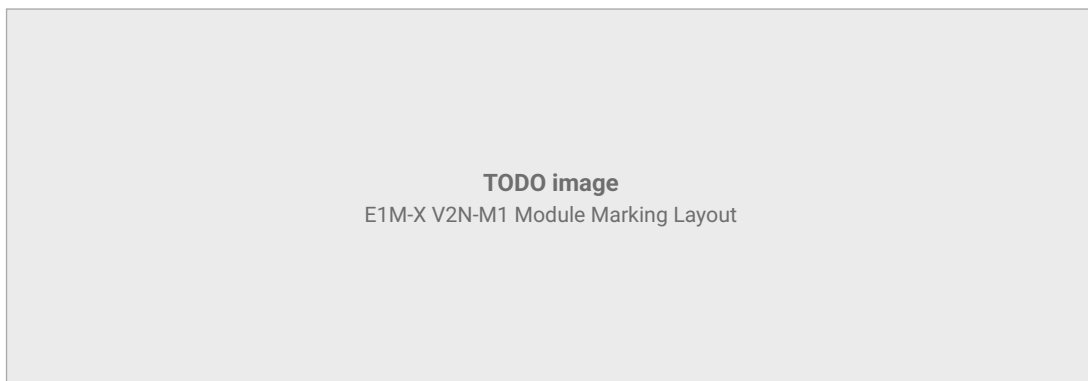


Figure 26 E1M-X V2N-M1 Module Marking Layout

15 Packaging

15.1 Tape & Reel

The E1M-X V2N-M1 is supplied in EIA-481-compliant carrier tape on 13" or 7" reels.

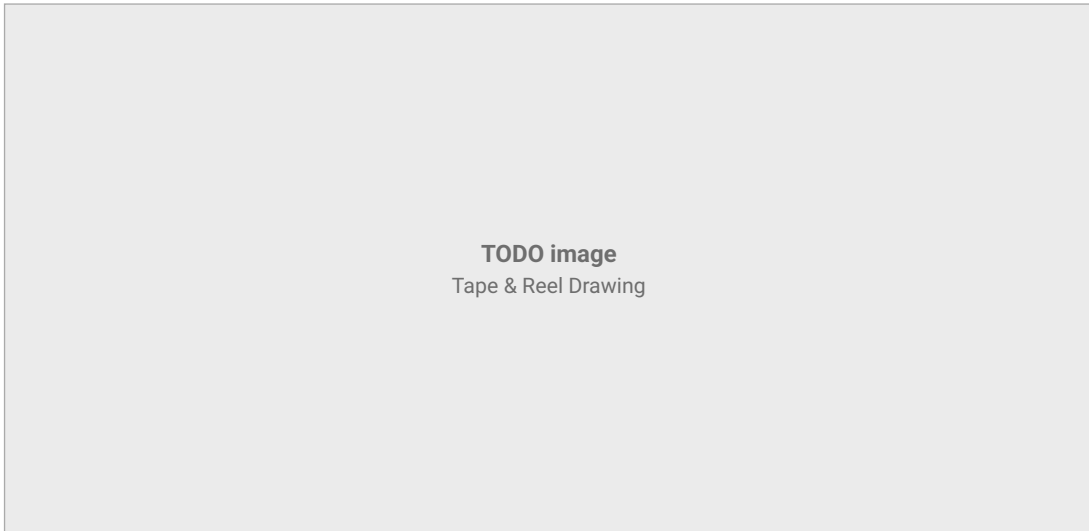


Figure 27 Tape & Reel Drawing

| Parameter | Symbol | Value | Unit |
|----------------------------|--------------|-------|------|
| Tape width | – | TBD | mm |
| Pocket pitch | P_{θ} | TBD | mm |
| Reel diameter (large reel) | D | 330 | mm |
| Reel diameter (small reel) | D | 180 | mm |
| Units per large reel | – | TBD | pcs |
| Units per small reel | – | TBD | pcs |

Table 27 Tape & Reel Specifications

15.2 Tray

A JEDEC-compliant tray is available for low-volume or prototyping orders.



Figure 28 Tray Drawing

15.3 MSL & Handling

The E1M-X V2N-M1 is classified to Moisture Sensitivity Level (MSL) TBD per IPC/JEDEC J-STD-020. Modules are shipped in dry-pack with desiccant and a humidity-indicator card.

After opening the dry-pack:

- Floor life: TBD hours at $\leq 30\text{ }^{\circ}\text{C}$ / $\leq 60\%$ RH.
- If floor life is exceeded before reflow, bake at TBD $^{\circ}\text{C}$ for TBD h before assembly.

Refer to IPC/JEDEC J-STD-033 for full moisture/reflow handling procedures.

16 Ordering Information

16.1 MPN Decoder

| Field | Example | Description |
|-------------------|---------|---|
| Family | E1M | Edge-1 AI Module standard footprint. |
| Form factor | -V | Implied 45 × 65 mm E1M-X. |
| Product line | V2M | Renesas RZ/V2N with on-module DeepX M1 accelerator (the “M” in V2M denotes the M1). Sibling line V2N omits the DX-M1. |
| Memory tier | 1 | 1 = lower memory tier (32 Gbit LPDDR4X + 32 Gbit eMMC). 2 = higher tier (64 Gbit LPDDR4X + 128 Gbit eMMC). |
| Hardware revision | 01 | Two-digit revision; incremented on form-fit-function changes. |

Table 28 E1M-X V2N-M1 MPN Convention

Note: Example: **E1M-V2M101** = E1M-X form factor, RZ/V2N + DX-M1, memory tier 1, hardware rev 01.

16.2 Ordering Matrix

| MPN | CPU | LPDDR4X | eMMC | AP cores | RT cores | AI | Temp. (°C) |
|------------|--------------------|---------|--------------------|-----------------|--|----------------------------------|-------------|
| E1M-V2M101 | R9A09G056N44GB#001 | 32 Gbit | eMMC 5.1, 32 Gbit | A55 4 × 1.8 GHz | V2N M33 1 × 200 MHz I/O MCU M33 1 × 216 MHz | V2N: 4 TOPS DeepX M1: 25 TOPS | - 40 to +85 |
| E1M-V2M102 | | 64 Gbit | eMMC 5.1, 128 Gbit | | | | |

Table 29 Ordering Information

All configurations above include:

- 2.4 GHz / 5 GHz / 6 GHz Wi-Fi® + Bluetooth® 5.4 combo module
- 2 × 1 Gbit Ethernet PHY
- 1 × display backlight driver
- 4 × LDOs for external cameras
- NOR Flash (size TBD)
- I/O MCU Cortex-M33 (216 MHz)
- TPM (secure chip)
- EEPROM
- RTC
- Temperature sensor
- DeepX DX-M1 25-TOPS AI accelerator (PCIe-attached on-module)
- 2 × LPDDR5X companion memory for DX-M1
- SPI NAND companion storage for DX-M1

RoHS-compliant. Contact Alp Lab for custom assembly variants (lead finish, ball material, etc.).

17 References & Related Documents

| Ref. | Title | Source |
|------|--|-------------------------|
| [1] | Renesas RZ/V2N Hardware Reference Manual | Renesas Electronics |
| [2] | Renesas RZ/V2N Series Datasheet | Renesas Electronics |
| [3] | DeepX DX-M1 Hardware Integration Manual | DeepX (vendor-supplied) |
| [4] | DeepX DX-COM™ User Guide | DeepX (vendor-supplied) |

| Ref. | Title | Source |
|------|---|---|
| [5] | E1M™ Specification | E1M-STD-1.0 / github.com/alpDevs/e1m-spec |
| [6] | E1M-X V2N-M1 Hardware Design Guide | Alp Lab (HG-V2N-M1-001) |
| [7] | E1M-X V2N Datasheet (sibling, without DX-M1) | Alp Lab (DS-V2N-001) |
| [8] | E1M-X EVK User Guide | Alp Lab (UG-E1M-X-001) |
| [9] | E1M-X EVK Getting Started Guide | Alp Lab (QS-E1M-X-EVK-001) |
| [10] | AN-009: DeepX DX-M1 First Inference Walkthrough | Alp Lab |
| [11] | Alp SDK™ Documentation | github.com/alpDevs/alp-sdk |
| [12] | IPC/JEDEC J-STD-020 – Reflow Profile | JEDEC |
| [13] | IPC/JEDEC J-STD-033 – Moisture/Reflow Handling | JEDEC |

Table 30 Related Documents

18 Revision History

| Revision | Changes | Date |
|----------|--|---------------|
| 0.1 | Initial draft (docx port). | December 2025 |
| 0.2 | Second draft. Added DeepX DX-M1 standalone AI accelerator description and PCIe-multiplexing details. | January 2026 |
| 0.3 | SoM-typical sections added: Module Variants, Recommended Operating Conditions, ESD & Latch-up, Thermal Characteristics, Power Architecture / Power-Up Sequence / Power Consumption, Boot Modes (top-level), Reset & Module Enable, JTAG / SWD Debug, Wireless RF/Antenna/Regulatory subsections, Environmental & Reliability, Software & OS Support, Reference Schematic, Compliance & Certifications, Mechanical & Footprint subsections, Packaging subsections, MPN Decoder, References, Legal Notices. | May 2026 |
| 0.4 | <ul style="list-style-type: none"> Pin-out drawing added: top-view, colour-coded 496-pad E1M-X diagram generated from the pin tables. On-module interface ESD/EMI protection removed except on the SDIO / SD-card interface; carrier board must now provide ESD/EMI protection on Ethernet, MIPI DSI, and MIPI CSI. Reflow profile populated (Pb-free, ALPHA OM338, peak 241–244 °C) with a parameters table. SMT stencil specified (nano-coated steel mesh, 80 µm). | June 2026 |
| 0.5 | Cover page: replaced the block-diagram placeholder with front/back product photos of the E1M-X V2N-M1 module (with DeepX DX-M1). | July 2026 |
| 0.6 | Cover photos swapped to transparent-background versions. | July 2026 |

Table 31 Revision History

19 Legal Notices

19.1 Disclaimer

The information in this document is provided in connection with Alp Lab AB products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document. Alp Lab reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time without notice.

Alp Lab products are not authorised for use as critical components in life-support devices, safety-critical equipment, military applications, or any other application where failure of the product could reasonably be expected to result in personal injury or significant property damage, without the express written approval of an officer of Alp Lab AB.

19.2 Trademarks

Alp Lab, **Alp SDK™**, **E1M™**, **E1M-X™**, and the Alp Lab logo are trademarks of Alp Lab AB. **Arm**, **Cortex**, **Mali**, and **Ethos** are trademarks of Arm Limited. **Renesas** and **RZ/V2N** are trademarks of Renesas Electronics. **DeepX**, **DX-M1**, and **DX-COM** are trademarks of DeepX. **Wi-Fi** is a trademark of the Wi-Fi Alliance. **Bluetooth** is a trademark of the Bluetooth SIG. All other trademarks are the property of their respective owners.

19.3 Export Control

This product may be subject to export-control regulations. The DeepX DX-M1 accelerator may be subject to additional export-control classifications beyond the base V2N silicon; consult Alp Lab and DeepX export-control guidance before re-exporting. The customer is responsible for complying with all applicable export-control laws.

19.4 Contact

For sales, technical support, or custom-variant requests:

- Web: alplab.ai
- Email: hello@alplab.ai
- Repository: github.com/alpDevs