E1M-X V2N-M1 Reliability Report

MTBF / FIT prediction — Telcordia SR-332

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1 Summary

This report gives the predicted reliability of the **E1M-X V2N-M1 System-on-Module** — Renesas RZ/V2N application processor with the on-module **DeepX DX-M1** AI accelerator — as **MTBF** and **FIT** (1 FIT = 1 failure per 10^9 device-hours). It is a **parts-count prediction** per **Telcordia SR-332 Issue 4**, summing the steady-state failure rate of all 1303 electrical components on the module. It is an intrinsic, random-failure estimate for the useful-life region; it excludes infant mortality (screened in production) and end-of-life wear-out.

> **Note:** **Headline — at the +55 °C operating reference (GF):** $\lambda \approx 2585$ FIT, giving an **MTBF of ≈ 387 000 hours**, equivalent to a **5-year field survival of ≈ 89.3%** and a **10-year survival of ≈ 79.7%** under continuous 24/7 use. See Section 4 and the +25… +85 °C sweep in Section 5.

> **Vendor data update (rev 0.2):** The DeepX DX-M1 accelerator FIT is now the **DeepX-published field-equivalent value — 8.245 FIT** at 60% CL from the DX-M1 HTOL qualification (JESD22-A108, 125 °C / 1000 h / 231 pcs, 0 failures; MTTF ≈ 1.21 × 10^8 h) — replacing the previous 80 FIT engineering estimate. This drops the headline from ≈ 2842 FIT / 352 000 h to ≈ 2585 FIT / 387 000 h. The Renesas SoC and Murata Wi-Fi module (†) remain on engineering estimates. See Section 6.

> **Reading this figure:** **MTBF is a fleet statistical measure, not a service life.** 352 000 h does not mean a unit lasts 40 years; it means one intrinsic failure is expected per 352 000 cumulative operating hours across a fielded population — i.e. ≈ 107 failures per 1000 units over 5 years of 24/7 use. The lower MTBF relative to a simple SoM reflects this module's high complexity (≈1300 parts, dual-PHY, multi-rail power, large memory and a second AI silicon device).

> **V2N vs V2N-M1:** This report covers the **V2N-M1** variant (DeepX DX-M1 populated). The **base E1M-X V2N** (without the DeepX subsystem) is covered by RL-V2N-001 (≈ 2443 FIT / ≈ 409 000 h at +55 °C). With the DeepX DX-M1 now on **vendor field-equivalent data** (8.245 FIT, Section 6) rather than the 80 FIT estimate, the accelerator **device itself adds only ≈ 8 FIT**; the remaining M1 subsystem delta is dominated by the PCIe/USB muxes and interconnect parts (Section 3).

1.1 Reference Condition

Parameter	Value
Prediction standard	Telcordia SR-332 Issue 4, Method I (parts count)
Environment	Ground Fixed, Controlled (GF)
Rated operating range	– 40 °C to +85 °C (industrial extended)
Headline operating ambient	+55 °C (representative loaded operating point)
Component-FIT build-up	+40 °C (Telcordia generic-device reference)
Duty cycle	100% (continuous, 24/7)
Component quality	Commercial, Quality Level II
Confidence level	50% (point estimate)

Table 1 Reference condition for the headline prediction

2 Method

The module failure rate is the series sum $\lambda_{\text{module}} = \sum_i n_i \cdot \lambda_i$ (any one part failing is a module failure; no on-module redundancy), and $\text{MTBF} = 1/\lambda_{\text{module}}$. Each λ_i embeds the Telcordia quality and reference-temperature factors. The per-class FIT is tabulated at the **+40 °C** Telcordia reference (build-up total ≈ 1132 FIT) and scaled to the **+55 °C** operating headline by the Arrhenius factor $\pi_T \approx 2.28$ on the silicon subtotal (Section 5), giving ≈ 2585 FIT. Non-electrical items (test pads, tooling) are excluded.

3 Failure-Rate Budget

The module carries **1303 electrical placements** across 98 line items. Silicon is ≈ 57% of the budget; the Renesas SoC and DeepX accelerator together are ≈ 11% (the DeepX device now on vendor data, Section 6). Values are at the +40 °C Telcordia reference build-up.

Component class	Qty	FIT total	Share
Ceramic capacitors (MLCC)	812	324.8	28.7%
Application SoC (Renesas RZ/V2N) †	1	120.0	10.6%
DC-DC switching regulators	5	76.0	6.7%
Wi-Fi / BLE module (Murata) †	1	60.0	5.3%
Flash — eMMC / OSPI NOR / SPI NAND §	3	56.2	5.0%
Chip resistors	372	55.8	4.9%
Load switches	10	50.0	4.4%
LPDDR4 / 4X DRAM §	3	50.0	4.4%
Crystals	6	48.0	4.2%
Ethernet PHY (2 × GbE)	2	40.0	3.5%
LDO regulators	6	36.0	3.2%
Clocks / RTC	4	36.0	3.2%
Other (level shifter, LED drv, temp, buffer, TVS, supercap, RF conn)	9	32.5	2.9%
Multi-output PMIC	1	25.0	2.2%
CAN transceivers	2	20.0	1.8%
Ferrite beads	38	19.0	1.7%
Power inductors	19	19.0	1.7%
Board-to-board connector	1	15.0	1.3%
Companion MCU (GD32)	1	15.0	1.3%
PCIe / USB muxes [M1]	2	12.0	1.1%
EEPROM	2	12.0	1.1%
Secure element	1	7.0	0.6%
AI accelerator (DeepX DX-M1) ‡ [M1]	1	2.5	0.2%
Total	**1303**	**≈ 1132**	**100%**

Table 2 E1M-X V2N-M1 failure-rate budget by class (+40 °C Telcordia reference)

Notes: **‡ vendor-qualified**: DeepX-published field-equivalent FIT for the DX-M1 (8.245 FIT @ 60% CL, JESD22-A108 HTOL; Section 6), back-referenced to the +40 °C build-up (÷ ≈ 3.27). **†** engineering estimate pending vendor reliability report (Renesas SoC, Murata Wi-Fi module). **§** chi-square 60% upper confidence limit from the JEDEC JESD47 HTOL qualification, accelerated to +40 °C with $E_a = 0.7$ eV (memory). [M1] marks parts unique to the V2N-M1 variant. Shares may not sum to 100% due to rounding.

4 Results

Metric	Value
Total failure rate, λ	2585 FIT
MTBF	387 000 h
MTBF (years, continuous)	44 yr
Survival R(1 yr)	97.76%
Survival R(3 yr)	93.43%
Survival R(5 yr)	89.29%
Survival R(10 yr)	79.74%

Table 3 Predicted reliability at the +55 °C operating headline (GF)

Mission time	Survival R(t)	Fails / 1000 units
1 year	97.76%	≈ 22.4
3 years	93.43%	≈ 65.7
5 years	89.29%	≈ 107.1
10 years	79.74%	≈ 202.6

Table 4 Expected intrinsic failures per 1000 fielded units (24/7, +55 °C)

5 Temperature & Environment Sensitivity

The silicon subtotal scales by $\pi_T = \exp\left[\frac{E_a}{k}(1/T_{\text{ref}} - 1/T)\right]$ with a generic $E_a = 0.7$ eV; passives, crystals, connectors and the PCB are held roughly constant. Each row assumes junctions track ambient (light-to-moderate load); under heavy SoC + DeepX load the junctions self-heat above ambient, so the hot-corner rows are **ambient-only** and optimistic until the thermal solution is folded in.

Ambient	π_T	λ (FIT)	MTBF (h)	MTBF (yr)	R(5 yr)
+25 °C	0.27	664	1 510 000	172	97.1%
+40 °C †	1.00	1132	884 000	101	95.2%
+55 °C *	3.27	2585	387 000	44	89.3%
+70 °C	9.66	6677	150 000	17	74.6%
+85 °C ‡	26.0	17 140	58 300	7	47.2%

Table 5 MTBF vs. ambient temperature (junction ≈ ambient)

* Headline operating point. † +40 °C Telcordia build-up reference. ‡ Rated maximum ambient.

The two AI silicon devices (Renesas SoC + DeepX) and the multi-rail power section are the hottest parts and dominate the temperature sensitivity — thermal design on those is the highest-leverage reliability action for the integrator.

6 Vendor Reliability Data (DeepX DX-M1)

The DeepX DX-M1 accelerator FIT used above is no longer an engineering estimate: it is the DeepX-published field-equivalent figure from the DX-M1 (IC) MTTF report. The DX-M1 is a 5 nm FCBGA device.

Parameter	Value
Life test	HTOL (JESD22-A108), 125 °C, 1000 h, 231 pcs, **0 failures**
Acceleration	$\mathrm{AF}_{\text{Total}} = \mathrm{AF}_{\text{Temp}}$ (Arrhenius) $\times$ $\mathrm{AF}_{\text{Voltage}}$ (E-model), 60% CL
FIT @ 60% CL	**8.245 FIT**
MTTF	≈ 1.21 × 10^8 h (121 287 290 h)

Table 6 DeepX DX-M1 field-equivalent reliability (DeepX MTTF report)

The 8.245 FIT is the **DX-M1 device** figure; it enters the module budget back-referenced to the +40 °C build-up (÷ ≈ 3.27) so the silicon-Arrhenius scaling of Section 5 reproduces 8.245 FIT at the +55 °C headline.

The DX-M1 additionally passed the full AEC-Q100 / JEDEC production qualification (DeepX DX-M1 Reliability Test Report, all lots 0 failures / PASS):

Stress	Condition	Method
HTOL	125 °C, ≥ V_{cc}max, 1008 h	JESD22-A108
ELFR	125 °C, 48 h, 800 ea/lot	AEC-Q100-008
Precon / MSL	MSL3, J-STD-020	JESD22-A113
HAST	110 °C / 85% RH, V_{cc}max, 264 h	JESD22-A101/A110
uHAST	130 °C / 85% RH, 96 h	JESD22-A102/A118
Temp cycle	− 55 °C ↔ +150 °C, 1000 cyc	JESD22-A104
HTS	150 °C, 1000 h	JESD22-A103
Mech. shock	1500 g, 0.5 ms	JESD22-B110
Vibration	50 g, 20 Hz–2 kHz	JESD22-B103
ESD	HBM ± 1000 V / CDM ± 250 V	AEC-Q100-002/011
Latch-up	± 100 mA / V_{max}, 125 °C	AEC-Q100-004

Table 7 DeepX DX-M1 qualification summary (all PASS)

7 Assumptions & Limitations

1. **Parts-count (Method I)**, not parts-stress — accepted at the design/datasheet stage and typically conservative for a derated design.
2. **Series reliability** — no on-module redundancy credited.
3. **Mixed FIT provenance.** The DeepX DX-M1 is now on **vendor field-equivalent data** (‡ — DeepX MTTF report, Section 6). The Renesas SoC and the Murata Wi-Fi module (†) remain engineering estimates pending vendor data; memory FITs (§) are conservative JEDEC-qual chi-square bounds. Substituting the two remaining † terms is now the main path to tightening the prediction.
4. **V2N-M1 variant.** The DeepX subsystem delta (Section 3) is based on the parts attributed to it in the netlist; confirm the fitted/DNP variant split.
5. **Excludes** solder-joint thermal fatigue (separate IPC-9701 analysis), infant mortality, and end-of-life wear-out.
6. **Point estimate at 50% confidence.**

8 Revision History

Revision	Changes	Date
0.1	Initial parts-count MTBF prediction (Telcordia SR-332 Issue 4) from the released E1M-X V2N + M1 netlist (1303 placements). Renesas SoC, DeepX accelerator and Wi-Fi module on engineering estimates; memory on JEDEC-qual chi-square bounds.	June 2026
0.2	DeepX DX-M1 accelerator FIT replaced with DeepX vendor field-equivalent data (8.245 FIT @ 60% CL; DX-M1 MTTF report). Added the Vendor Reliability Data section (Section 6) summarising the DX-M1 MTTF report and the AEC-Q100/JEDEC Reliability Test Report (all PASS). Headline improves to ≈ 2585 FIT / 387 000 h; budget reordered (DeepX now the smallest silicon term). Renesas SoC and Murata Wi-Fi module remain engineering-estimate (†) terms.	July 2026

Table 8 Document revision history