# E1M-X V2N Reliability Report

## MTBF / FIT prediction — Telcordia SR-332

**Document Number:** RL-V2N-001 **Revision:** 0.1 **Date:** June 2026 **Status:** Preliminary

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# 1 Summary

This report gives the predicted reliability of the **E1M-X V2N System-on-Module** (Renesas RZ/V2N, **base variant — no on-module DeepX accelerator**) as **MTBF** and **FIT** (1 FIT = 1 failure per $10^9$ device-hours). It is a **parts-count prediction** per **Telcordia SR-332 Issue 4**, summing the steady-state failure rate of the module's electrical components. It is an intrinsic, random-failure estimate for the useful-life region; it excludes infant mortality and end-of-life wear-out.

**Note:** **Headline — at the +55 °C operating reference (GF):** $\lambda \approx 2443$ FIT, giving an **MTBF of ≈ 409 000 hours**, equivalent to a **5-year field survival of ≈ 89.9%** and a **10-year survival of ≈ 80.7%** under continuous 24/7 use. See Section 4 and the +25…+85 °C sweep in Section 5.

**Reading this figure:** **MTBF is a fleet statistical measure, not a service life.** 409 000 h does not mean a unit lasts 47 years; it means one intrinsic failure is expected per 409 000 cumulative operating hours across a fielded population — i.e. ≈ 102 failures per 1000 units over 5 years of 24/7 use. The figure reflects this module's high complexity (≈1180 parts, dual-PHY, multi-rail power, large memory).

**V2N vs V2N-M1:** This report covers the **base V2N**. The **V2N-M1** variant (DeepX DX-M1 populated) is covered by RL-V2NM1-001 and predicts ≈ 2842 FIT / ≈ 352 000 h at +55 °C — the DeepX accelerator and its dedicated LPDDR4X + PCIe-mux subsystem add ≈ 122 FIT.

## 1.1 Reference Condition

| Parameter | Value |
|---|---|
| Prediction standard | Telcordia SR-332 Issue 4, Method I (parts count) |
| Environment | Ground Fixed, Controlled (GF) |
| Rated operating range | – 40 °C to +85 °C (industrial extended) |
| Headline operating ambient | +55 °C (representative loaded operating point) |
| Component-FIT build-up | +40 °C (Telcordia generic-device reference) |
| Duty cycle | 100% (continuous, 24/7) |
| Component quality | Commercial, Quality Level II |
| Confidence level | 50% (point estimate) |

**Table 1** Reference condition for the headline prediction

# 2 Method

The module failure rate is the series sum $\lambda_{\text{module}} = \sum_i n_i \cdot \lambda_i$ (any one part failing is a module failure; no on-module redundancy), and $\mathrm{MTBF} = 1/\lambda_{\text{module}}$. The per-class FIT is tabulated at the **+40 °C** Telcordia reference (build-up ≈ 1087 FIT) and scaled to the **+55 °C** operating headline by $\pi_T \approx 2.25$ on the silicon subtotal (Section 5), giving ≈ 2443 FIT.

# 3 Failure-Rate Budget

The base module carries ≈ 1180 electrical placements. Silicon is ≈ 55% of the budget; the Renesas SoC is ≈ 11%. Values at the +40 °C Telcordia reference build-up.

| Component class | Qty | FIT total | Share |
|---|---|---|---|
| Ceramic capacitors (MLCC) | 810 | 324.4 | 29.8% |
| Application SoC (Renesas RZ/V2N) † | 1 | 120.0 | 11.0% |
| DC-DC switching regulators | 5 | 76.0 | 7.0% |
| Wi-Fi / BLE module (Murata) † | 1 | 60.0 | 5.5% |
| Flash — eMMC / OSPI NOR / SPI NAND § | 3 | 56.2 | 5.2% |
| Chip resistors | 370 | 55.5 | 5.1% |
| Load switches | 10 | 50.0 | 4.6% |
| Crystals | 6 | 48.0 | 4.4% |
| Ethernet PHY (2 × GbE) | 2 | 40.0 | 3.7% |
| LDO regulators | 6 | 36.0 | 3.3% |
| Clocks / RTC | 4 | 36.0 | 3.3% |
| Multi-output PMIC | 1 | 25.0 | 2.3% |
| LPDDR4 DRAM (main) § | 1 | 20.0 | 1.8% |
| CAN transceivers | 2 | 20.0 | 1.8% |
| Ferrite beads | 38 | 19.0 | 1.7% |
| Power inductors | 19 | 19.0 | 1.7% |
| Board-to-board connector | 1 | 15.0 | 1.4% |
| Companion MCU (GD32) | 1 | 15.0 | 1.4% |
| EEPROM | 2 | 12.0 | 1.1% |
| Secure element | 1 | 7.0 | 0.6% |
| Other (level shifter, LED drv, temp, buffer, TVS, supercap, RF conn) | 9 | 32.5 | 3.0% |
| **Total** | **~ 1180** | **≈ 1087** | **100%** |

**Table 2** E1M-X V2N failure-rate budget by class (+40 °C Telcordia reference)

**Notes:** **†** engineering estimate pending vendor reliability report (Renesas SoC, Murata Wi-Fi module). **§** chi-square 60% upper confidence limit from the JEDEC JESD47 HTOL qualification, accelerated to +40 °C with $E_a = 0.7$ eV (memory). The DeepX accelerator and its dedicated LPDDR4X / PCIe muxes are **not** fitted on the base V2N. Shares may not sum to 100% due to rounding.

## 4 Results

| Metric | Value |
|---|---|
| Total failure rate, $\lambda$ | 2443 FIT |
| MTBF | 409 000 h |
| MTBF (years, continuous) | 47 yr |
| Survival R(1 yr) | 97.88% |
| Survival R(3 yr) | 93.78% |
| Survival R(5 yr) | 89.85% |
| Survival R(10 yr) | 80.74% |

**Table 3** Predicted reliability at the +55 °C operating headline (GF)

| Mission time | Survival R(t) | Fails / 1000 units |
|---|---:|---:|
| 1 year | 97.88% | ≈ 21.2 |
| 3 years | 93.78% | ≈ 62.2 |
| 5 years | 89.85% | ≈ 101.5 |
| 10 years | 80.74% | ≈ 192.6 |

**Table 4** Expected intrinsic failures per 1000 fielded units (24/7, +55 °C)

## 5 Temperature & Environment Sensitivity

The silicon subtotal scales by $\pi_T = \exp\left[\frac{E_a}{k}(1/T_{\text{ref}} - 1/T)\right]$ with a generic $E_a = 0.7$ eV; passives, crystals, connectors and the PCB are held roughly constant. Each row assumes junctions track ambient; under heavy load the junctions self-heat above ambient, so the hot-corner rows are **ambient-only** and optimistic until the thermal solution is folded in.

| Ambient | $\pi_T$ | $\lambda$ (FIT) | MTBF (h) | MTBF (yr) | R(5 yr) |
|---|---|---|---|---|---|
| +25 °C | 0.27 | 652 | 1 534 000 | 175 | 97.2% |
| +40 °C † | 1.00 | 1087 | 920 000 | 105 | 95.4% |
| +55 °C * | 3.27 | 2443 | 409 000 | 47 | 89.9% |
| +70 °C | 9.66 | 6249 | 160 000 | 18 | 76.0% |
| +85 °C ‡ | 26.0 | 15 006 | 66 600 | 8 | 51.7% |

**Table 5** MTBF vs. ambient temperature (junction ≈ ambient)

* Headline operating point. † +40 °C Telcordia build-up reference. ‡ Rated maximum ambient.

The Renesas SoC and the multi-rail power section are the hottest parts and dominate the temperature sensitivity — thermal design there is the highest-leverage reliability action for the integrator.

## 6 Assumptions & Limitations

1. **Parts-count (Method I)**, not parts-stress — accepted at the design/datasheet stage and typically conservative for a derated design.
2. **Series reliability** — no on-module redundancy credited.
3. **Mixed FIT provenance.** Renesas SoC and the Murata Wi-Fi module (†) are engineering estimates pending vendor data; memory FITs (§) are conservative JEDEC-qual chi-square bounds.
4. **Base variant** — the DeepX subsystem is excluded; see RL-V2NM1-001 for the M1.
5. **Excludes** solder-joint thermal fatigue, infant mortality, end-of-life wear-out.
6. **Point estimate at 50% confidence.**

## 7 Revision History

| Revision | Changes | Date |
|---|---|---|
| 0.1 | Initial parts-count MTBF prediction (Telcordia SR-332 Issue 4) from the released E1M-X V2N netlist (base variant, DeepX subsystem excluded). Renesas SoC and Wi-Fi module on engineering estimates; memory on JEDEC-qual chi-square bounds. | June 2026 |

**Table 6** Document revision history